XC3S1500 and XC3S1500L FPGA Errata and Deviations from Spartan-3 FPGA Data Sheet

EN089 (DS099-E06) (v2.6) June 24, 2008 **Errata Notice**

These errata apply ONLY to Spartan®-3 XC3S1500 and XC3S1500L FPGAs. These errata DO NOT apply to any other Spartan-3 FPGA. If using a different Spartan-3 FPGA, check for errata specific to that device.

Although Xilinx has made every effort to ensure that the XC3S1500/L devices are of the highest possible quality, these devices are subject to the limitations described in the following errata. Please review these errata to ensure that XC3S1500 or XC3S1500L FPGA devices meet your application requirements. Xilinx wants you to know about any known issues that may potentially affect your Spartan-3 FPGA application. This notice also includes advisories on the latest Spartan-3 FPGA design practices.

Obtaining the Most-Recent Errata Version

By its very nature, an errata notification is a living document and is subject to updates based on recent findings. If this document is printed or saved locally in electronic form, please check for the most recent release, available to registered users via the Xilinx web site.

http://www.xilinx.com/support/documentation/spartan-3_errata.htm

The Spartan-3 FPGA data sheet can be found on the Xilinx web site.

http://www.xilinx.com/support/documentation/spartan-3_data_sheets.htm

Contents

Devices Affected by This Errata

These errata only apply to the XC3S1500 or XC3S1500L FPGA as shown in Table 1. Both engineering sample (ES) and production silicon (no ES marking) are affected. The errata details may further limit the class of devices affected by a specific issue.

Table 1: **Spartan-3 XC3S1500 FPGAs Affected by This Errata**

Device Types:	XC3S1500 XC3S1500L
Packages:	All
Speed Grades:	All
Mask/Fabrication/Process Codes:	AFQ AGQ EGQ before date code 0532

All XC3S1500/L devices produced since 2006 have the mask/fab/process code EGQ and are free of all hardware errata.

XC3S1500L Discontinued

Note that the low-power version of the XC3S1500, the XC3S1500L, has been discontinued. See the discontinuation notice on xilinx.com:

http://www.xilinx.com/support/documentation/customer_notices/xcn07010.pdf

How to Identify an Affected Device

These errata affect all Spartan-3 FPGAs marked with an "XC3S1500" device type, including the XC3S1500L. The latest mask set, which is errata free, is fabricated at the UMC 300 mm wafer facility using 90 nm process technology and has an "EGQ" mask/fab/process code. This mask set began production in 2005 and were 100% of production starting during 2006. The previous mask revision was from the UCM 300 mm wafer facility had an "AGQ" mask/fab/process code. The initial mask set was fabricated at the UMC 200 mm wafer facility using 90 nm process technology. These devices have an "AFQ" mask/fab/process code, as indicated in Table 2. For more details see XCN05009, Addition of UMC 300 mm Wafer Fabrication for Spartan-3 Family.

Table 2: **Spartan-3 FPGA Production Facilities, Mask, and Fabrication/Process Codes**

Production Facility	Mask Revisions	Fabrication/ Process Code	Example Top Mark
UMC 200 mm, 90 nm (8D)	A	FQ	Figure 1
UMC 300 mm, 90 nm (12A)	A (initial) E (latest)	GQ	Figure 2

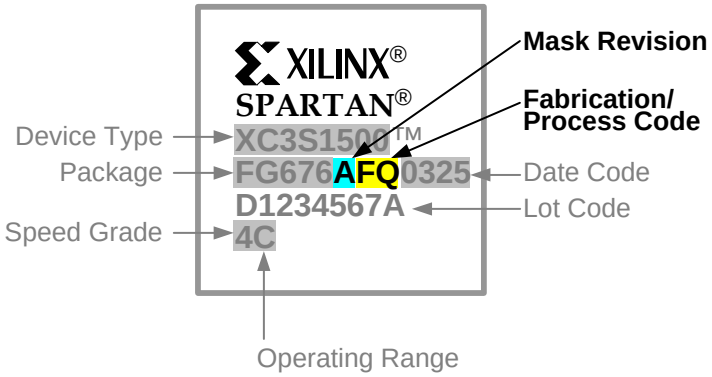

Figure 1: **Spartan-3 FPGA from UMC 200 mm facility with "FQ" Fabrication/Process Code Marking**

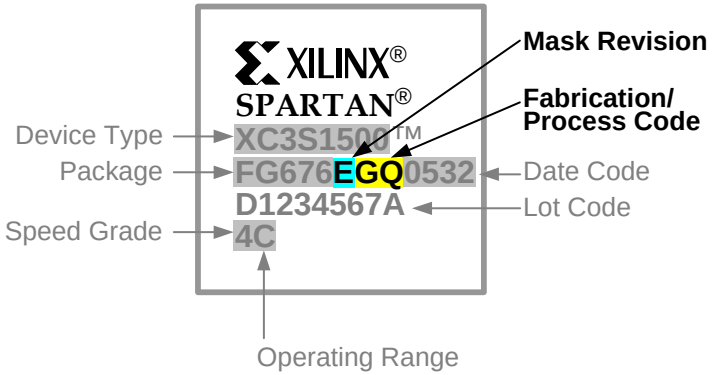

Figure 2: **Spartan-3 FPGA from UMC 300 mm facility with "GQ" Fabrication/Process Code Marking**

Hardware Errata Summary

Table 3 summarizes the known hardware issues with the XC3S1500 or XC3S1500L FPGA. See "**Hardware Errata Details**" for a detailed description of each known issue. Table 3 also shows which mask revision is affected by a particular errata item.

Table 3: **Hardware Errata Summary**

Errata Issue	Mask/Fabrication/Process Code		
	"AFQ"	**"AGQ"**	**"EGQ"**
DCM Using CLK2X Feedback May Lose Lock	Applies	N/A	N/A
Some Power Up Sequences where the VCCINT Supply Powers Up Last May Fail to Configure	Applies	N/A	N/A
If HSWAP_EN Input Is High, Pull-Up Resistors Are Momentarily Enabled on User-I/O at the End of Configuration	Applies	N/A	N/A
Readback Feature Not Available on Devices with "GQ" Fabrication/Process Code Marking Built before Date Code "0532"	N/A	Applies	N/A for devices with "0532" date code or later
Mask Revision	Initial	Revised	Latest
Products	XC3S1500	XC3S1500 XC3S1500L	XC3S1500 XC3S1500L

N/A=Not Applicable

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

DCM Using CLK2X Feedback May Lose Lock

Applications Affected by This Issue

This issue only affects applications that use the DCM CLK2X output signal as the CLKFB feedback input to the DCM.

This issue only affects the XC3S1500 FPGAs shown in Table 4, marked with the "AFQ" mask/fab/process code as shown in Figure 1.

Table 4: **Spartan-3 XC3S1500 FPGAs Affected by the CLK2X Feedback Issue**

Device Types:	XC3S1500
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

Description of Issue

The DCM compensates for delay on the routing network by monitoring an output clock, either CLK0 or CLK2X, through a BUFGMUX. If a design uses the CLK2X output as the feedback clock for a DCM, the LOCKED output may go Low and the DCM may stop operating correctly after tens of milliseconds.

Correction/Workaround/Resolution

Use feedback from the CLK0 (through a BUFGMUX) instead of CLK2X and change the CLK_FEEDBACK attribute from 2X to 1X. There is no difference in DCM performance. The CLK2X output is still valid and available for the application but it cannot be used for feedback to the CLKFB pin.

This issue is corrected on XC3S1500L FPGAs and on XC3S1500 FPGAs with a "BGQ" or "EGQ" mask/fab/process code marking, as shown in Figure 2.

Some Power Up Sequences where the VCCINT Supply Powers Up Last May Fail to Configure

Applications Affected by This Issue

This issue potentially affects some applications where the VCCINT power supply is the last supply to reach its Power-On Reset (POR) voltage threshold. This issue only affects devices with the "FQ" fab/process code, as indicated in Table 5.

Applications where VCCINT reaches its POR threshold first or second are not affected.

Table 5: **Spartan-3 XC3S1500 FPGAs Affected by the VCCINT Supply Sequence Issue**

Device Types:	XC3S1500
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

Description of Issue

Three voltage-supply inputs—VCCINT, VCCAUX and the VCCO supply to Bank 4—control the behavior of the Spartan-3 FPGA Power On Reset (POR) circuit. When applying power, a Power-On Reset (POR) circuit within the FPGA monitors each of these three rails. Once the voltages on each of the three rails exceed their respective POR thresholds, the POR circuit allows the FPGA to continue with its configuration process.

In the potentially failing condition, the VCCINT supply must be the last supply to reach its valid POR voltage and the ramp rate must be slower than 500 µS. When the FPGA fails to configure, the INIT_B remains Low and the FPGA ignores the PROG_B program pin. Even with the worst identified power sequence, actual failures only occur on a small percentage of devices, typically measured in parts per million. The issue is more pronounced at cold temperatures.

Correction/Workaround/Resolution

OPTION 1: Use Spartan-3 FPGAs fabricated from the 300 mm production facility ("AGQ" or "EGQ" mask/fab/process code).

SCD 0961 is not available for new orders but provided specially-screened FPGAs from the 200 mm production facility ("AFQ" mask/fab/process code).

OPTION 2: Use a power-on sequence where VCCINT is not the last supply to reach its POR threshold level.

VCCINT must reach its maximum POR threshold (V_{CCINTT} = 1.0V) before or coincident with VCCAUX reaching its minimum threshold (V_{CCAUXT} = 0.8V). This supply sequence and threshold relationship is illustrated in Figure 3.

Alternatively, VCCINT must reach its maximum POR threshold (V_{CCINTT} = 1.0V) before or coincident with VCCO_4 supplying I/O bank 4 reaching its minimum threshold (V_{CCO4T} = 0.4V). This supply sequence and threshold relationship is also illustrated in Figure 3.

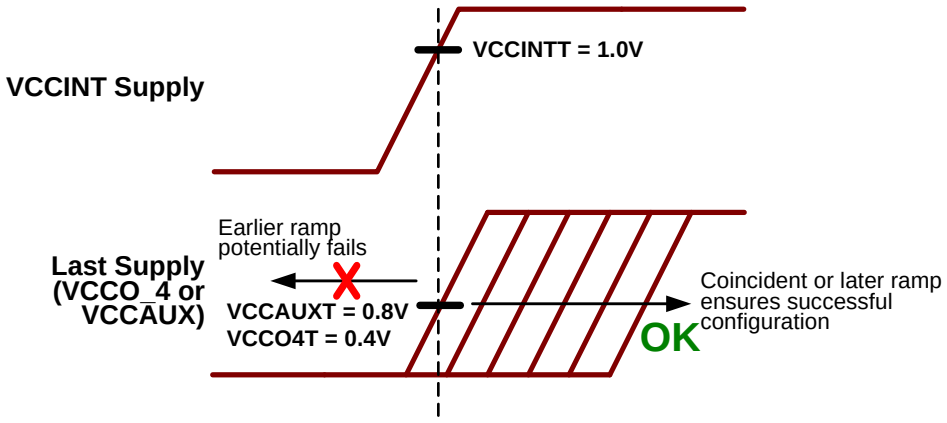

Figure 3: **Requirements when VCCINT is not the Last Supply**

The lowest power-consuming sequence is to apply VCCAUX before or coincident with VCCINT, then VCCINT followed by VCCO_4. If VCCINT is applied before VCCAUX, the VCCINT supply consumes a surplus current until the VCCAUX supply reaches its maximum POR threshold, VCCAUXT. This additional current is a few hundred to several hundred milliamps (mA). This additional current is not required for successful configuration and the surplus current disappears when VCCAUX is applied.

Power-sequencing restrictions apply neither for the VCCO supplies to I/O Banks 0 through 3 nor for the VCCO supplies to I/O Banks 5 through 7, as these voltage rails are not inputs to the POR circuit.

OPTION 3: In a system that requires that the VCCINT supply is last in the power-up sequence, ensure that it ramps to its maximum POR threshold voltage (V_{CCINTT} = 1.0V) in less than 500 µS, as shown in Figure 4.

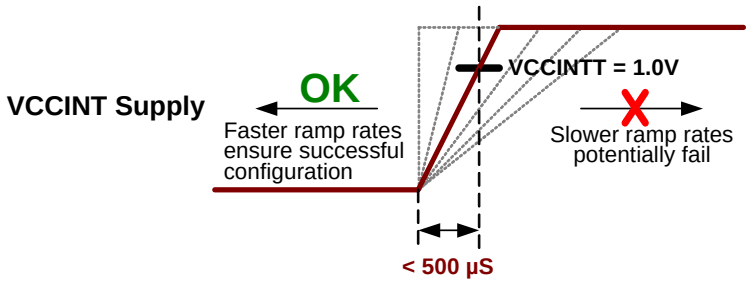

Figure 4: **Use Faster VCCINT Ramp Rate if VCCINT is Last Supply**

JTAG INTEST Instruction during UPDATE_DR Operation Potentially Forces Dedicated Configuration Input Pins to Invalid Value

Applications Affected by This Issue

This issue only affects applications that use the JTAG INTEST feature. If used at all, this feature is typically part of a JTAG-based device test procedure.

This issue does not affect applications that use the JTAG interface to download configuration data.

This issue only affects the XC3S1500 FPGAs shown in Table 6, marked with the "AFQ" mask/fab/process code as shown in Figure 1.

Table 6: **Spartan-3 XC3S1500 FPGAs Affected by the JTAG INTEST Instruction Issue**

Device Types:	XC3S1500
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

Description of Issue

The dedicated configuration input pins may be inadvertently forced High or Low during a JTAG INTEST operation.

After the device is configured, the M2, M1, M0, and HSWAP_EN pins may be driven High or Low without consequence. The INTEST operation does not affect these pins unless the FPGA is un-configured.

However, if the INTEST operation drives HSWAP_EN Low during an UPDATE_DR operation, then the FPGA restarts its configuration process. Because PROG_B follows HSWAP_EN in the JTAG chain, the Low in HSWAP_EN shifts into PROG_B, inadvertently triggering a device reconfiguration.

Correction/Workaround/Resolution

Do not shift a '0' into the HSWAP_EN position during device test using JTAG INTEST. If the JTAG operation consistently drives HSWAP_EN High, then the PROG_B pin is never driven Low during the operation. However, the other dedicated configuration inputs may still see invalid values.

This issue is corrected on XC3S1500L FPGAs and XC3S1500 FPGAs with a "BGQ" or "EGQ" mask/fab/process code marking, as shown in Figure 2.

If HSWAP_EN Input Is High, Pull-Up Resistors Are Momentarily Enabled on User-I/O at the End of Configuration

Applications Affected by This Issue

This issue only affects applications that drive HSWAP_EN High or leave it unconnected during configuration to disable weak pull-up resistors on the I/O. The issue has no effect on the use of pull-ups after configuration and the HSWAP_EN pin is a "don't care" after configuration.

This issue only affects the XC3S1500 FPGAs shown in Table 7, marked with the “AFQ” mask/fab/process code as shown in Figure 1.

Table 7: **Spartan-3 XC3S1500 FPGAs Affected by the HSWAP_EN Issue**

Device Types:	XC3S1500
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

Description of Issue

A High (the default) on HSWAP_EN disables weak pull-up resistors on all pins that are not actively involved in the configuration process, placing these pins in a high-impedance state. At the very end of the configuration process, the pull-up resistors within each user-I/O pin are momentarily enabled, just before the I/Os become operational.

Correction/Workaround/Resolution

Configure with pull-ups active by driving HSWAP_EN Low. This is the recommended solution, as users should not rely on floating outputs to hold the value during configuration. The output behavior can be guaranteed if pull-ups are enabled.

Alternatively, use external pull-downs to insure logical 0 if an I/O must be Low during configuration.

This issue is corrected on XC3S1500L FPGAs and XC3S1500 FPGAs with a “BGQ” or “EGQ” mask/fab/process code marking, as shown in Figure 2.

Readback Feature Not Available on Devices with “GQ” Fabrication/Process Code Marking Built before Date Code “0532”

Applications Affected by This Issue

This issue only applies to those designs using the Readback feature on the XC3S1500 or XC3S1500L FPGAs shown in Table 8 with an “AGQ” mask/fab/process code marking, or “EGQ” before date code 0532, as shown in Figure 2.

Table 8: **Spartan-3 XC3S1500 FPGAs Affected by the Readback Issue**

Device Types:	XC3S1500 XC3S1500L
Mask Revision Codes:	A (any date code) and E with date codes prior to “0532”
Fabrication/Process Codes:	GQ only
Packages:	All
Speed Grades:	All
Date Codes:	Mask Rev A: All Mask Rev E: Prior to 0532

This issue affects all manifestations of device readback, including Slave Parallel and Master Parallel readback and JTAG readback. Otherwise, the XC3S1500 or XC3S1500L FPGA functions normally.

Description of Issue

The readback feature is not available on devices with an "AGQ" Mask/Fabrication/Process Code marking.

Correction/Workaround/Resolution

XC3S1500 FPGAs with an "FQ" fab/process code marking fully support the Readback feature. Similarly, XC3S1500 or XC3S1500L FPGAs with an "EGQ" mask/fab/process code marking and with a date code of "0532" or later fully support Readback.

Advisories

This section advises designers of any potential software changes that may affect their XC3S1500 or XC3S1500L FPGA applications. Table 9 summarizes the advisories and indicates which software update will correct the issue.

Table 9: **Advisories and Software Update**

Advisory	ISE® Tool Version
Bitstream Update Required using ISE 6.3i, Service Pack 1 (SP1) or Later	ISE 6.3i, Service Pack 1
New FACTORY_JF Settings Required for Spartan-3 FPGA DCMs	ISE 8.2i
Two VREF Pins on I/O Bank 2 in XC3S1500 FG676 Are Connected to I/O	N/A

Bitstream Update Required using ISE 6.3i, Service Pack 1 (SP1) or Later

Spartan-3 FPGA block RAM internal timing is controlled by settings in the FPGA configuration bitstream. Through yield analysis, new optimal bitstream settings were identified for specific Spartan-3 device types. These new settings improve the block RAM internal timing margin, which consequently improves overall product yield and availability. **These new settings do not affect any timing in the FPGA application**, only internal timing relationships within the block RAM. The specific improved internal block RAM timing path is the relationship between the write-enable timing and the input latch-enable timing.

These new bitstream settings are now the default settings starting with Xilinx ISE 6.3i, Service Package 1, available for download from the Xilinx web site after September 13, 2004. XC3S1500 FPGAs are tested using these new bitstream settings beginning with date codes "0433", corresponding to Work Week 33 of 2004. Figure 5 shows an example top marking for a Spartan-3 FPGA. The relevant fields to identify an affected device are highlighted and include the **Device Type** and the **Date Code**.

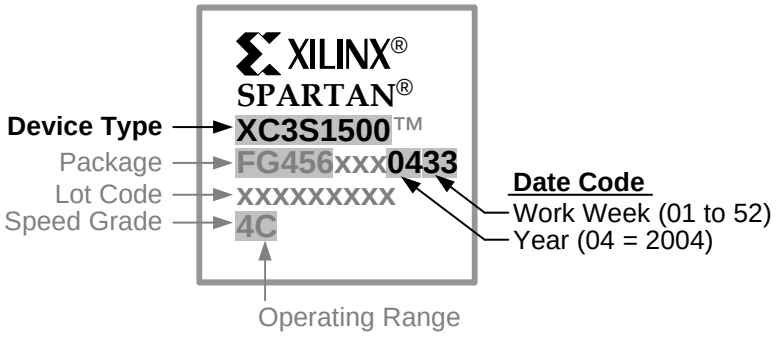

Figure 5: **Example Spartan-3 Device Package Markings**

Please regenerate any Spartan-3 FPGA configuration bitstreams created using software versions prior to Xilinx ISE 6.3i development software, Service Pack 1. By updating the bitstream, the application can use any existing or future production Spartan-3 FPGA device.

New FACTORY_JF Settings Required for Spartan-3 FPGA DCMs

Applications Affected by This Issue

This issue potentially affects applications that use Digital Clock Managers (DCMs). This issue only affects an application if and only if …

- The application uses one or more DCMs
- One of the DCMs uses phase shifting, either fixed or variable mode.
- The phase shift is negative, or very slightly positive (< 600 ps).

Unless a design meets these exact criteria, this issue can be safely ignored.

Description of Issue

The DCM automatically compensates for process, voltage, and temperature (PVT) changes and consequently it periodically updates its delay tap settings. The rate at which the update occurs is controlled by an internal attribute called FACTORY_JF. Xilinx has identified an optimal FACTORY_JF setting value (FACTORY_JF=8080). Other settings may potentially fail to track properly over process, voltage, and temperature.

Without using the optimal settings, the DCM could potentially, with low probability, fail to assert the LOCKED output, could lose lock, or could produce erroneous clock outputs.

Correction/Workaround/Resolution

The new optimal settings are applied starting in ISE 8.2i software. If using an earlier version, modify the new FACTORY_JF=8080 settings on each DCM instantiated in the design. Table 10 shows the best available options to update the DCM settings, depending on current design status.

Table 10: Options for Updated FACTORY_JF DCM Setting

Method	Design Status	Steps After Editing
FPGA Editor	Design complete, no further edits planned	Rerun Bitstream Generator
Constraints File	Design in progress	Rerun Design Implementation
VHDL or Verilog Source Code	Design in progress	Rerun complete flow

FPGA Editor

If the design is complete, with no further edits planned, then FPGA Editor offers the easiest method to update the FACTORY_JF setting.

- Invoke the FPGA Editor. On Windows PCs, select **Start → Xilinx ISE 6 → Accessories → FPGA Editor**.
- Select **File → Open**. Select the ***.ncd** file for the completed design. Set the **Edit Mode** to "**Read Write**" mode as shown in Figure 6.

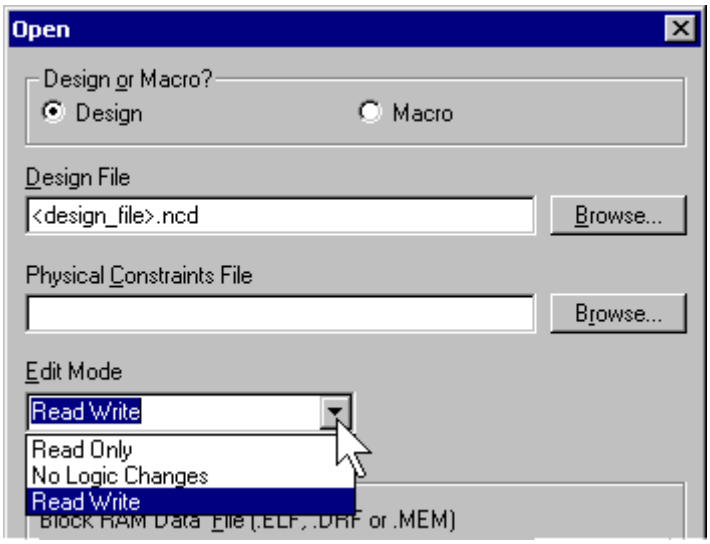

Figure 6: **Enable User Editing in FPGA Editor**

- For each DCM used in the design …
  - Select the DCM block using the cursor.
  - Click '**editblock'** from the right-most command button bar.
  - Click the Edit Mode button from the icon bar, as shown in Figure 7.

Figure 7: **Click "Edit Mode" Button to Change DCM Settings**

  - Check the two 0X80 options for the FACTORY_JF DCM attribute, as shown in Figure 8.

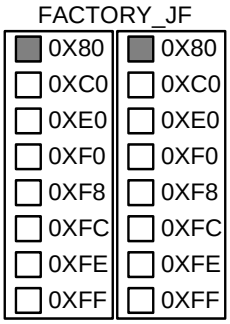

Figure 8: **Edit Block View of DCM FACTORY_JF Settings**

- After all DCMs are modified, save the design.
- Re-run the Bitstream Generator.

Constraints File

An easy option for designs in progress is to apply a user constraint. Edit an existing user constraints file (UCF) or create a new file and add the following constraint for every DCM used in the design.

```
INST <dcm_inst> FACTORY_JF = "8080";
```

VHDL

When using VHDL, update the FACTORY_JF values in both the DCM component declaration and in all component instantiations of the DCM. The following code snippet provides an example for XST VHDL. The VHDL source for other logic synthesis packages may vary slightly.

```
component DCM   -- DCM component declaration
   generic(
            . . .
            FACTORY_JF : bit_vector :=  x"8080";
            . . .
          );
. . .

DCM_INST : DCM   -- DCM instantiation
generic map(
            . . .
            FACTORY_JF => x"8080",
            . . .
           )
```

Verilog

When using Verilog, update the FACTORY_JF values as shown in the following XST Verilog code snippet.

```
DCM DCM_INST (
              . . .
             );
. . .
// synthesis attribute FACTORY_JF of DCM_INST is "8080"
. . .
// synopsys translate_off
. . .
defparam DCM_INST.FACTORY_JF = 16'h8080;
. . .
// synopsys translate_on
```

Clock Wizard

The Clock Wizard architecture wizard automatically generates a VHDL or Verilog description of a DCM design based on user input. If using Clock Wizard, update the HDL source as shown in the VHDL or Verilog examples above. Be forewarned that Clock Wizard overwrites the source file each time Clock Wizard is executed.

Other References

- **Answer Record #21559: What is the correct value for the FACTORY_JF attribute?** http://www.xilinx.com/support/answers/21559.htm

Two VREF Pins on I/O Bank 2 in XC3S1500 FG676 Are Connected to I/O

Applications Affected by This Issue

This issue only affects XC3S1500FG676 (or XC3S1500LFG676) applications that use an I/O standard requiring a VREF voltage reference in I/O Bank 2. I/O standards that require VREF voltage inputs include the various variants of GTL, HSTL, and SSTL. As indicated in Table 11,

only the XC3S1500 and XC3S1500L FPGAs in the FG676 package are affected. No other device types are affected and no other package options for the XC3S1500 are affected.

Table 11: **Spartan-3 XC3S1500 FPGAs Affected by the FG676 VREF Issue**

Device Types:	XC3S1500 XC3S1500L
Mask Revision Codes:	All
Fabrication/Process Codes:	All
Packages:	FG(G)676
Speed Grades:	All
Date Codes:	All

Description of Issue

Balls D25 and F25 on the FG676 package are labeled as VREF voltage reference inputs for I/O Bank 2. However, as noted in the data sheet, these two pads are not VREF inputs on the XC3S1500 FPGAs. When using an I/O standard that requires the VREF voltage reference input, the ISE software will treat these pins as VREF although they are standard I/O pins. The apparent VREF voltage will be lower than expected.

Correction/Workaround/Resolution

OPTION 1: Do not use I/O standards requiring VREF (GTL, HSTL, SSTL) on bank 2 in the XC3S1500 FG676.

OPTION 2: Use the following workaround. After the design is completed, use FPGA Editor to edit the settings for balls D25 and F25. Configure both pins as three-state output buffers and force the buffer into the high-impedance state by driving the T-input High.

Then, regenerate the configuration bitstream and disable the design rule checker (DRC). Otherwise, the DRC assumes that balls D25 and F25 are VREF pins and refuses to accept the new three-state buffer settings. Using the BitGen command-line program, the DRC software is disabled using the –d option.

See also Answer Record #20519 for additional information and a FPGA Editor macro to automate the recommended workaround.

- **Answer Record #20519**
  http://www.xilinx.com/support/answers/20519.htm

Design Software Requirements

The devices covered by these errata require the following Xilinx development software installations to create bitstream programming files.

- Xilinx ISE 8.2i or later
  (updates are available at the following web link)

  http://www.xilinx.com/support/download/index.htm

Additional Questions or Clarifications

If additional questions arise regarding these errata, please contact your local Xilinx field application engineer (FAE) or sales representative. Alternatively, please contact Xilinx Technical Support.

www.xilinx.com/company/contact.htm

Alternatively, please visit the Xilinx MySupport web site.

www.xilinx.com/support/mysupport.htm

Revision History

Date	Version No.	Description
16-DEC-2003	1.5	Initial release.
22-DEC-2003	1.6	Provided additional workarounds for **VCCO Fast Ramp** issue. Added workaround details and clarified that the LVDS_EXT standard is not supported the **LVDS** issue.
9-FEB-2004	1.7	Included both engineering samples (ES) and production devices in errata notification. Updated **VCCO Fast Ramp** issue. Updated **LVDS** issue, including information on output voltage levels and bitstream generator settings. Added **DCM Negative Phase Shift** issue. Added **Maximum Guaranteed DCM Clock Output Frequency** issue.
5-MAR-2004	1.8	The **VCCO Fast Ramp** issue, the **LVDS** issue, the **Maximum Guaranteed DCM Clock Output Frequency** issue and the **I/O Leakage** issue are now described in the **Spartan-3 FPGA Data Sheet**. These issues are no longer covered as errata topics.
15-APR-2004	1.9.1	Added **Readback** issue that only affects specially marked versions of the XC3S1500 FPGA.
22-SEP-2004	2.0	Added the **Reduced DLL Frequency** issue. Added the advisory about the **Block RAM Bitstream Change** implemented in ISE 6.3i, SP1. Removed **DCM Negative Phase Shift** issue as this is now fully documented in the Spartan-3 FPGA data sheet. Phase shifting is only supported in the DCM low-frequency mode. Updated the **Readback** issue to include identifying marking information.
20-OCT-2004	2.1	Removed the **Reduced DLL Frequency** issue. Updated link to online errata.
20-DEC-2004	2.2	Added **VCCINT Supply Sequence** issue. Added information about the top markings indicating the mask revision, fabrication facility, and process technology for a given Spartan-3 FPGA. Clarified which erratum applies to which mask revision. Added advisory on **FG676 VREF** issue. Added advisory on **New DCM FACTORY_JF Settings**.
7-JAN-2005	2.3	Changed the mask revision code for devices manufactured at the UMC 300 mm, 90 nm facility (12A) from 'B' to 'A' in Table 2. Also updated Table 8 for the 'A' mask revision code. Updated Table 3 and the Correction/Workaround/Resolution section of the **VCCINT Supply Sequence** issue as this issue was removed for devices manufactured at the UMC 300 mm, 90 nm facility (12A).
8-AUG-2005	2.4.1	Updated Table 2 and Table 3 to add mask revision 'E', which is errata-free for FPGAs with date codes of "0532" or later. Updated **Readback** because this issue is corrected for mask revision 'E' devices with date codes of "0532" or later. Updated workarounds section of **VCCINT Supply Sequence** issue to clearly define available options. Updated the advisory on **New DCM FACTORY_JF Settings** to clarify the conditions when the new settings are required.
14-DEC-2006	2.5	Added link to XCN05009 for details regarding addition of 300 mm fab. Updated **New DCM FACTORY_JF Settings** to note that ISE 8.2i automatically includes the new settings.
24-JUN-2008	2.6	Added Contents listing. Added note that XC3S1500L is discontinued. Added note that the errata-free mask set began production in 2005 and was 100% of production starting during 2006. Clarified workarounds for advisory on VREF pins. Updated links.