DEMO MANUAL DC1774A-C

LTC6431-15
50Ω Gain Block IF Amplifier

DESCRIPTION

Demonstration circuit 1774A-C is a 50Ω gain block IF amplifier featuring the LTC®6431-15. It is part of the DC1774A demo board family supporting the LTC643X-YY amplifier series. The DC1774A-C is optimized for a frequency range of 100MHz to 1200MHz and utilizes a minimum of passive external components to configure the amplifier for this application.

Because the LTC6431-15 has 50Ω single-ended input and output impedance, the demo circuit can be connected directly to most commercially available RF test equipment for the evaluation.

Design files for this circuit board are available at http://www.linear.com/demo

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PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, V_{CC} = 5V

Table 1. Typical Demo Board Performance Summary

SYMBOL	PARAMETER	CONDITIONS	VALUE/UNIT
Power Supply			
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus +OUT	4.75V to 5.25V
I_{CC}	Current Consumption	Total Current	90mA

FREQUENCY (MHz)	POWER GAIN S21 (dB)	OUTPUT THIRD-ORDER INTERCEPT POINT [1] OIP3 (dBm)	OUTPUT THIRD-ORDER INTERMODULATION [1] OIM3 (dBc)	SECOND HARMONIC DISTORTION [2] HD2 (dBc)	THIRD HARMONIC DISTORTION [2] HD3 (dBc)	OUTPUT 1dB COMPRESSION POINT P1dB (dBm)	NOISE FIGURE [3] NF (dB)
100	15.1	46.6	–89.2	–58.0	–88.0	20.0	3.8
200	15.4	46.7	–89.5	–58.0	–88.0	20.0	3.5
240	15.6	46.7	–89.3	–59.0	–88.0	20.3	3.4
300	15.5	46.6	–89.3	–60.0	–86.0	20.1	3.5
400	15.5	46.1	–88.3	–57.0	–87.0	20.3	3.5
500	15.4	45.3	–86.6	–55.6	–77.0	20.3	3.6
600	15.3	43.5	–83.1	–53.6	–69.0	20.4	3.7
700	15.2	42.2	–80.4	–51.9	–69.0	20.2	3.8
800	15.0	41.1	–78.1	–49.2	–65.0	20.1	4.0
900	14.8	39.5	–74.9	–46.7	–63.0	19.7	4.2
1000	14.7	38.7	–73.3	–45.0	–59	19.3	4.2
1100	14.5	38.0	–71.9	–40.8	–56.8	18.8	4.4
1200	14.3	38.0	–71.9	–38.4	–54.2	18.6	4.6

Notes: All measurements are referenced to J7 (Input Port) and J10 (Output Port).

1. Two-tone test condition: Output power level = +2dBm/tone; Tone spacing = 1MHz.
2. Single-tone test condition: Output power level = +6dBm.
3. Small-signal noise figure.

QUICK START PROCEDURE

Demo circuit 1774A-C can be set up to evaluate the performance of the LTC6431-15. Refer to Figures 4 and 5, for proper equipment connections and follow the procedure below:

Single-Tone Measurement:

Connect all test equipment as suggested in Figure 4.

1. The power labels of +5V and GND directly correspond to the power supply. Typical current consumption of the LTC6431-15 is about 90mA.
2. Apply an input signal to J7. A low-distortion, low noise signal source with an external high order lowpass filter will yield the best performance. The input signal is –10dBm.
3. Observe the output via J10. The measured power at the analyzer should be about +5dBm.

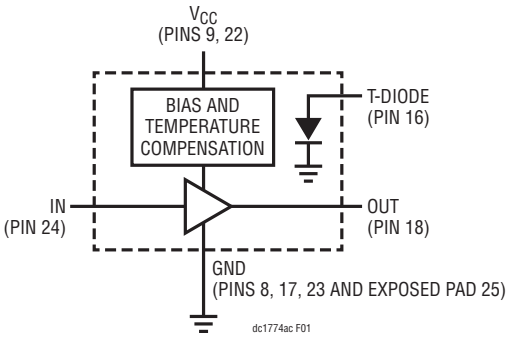

Figure 1. LTC6431-15 Device Block Diagram

Two-Tone Measurement:

Connect all test equipment as suggested in Figure 5.

1. The power labels of +5V and GND directly correspond to the power supply. Typical current consumption of the LTC6431-15 is about 90mA.
2. Apply two independent signals f1 and f2 from SG1 and SG2 at 240MHz and 241MHz respectively.
3. Monitor the output tone level on the spectrum analyzer. Adjust signal generator levels such that output power measures +2dBm/tone at the amplifier output J10, after correcting for external cable losses and attenuators.
4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. The frequencies of IM3_LOW and IM3_HIGH are 239MHz and 242MHz, respectively.

   For this setup, the Rohde and Schwarz FSEM30 spectrum analyzer was used. This spectrum analyzer has a typical 20dBm third-order intercept point (TOI). The Rohde and Schwarz FSU can also be used. The system as described can measure OIP3 up to 50dBm.

QUICK START PROCEDURE

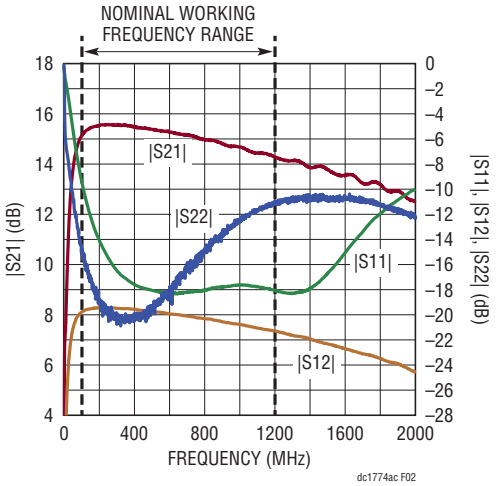

Figure 2. Demo Board S-Parameters

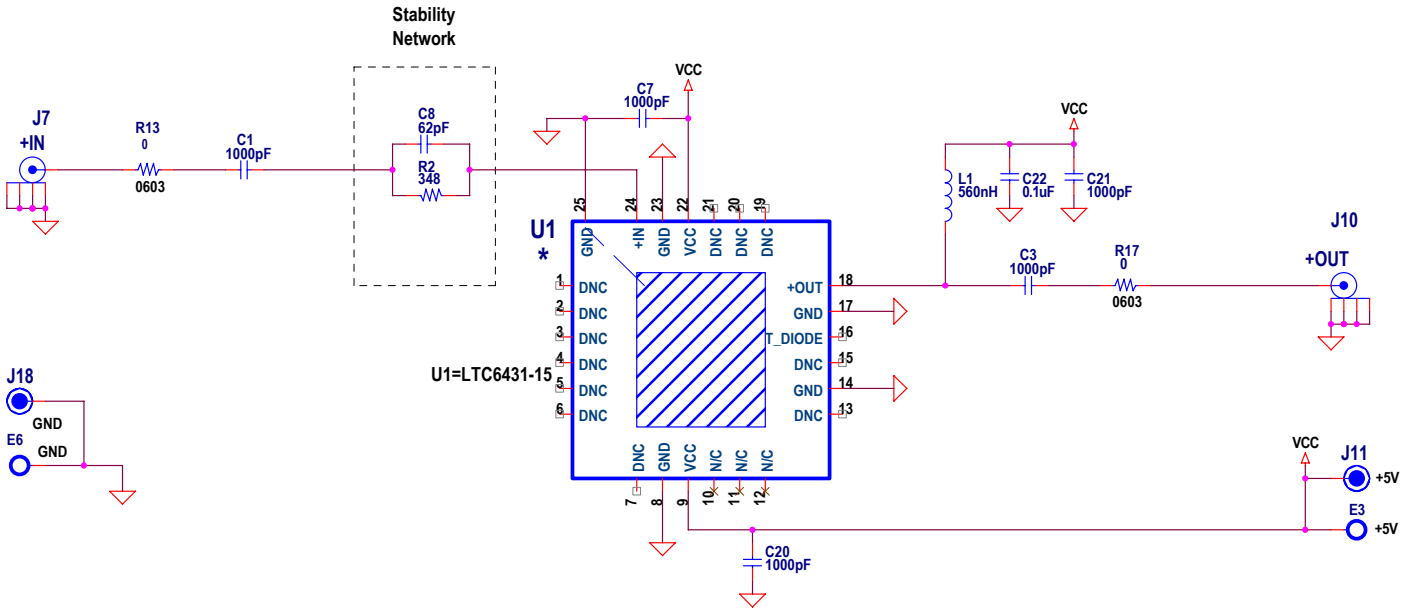

Figure 3. Simplified Demo Board DC1774A-C Schematic

OPERATION

The demo circuit 1774A-C is a high linearity fixed gain amplifier. It is designed for ease of use. Both the input and output are internally matched to 50Ω single-ended source and load impedance which is compatible with most test equipment. Figure 2 shows the demo board S-parameters.

Figure 3 shows the demo circuit schematic. It requires a minimum of passive support components. The input and output DC blocking capacitors (C1 and C3) are required because this device is internally biased for optimal operation. The frequency appropriate choke (L1) and the decoupling capacitors (C21 and C22) provide bias to the RF +OUT node. Only a single 5V supply is necessary for the V_{CC} pins on the device.

An optional input stability network has been added. It consists of a parallel 62pF (C8) and 348Ω (R2) input network has been added to insure low frequency stability.

Table 2 shows the function of each input and output on the board.

Table 2. DC1774A-C Board I/O Descriptions

CONNECTOR	FUNCTION
J7 (+IN)	Single-Ended Input. Impedance Matched to 50Ω. Drive from a 50Ω Network Analyzer or Signal Source.
J10 (+OUT)	Single-Ended Output. Impedance Matched to 50Ω. Drive from a 50Ω Network Analyzer or Spectrum Analyzer.
E3 or J11 (V_{CC})	Positive Supply Voltage Source.
E6 or J18 (GND)	Negative Supply Ground.

ADDITIONAL INFORMATION

The particular element values shown in the demo board schematic are chosen for wide bandwidth operation. Depending on the desired frequency, performance may be improved by the proper selection of these supporting components.

As with any RF device, minimizing ground inductance is critical. Care should be taken with the board layout because of these exposed pad packages. The maximum number of minimum diameter vias holes should be placed underneath the exposed pad. This will ensure good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and reduce inductance. It is a good idea to cover the via holes with solder mask on the back side of the PCB to prevent solder from wicking away from the critical PCB to the exposed pad interface.

The DC1774A-C is a wide bandwidth demo board but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements.

Figure 6 shows the generic PCB schematic for the LTC643X-YY amplifier series. The board can be modified for multiple demo board versions. For example, both DC1774A-A and DC1774A-B demo boards have a differential amplifier at U1; therefore, the board is using transformers to transform from differential to single-ended input and output. Likewise, the DC1774A-C is a single-ended demo board; consequently, it uses the LTC6431-15 for single-ended input and output.

Setup and Testing Signal Sources

The LTC6431-15 is an amplifier with high linearity performance, therefore output intermodulation products are very low. For this reason, it drives most test equipment and test setups to their limits. Consequently, accurate measurement of the third-order intercept point for a low distortion IC such as the LTC6431-15 requires certain precautions to be observed in the test setup and testing procedure.

Setup Signal Source

Figure 5 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined below:

1. High performance signal generators 1 and 2 (HP8644A) were used in the setup. These suggested generators have low harmonic distortion and very low phase noise.

ADDITIONAL INFORMATION

2. High linearity amplifiers to improve isolation. It prevents the two signal generators from crosstalking with each other and provides higher output power.
3. A lowpass filter to suppress the harmonic contents from interfering with the test signal.
4. The signal combiner from Mini-Circuits ADP-2-9 combines the two isolated input signals. This combiner has a typical isolation of 27dB. For better VSWR and isolation, use the H-9 signal combiner from MA/COM which features >40dB isolation and a wider frequency range. Passive devices (e.g., combiners) with magnetic elements can contribute no-linearity to the signal chain and should be used cautiously.
5. The attenuator pads on all three ports of the signal combiner will support further isolation of the two input signal sources. They will reduce reflection and promote maximum power transfer with wideband impedance matching.

Testing Signal Sources

The testing signal should be evaluated and optimized before it is used for measurements. The following outlines the necessary steps to achieve optimization:

a. Apply two independent signals f1 and f2 from signal generator 1 and signal generator 2 at 240MHz and 241MHz while setting amplitude = –13dBm per tone at the combined output.

b. Connect the combined signal directly to the spectrum analyzer (without the DUT).

c. Adjust the spectrum analyzer for the maximum possible resolution of the intermodulation products amplitude in dBc relative to the main tone power. A narrower resolution bandwidth will take a longer time to sweep. Optimize the dynamic range of the spectrum analyzer by adjusting input attenuation. First increase the spectrum analyzer input attenuation (normally in steps of 5dB or 10dB). If the IMD product levels decrease when the input attenuation is increased, then the input power level was too high for the spectrum analyzer to make a valid measurement. In other words, the spectrum analyzer 1st mixer was overloaded and producing its own IMD products. If the IMD reading holds constant with increased input attenuation, then a sufficient amount of attenuation was present. Adding too much attenuation will raise the noise floor and bury the intended IMD signal. Therefore, select just enough attenuation to achieve a stable and valid measurement.

d. In order to achieve a valid measurement result, the test system must have lower distortion than the DUT intermodulation. For example, to measure a +47dBm OIP3, the measured intermodulation products will be –90dBc below the –13dBm per tone input level and the test system must have Intermodulation products approximately –96dBc or better. For best results, the IMD or noise floor should be at least –100dBc before connecting the DUT.

Testing the DUT

At this point, the input level has been established at –13dBm per tone, and the input IMD from the test setup is well suppressed at –96dBm max. Furthermore, the spectrum analyzer is setup to measure very low level IMD components.

a. Insert the DUT and output attenuator into the setup, inline between the signal source and the spectrum analyzer. The output attenuator should match the DUT gain.

b. Fine tune the signal generator levels by a small amount if necessary (<1dB), to keep output power at +2dBm per tone at the amplifier output.

c. Measure the output IMD level using the same optimized setup as previous. Based on the output power level of +2dBm per tone, and knowing the IMD level, OIP3 can be calculated.

ADDITIONAL INFORMATION

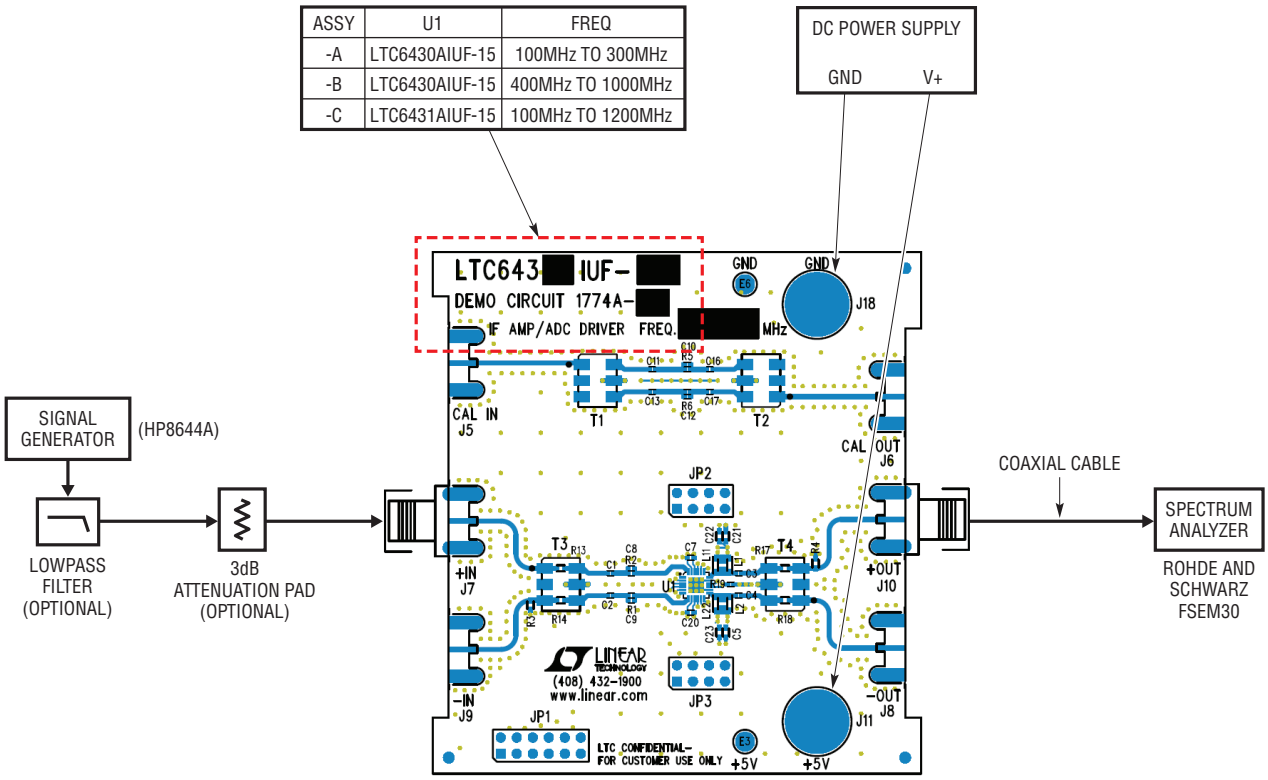

Figure 4. Proper Equipment Setup for Gain and Single-Tone Measurement

ADDITIONAL INFORMATION

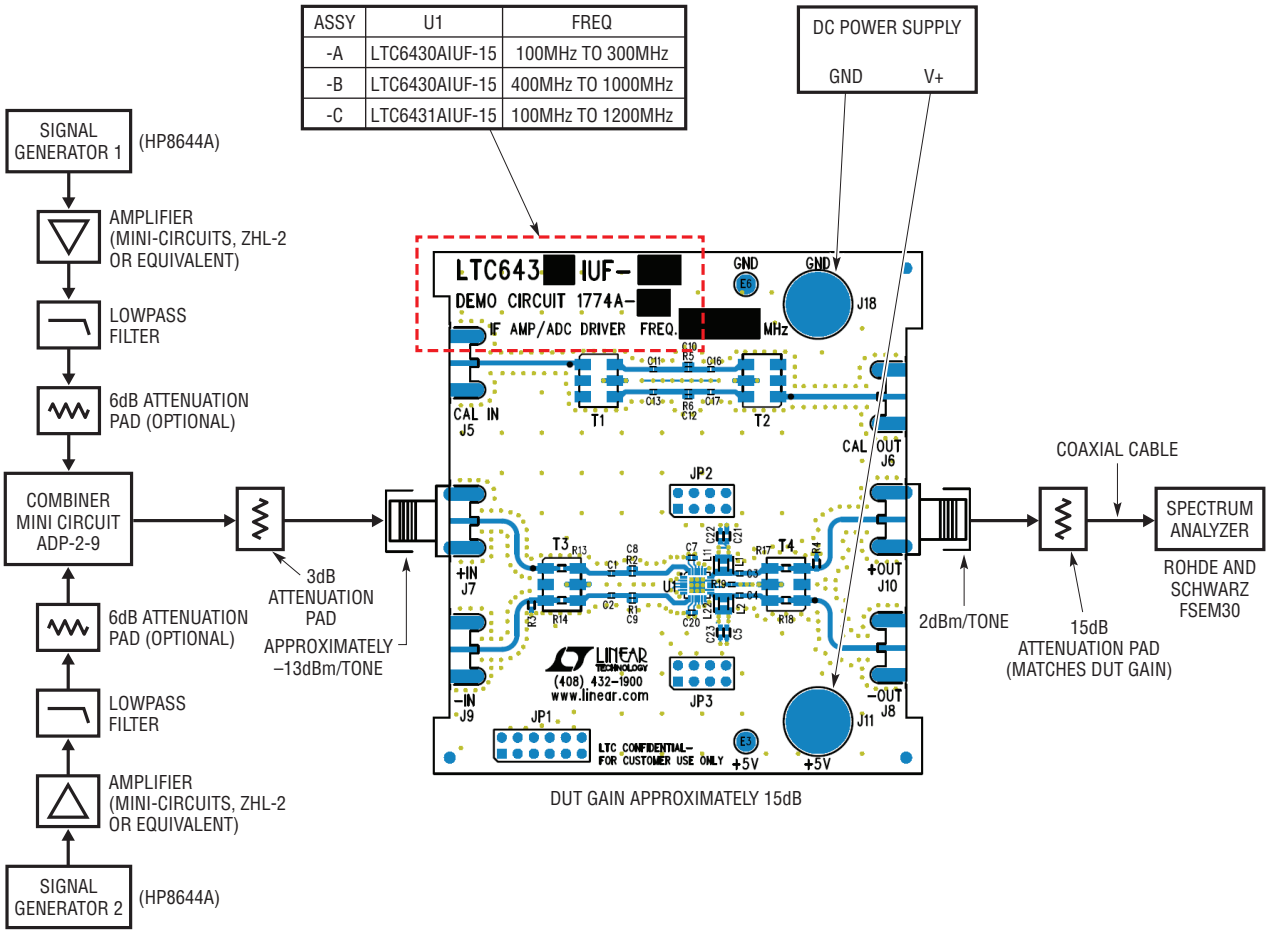

Figure 5. Proper Equipment Setup for IP3 Measurement

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1774A2 Required Circuit Components				
1	4	C1, C3, C7, C20	CAP., X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
2	1	C21	CAP., X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
3	1	C8	CAP., COG, 62pF, 16V 2%, 0402	AVX, 0402YA620GAT2A
4	0	C10, C12	CAP., COG, 62pF, 16V 2%, 0402	OPT
5	0	C11, C13, C16-C19	CAP., X7R, 1000pF, 5%, 0402	OPT
6	1	C22	CAP., X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
7	2	E3, E6	TESTPOINT, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
8	0	JP1	HEADER, 2X6, 0.1"	OPT
9	0	JP2, JP3	HEADER, 2X4, 0.1"	OPT
10	0	J5, J6	CONN., SMA 50Ω EDGE-MOUNTED	OPT
11	1	J7	CONN., SMA 50Ω EDGE-MOUNTED	JOHNSON, 142-0701-851
12	0	J9	CONN., SMA 50Ω EDGE-MOUNTED	OPT
13	2	J11, J18	JACK, BANANA	KEYSTONE, 575-4
14	1	L1	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
15	0	L11, L22	INDUCTOR, CHIP, 1008LS-2520	OPT
16	1	R2	RES., CHIP, 348Ω, 1%, 0402	YAGEO, RC0402FR-07348RL
17	0	R5, R6	RES., CHIP, 348Ω, 1%, 0402	OPT
18	0	R19	RES., CHIP, 0Ω, 5%, 0402	YAGEO, RC0402JR-070RL
DC1774A2-C Required Circuit Components				
1	1	DC1774A-2	GENERAL BOM	
2	0	C2, C4	CAP., X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
3	0	C5	CAP., X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
4	0	C9	CAP., COG, 62pF, 16V 2%, 0402	AVX, 0402YA620GAT2A
5	0	C14, C15	CAP., X7R, 1000pF, 25V 5%, 0402	AVX, 04023C102JAT2A
6	0	C23	CAP., X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
7	0	L2	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
8	0	J8	CONN., SMA 50Ω EDGE-MOUNTED	OPT
9	1	J10	CONN., SMA 50Ω EDGE-MOUNTED	JOHNSON, 142-0701-851
10	0	R1	RES., CHIP, 348Ω, 1%, 0402	YAGEO, RC0402FR-07348RL
11	0	R3, R4	RES., CHIP, 0Ω, 1/16W, 5%, 0603	OPT
12	4	R13, R14, R17, R18	RES., CHIP, 0Ω, 1/16W, 5%, 0603	YAGEO, RC0603JR-070RL
13	0	T1, T2	XFMR, MINI-CIRCUITS	OPT
14	0	T3, T4	XFMR, 2:1	OPT
15	1	U1	IC, IF AMP., QFN24UF-4X4	LINEAR TECH., LTC6431AIUF-15

SCHEMATIC DIAGRAM

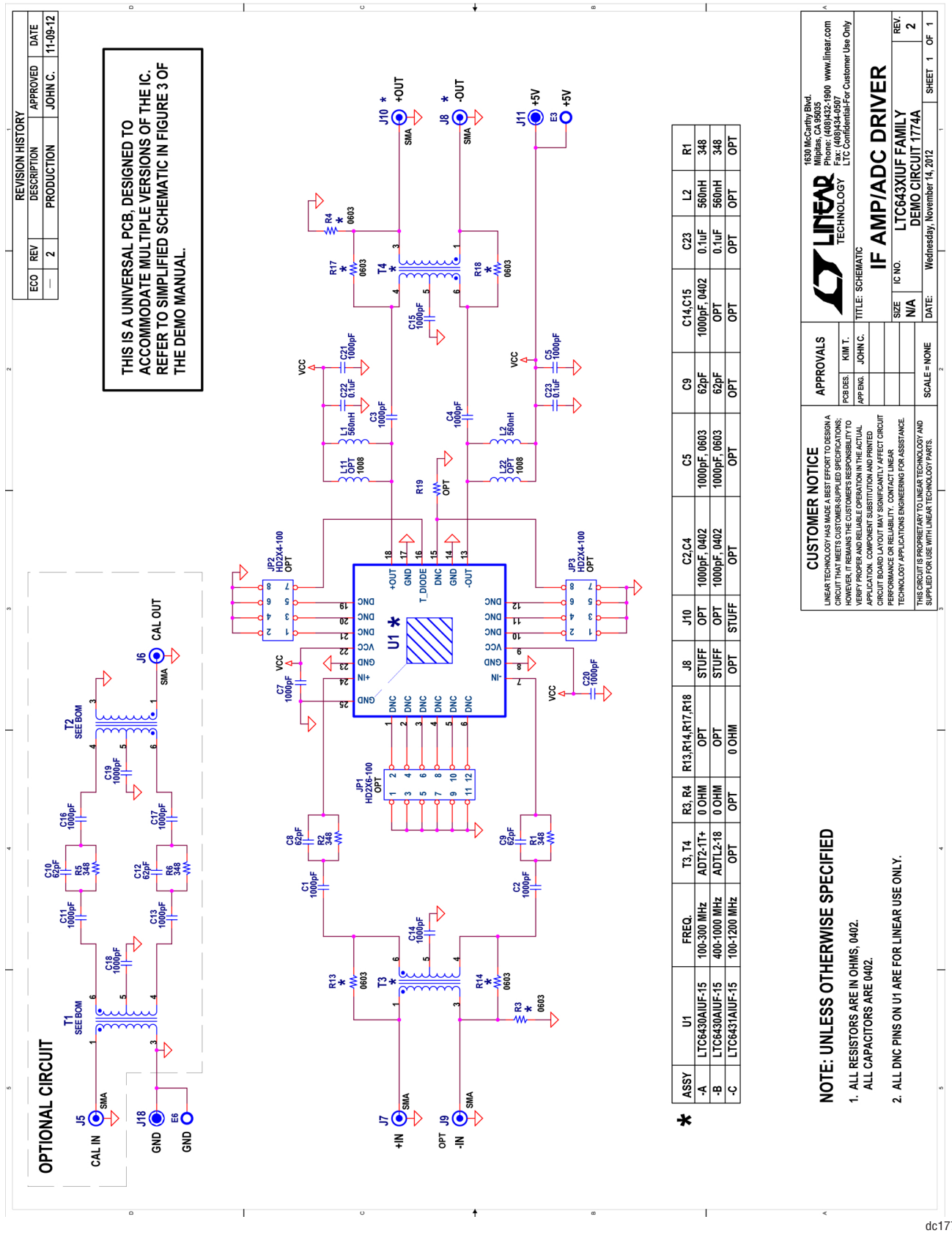

Figure 6. DC1774A RF/IF AMP/ADC Driver

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