



Power MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	500	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.52
Q <sub>g</sub> (Max.) (nC)	52	
Q <sub>gs</sub> (nC)	13	
Q <sub>gd</sub> (nC)	18	
Configuration	Single	

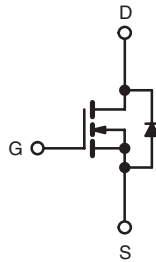
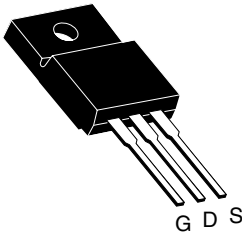
FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C<sub>oss</sub> Specified
- Compliant to RoHS directive 2002/95/EC



RoHS\* COMPLIANT

TO-220 FULLPAK



N-Channel MOSFET

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half and Full Bridge Convertors
- Power Factor Correction Boost

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB7N50APbF
	SiHFIB7N50A-E3
SnPb	IRFIB7N50A
	SiHFIB7N50A


ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>		500	V	
Gate-Source Voltage	V <sub>GS</sub>		± 30		
Continuous Drain Current <sup>f</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	6.6	A	
Continuous Drain Current			T <sub>C</sub> = 100 °C		4.2
Pulsed Drain Current <sup>a, e</sup>	I <sub>DM</sub>		44		
Linear Derating Factor			0.48	W/°C	
Single Pulse Avalanche Energy <sup>b, e</sup>	E <sub>AS</sub>		275	mJ	
Repetitive Avalanche Current <sup>a, e</sup>	I <sub>AR</sub>		11	A	
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>		6.0	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	60	W
Peak Diode Recovery dV/dt <sup>c, e</sup>	dV/dt		6.9	V/ns	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T<sub>J</sub> = 25 °C, L = 4.5 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 11 A (see fig. 12).
- I<sub>SD</sub> ≤ 11 A, di/dt ≤ 140 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.
- Uses IRFB11N50A, SiHFB11N50A data and test conditions.
- Drain current limited by maximum junction temperature.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

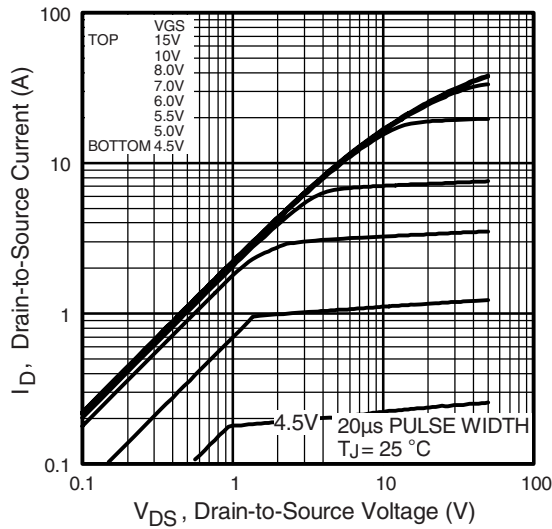
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	610	-	mV/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.0\text{ A}^b$	-	-	0.52	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.6\text{ A}^d$	6.1	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>d</sup>	-	1423	-	pF	
Output Capacitance	$C_{oss}$		-	208	-		
Reverse Transfer Capacitance	$C_{rss}$		-	8.1	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2000	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	55	-	
			$V_{DS} = 0\text{ V to } 400\text{ V}^{c, d}$	-	97	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b, d</sup>	-	-	52	nC
Gate-Source Charge	$Q_{gs}$			-	-	13	
Gate-Drain Charge	$Q_{gd}$			-	-	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 11\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 22\text{ }\Omega$ , see fig. 10 <sup>b, d</sup>	-	14	-	ns	
Rise Time	$t_r$		-	35	-		
Turn-Off Delay Time	$t_{d(off)}$		-	32	-		
Fall Time	$t_f$		-	28	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.6	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	44		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^{b, d}$	-	510	770	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.4	5.1	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

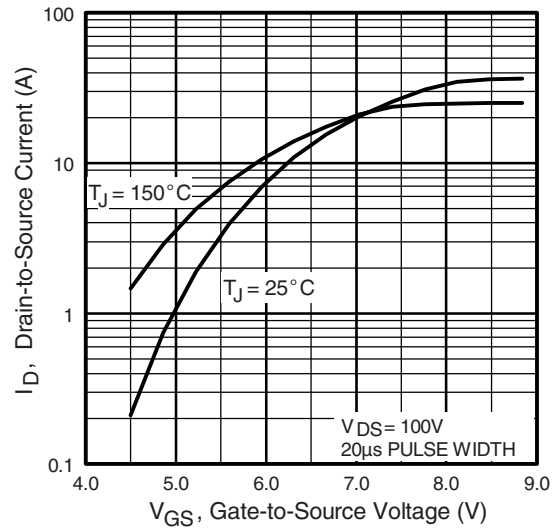
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0% to 80%  $V_{DS}$ .
- d. Uses IRFB11N50A, SiHF11N50A data and test conditions.

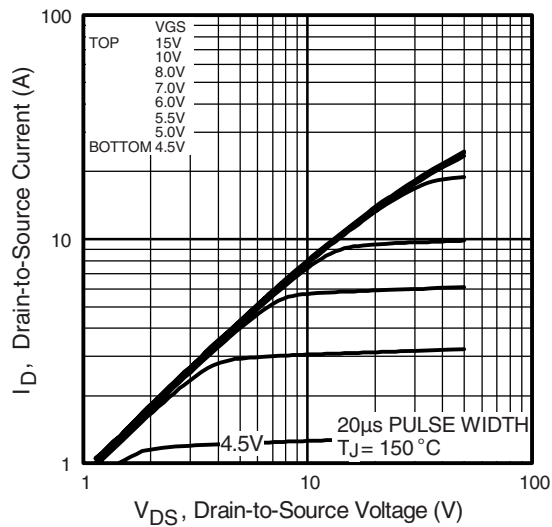
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



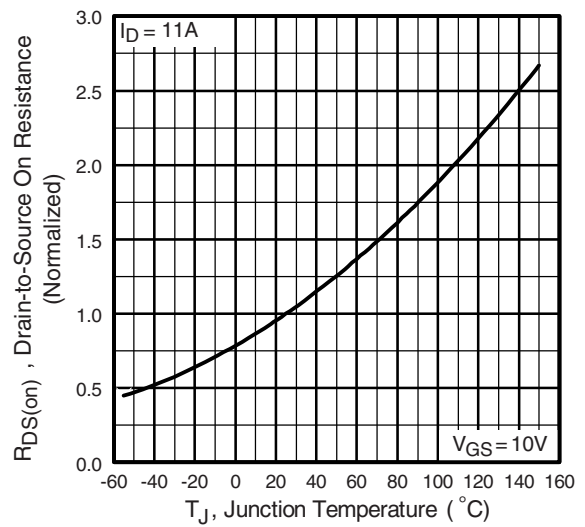
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

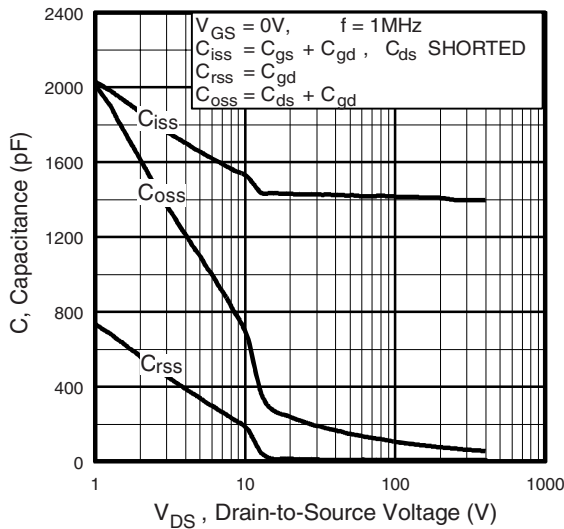


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

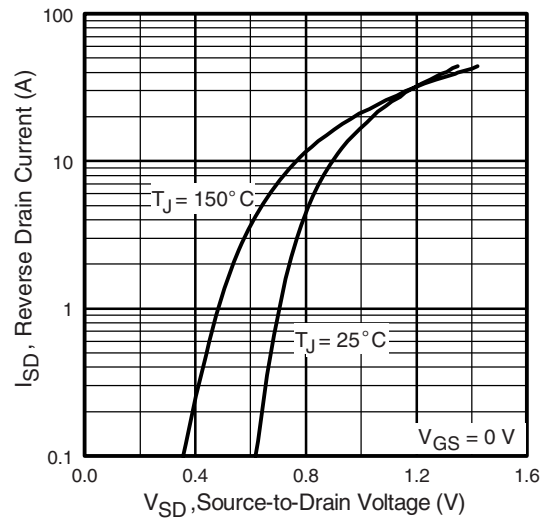


Fig. 7 - Typical Source-Drain Diode Forward Voltage

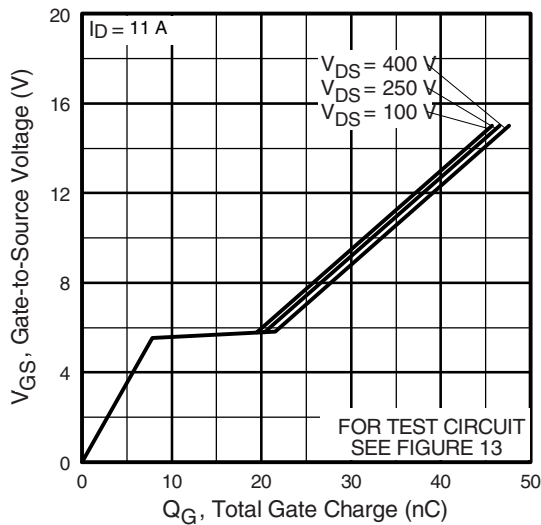


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

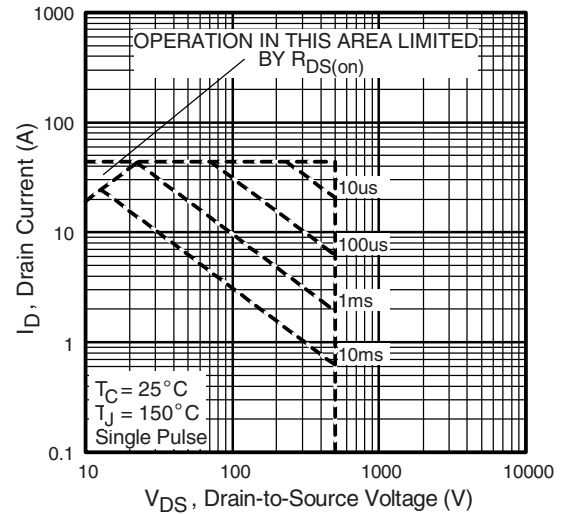


Fig. 8 - Maximum Safe Operating Area

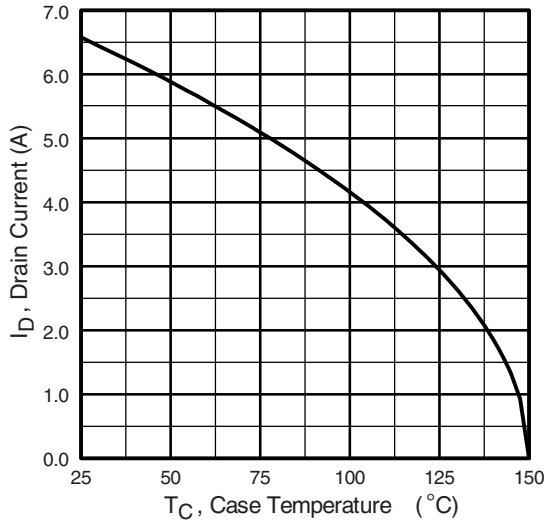


Fig. 9 - Maximum Drain Current vs. Case Temperature

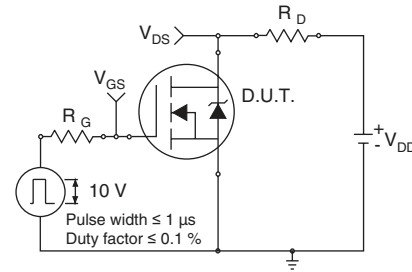


Fig. 10a - Switching Time Test Circuit

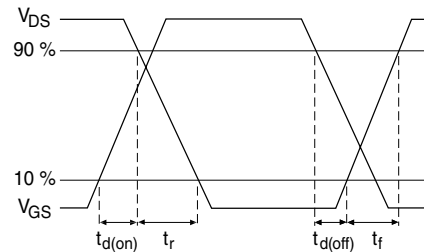


Fig. 10b - Switching Time Waveforms

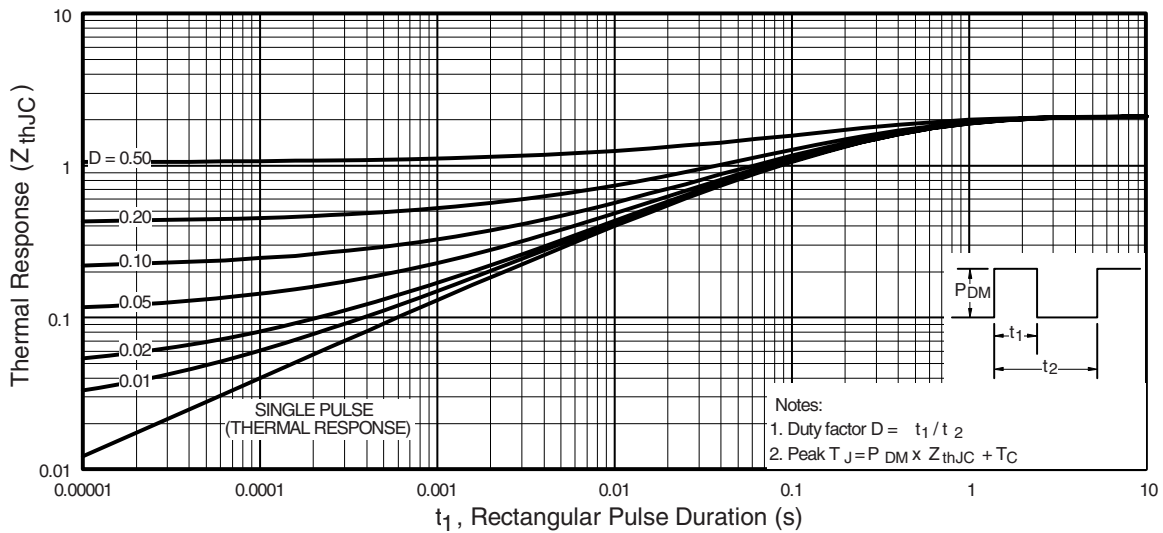


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

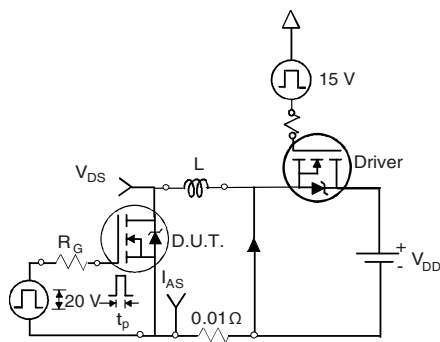


Fig. 12a - Unclamped Inductive Test Circuit

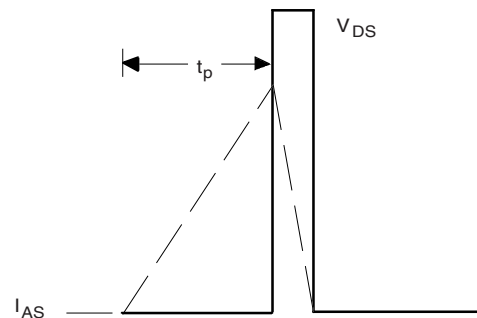
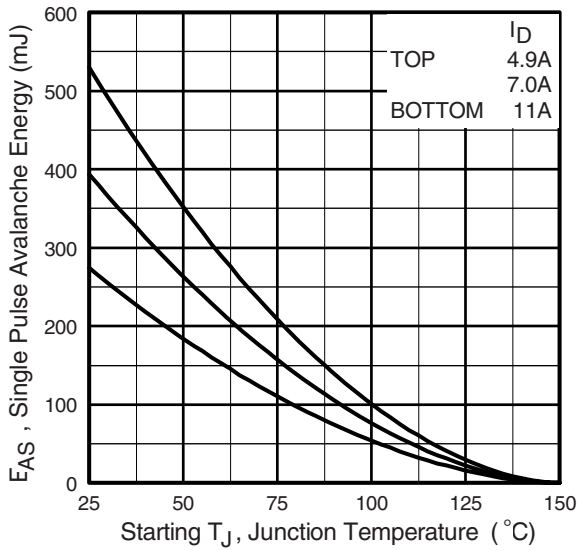
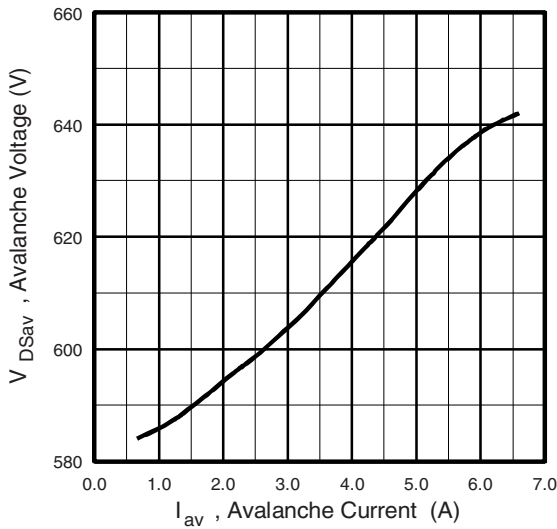


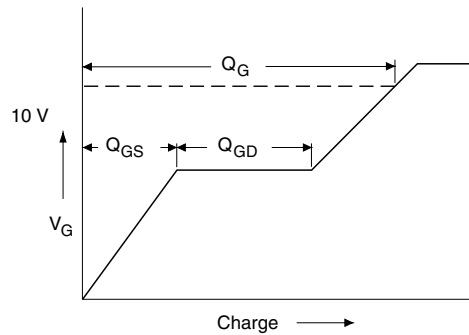
Fig. 12b - Unclamped Inductive Waveforms



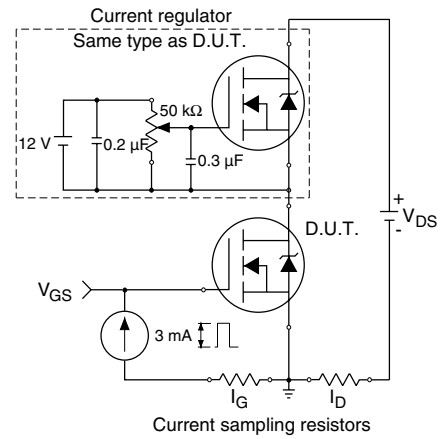
**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current**

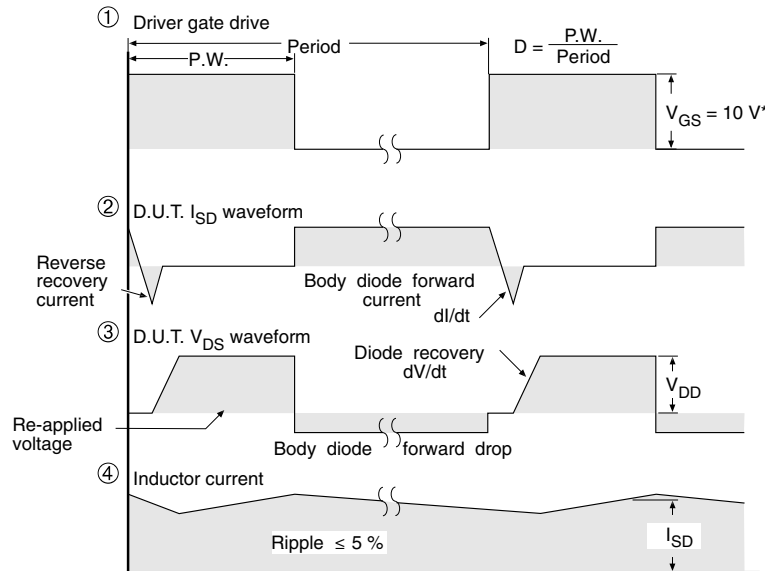
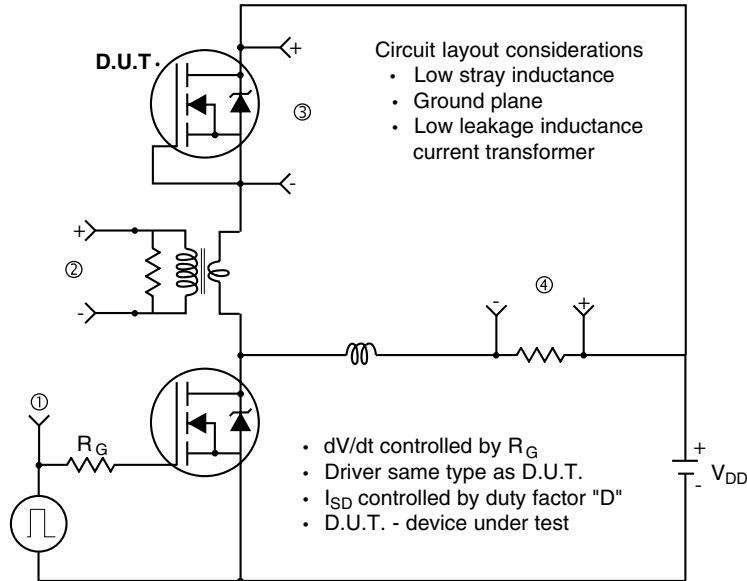


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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