FLAME

approved sheet

Model No : F101T50

Customer: _____

Version: _____

Date: 2012-02-17

CUSTOMER'S Accept APPROVAL&DATE:_____

CUSTOMER'S APPROVAL :

A.Configuration: ☐ **OK** ☐**NG**

B.Function: ☐ **OK** ☐**NG**

C.Standard for product check: ☐ **OK** ☐**NG**

D.Other: ☐ **OK** ☐**NG**

CUSTOMER'S SIGNATURE &DATE:_____

For MJK's improve,please tick or explain it(them) as belows while on debugging on our products:

☐A. price away from our target:_____

☐B. other supply's debugging success:_____

☐C. Sample period away from our target:_____

☐D. Project cancel :_____

☐E. NO need to test for solution change:_____

☐F. Other:_____

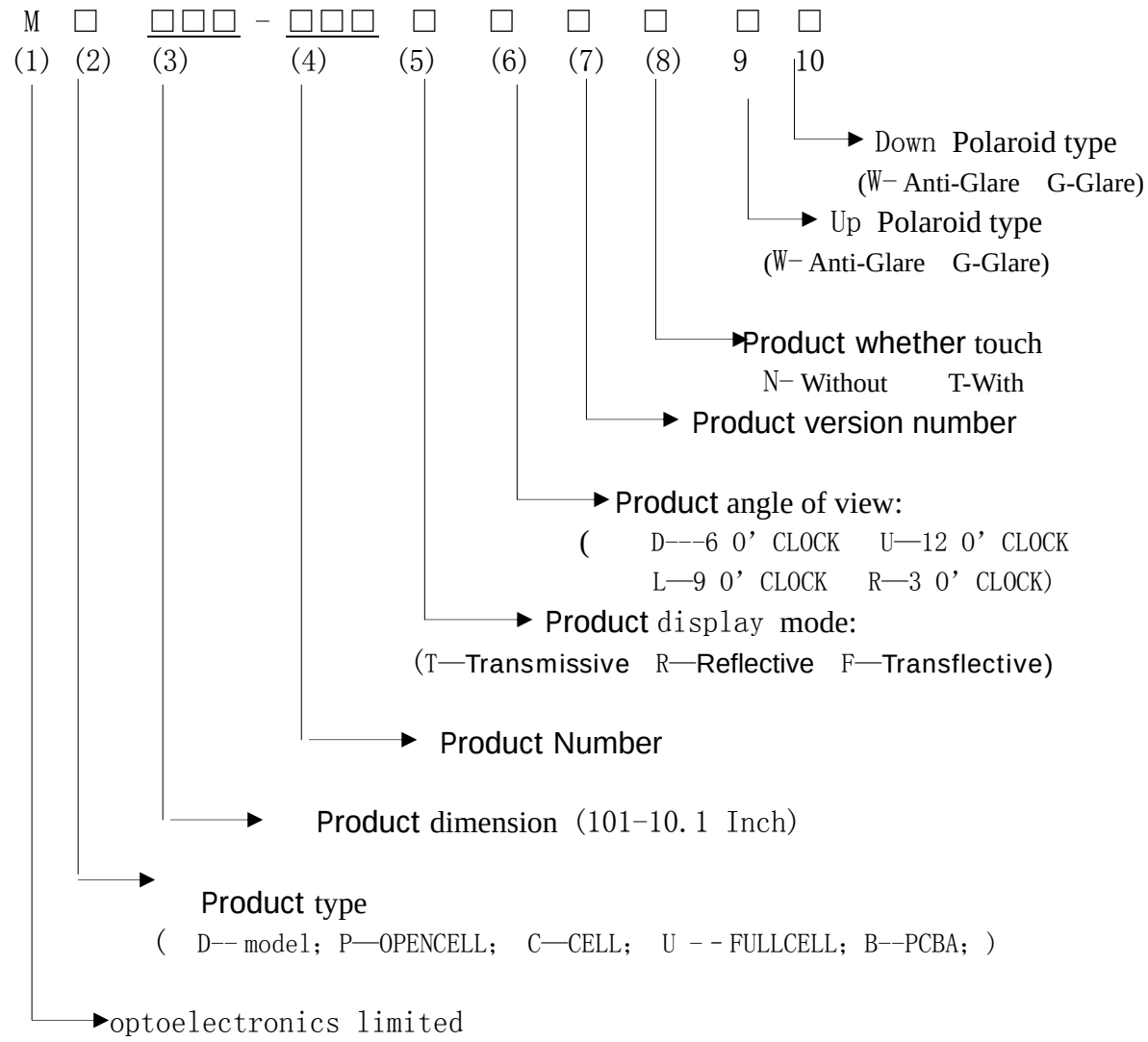
Product Specification

Product	Standard LCD Module 1024(RGB) x 600Dots graphic type 10.1”TFT 16.2M Transmissive LCD COG bonding type Wide temperature LED back light Without Touch Panel 50PIN 24Bits TTL interface

变更记录

日期	版本	修改页码	变更前描述	变更后描述	备注

Product Model description



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1. Summary

This technical specification applies to 10.1" color TFT-LCD is a color active matrix thin film transistor (TFT) liquid crystal display(LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 10.1-inch diagonally measured active display area with WSVGA resolution (1024 vertical by 600 horizontal pixel array)

2. Features

- **10.1" WSVGA TFT LCD Panel**
- **LED Light-bar Backlight System(9 Parallel 3 Serial)**
- **Supported WSVGA (V:1024 lines, H:600 pixels) Resolution**
- **DualGate(1 Source + 1Gate)**

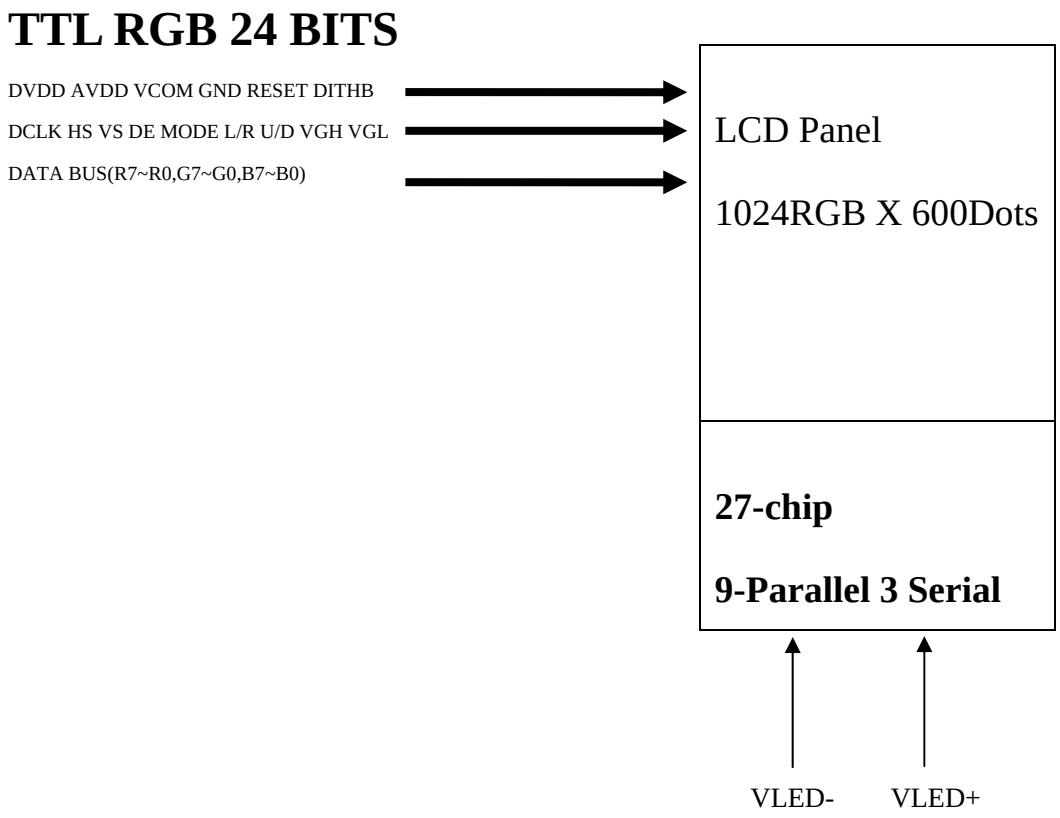
3.General Specifications

NO	Item	Contents	Contents	Unit
(1)	Module Outsize(mm)	235.00 x 143.00 x 5.40(Max.)		mm
(2)	LCD Active area(mm)	222.72(H) x 125.28(V)		mm
(3)	Display resolution(dot)	1024(x3) x 600		dot
(4)	Screen size(inch)	10.1		Inch
(5)	Dot pitch(mm)	0.2175(H) x 0.2088(V)		mm
(6)	Color configuration	R.G. B vertical stripe		-
(7)	Support color	16.2M		-
(8)	Display Mode	Normally White(TN)		-
(9)	Gray Scale inversion	6 o'clock		-
(10)	LCD type	a-si TFT		-
(11)	Electrical Interface(Logic)	50PIN 24Bits TTL interface		-
(12)	Weight	TBD		g
(13)	Panel surface treatment	Glare	MD101-056TDANGG	-- --
(14)	White Luminance	200 (Typ.)	5 points average	Cd/m2
(15)	Contrast Ratio	600 (Typ.)		
(16)	Input Voltage(V)	+3.3 (Typ.)	Logic Voltage	V
(17)	Power Consumption(W)	TBD	Logic system	watt

4.Function Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block diagram



5.Absolute Maximum Ratings

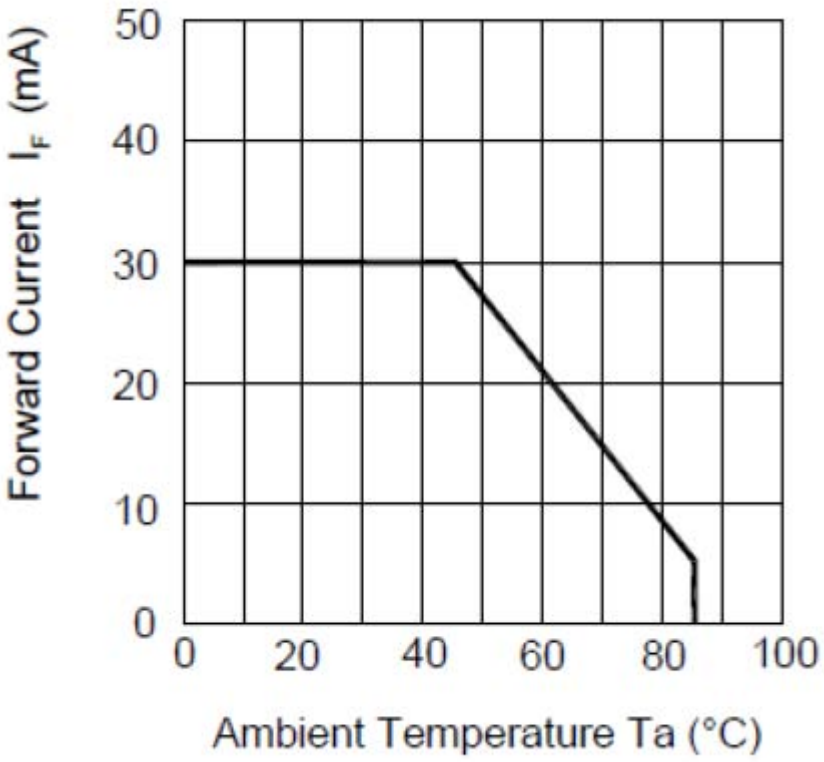
Item	Symbol	Min	Max	Unit	Condition
Digital Supply Voltage	VDD	-0.3	4	V	
Analog Supply Voltage	AVDD	-0.5	15	V	
Gate On Voltage	VGH	-0.3	42	v	
Gate Off Voltage	VGL	-20	0.3	V	
Logic Signal Input Level	VI	-0.3	VDD+0.3	V	
Forward Current （per LED）	If	--	30	mA	
Reverse Voltage（per LED）	VR	--	5	V	
Pulse forward current（per LED）	Ifp	--	100	mA	Note 1、2

Note:

Note1：Ifp Conditions ： Pulse Width ≦10msec；Duty ≦1/10

Note2：perating must under the condition as below drawing.

(Ambient Temperature /Allowable Forward Current) Each LED .



6.Electrical Characteristics

6.1 TFT LCD

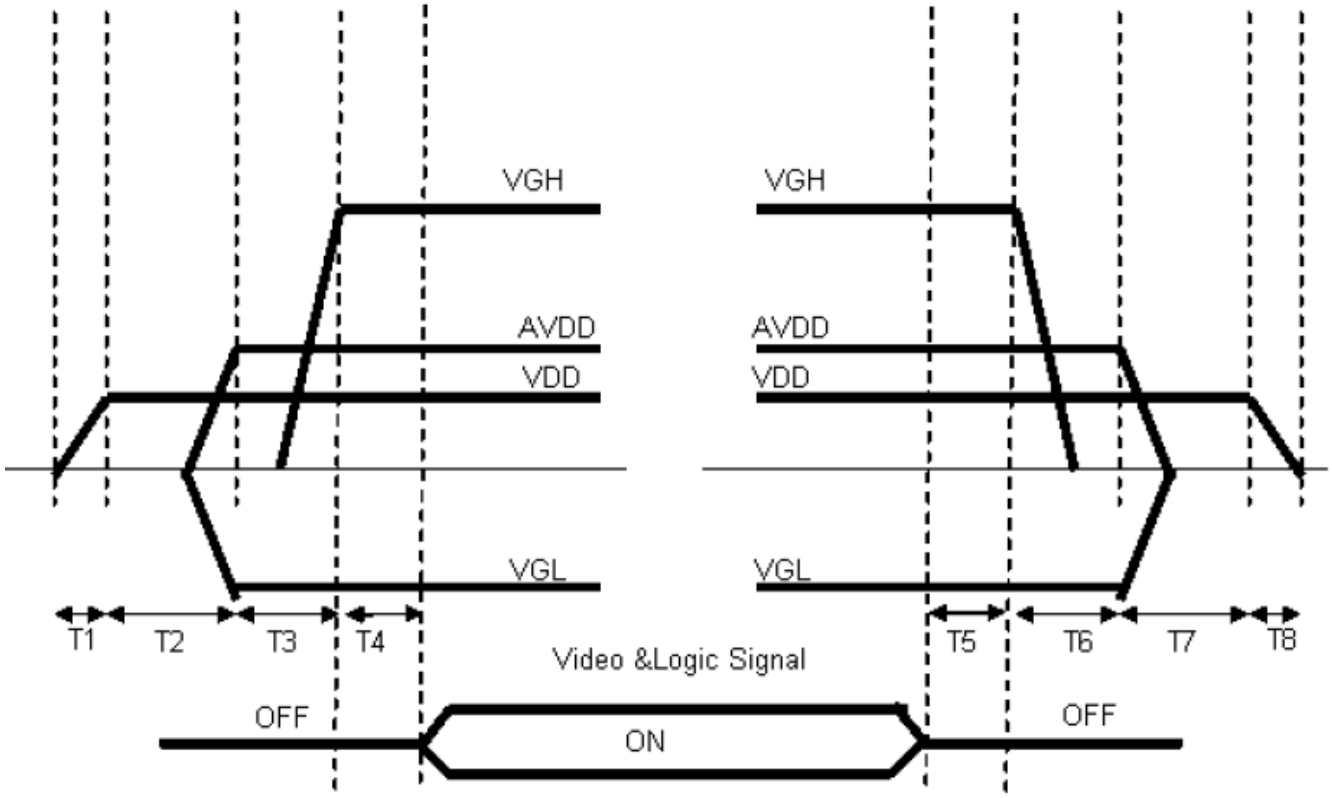
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	VDD	3	3.3	3.6	V	
VDD Current	IDD	--	150	--	mA	
Logic Signal Input Level	ViH	0.7 Vcc	-	VCC	V	
	ViL	0	-	0.3 Vcc	V	
Analog Power Supply Voltage	AVDD	TBF	10.85	TBD	V	
Gate On Power Supply Voltage	VGH	18	19	20	V	
Gate Off Power Supply Voltage	VGL	-9	-8	-7	V	
Common Power Supply Voltage	VCOM	2.2	3.2	4.2	V	

Note:

1. Please adjust VCOM to make the flicker level be minimum.

6.2 Power、Signal sequence

Power On：VDD→AVDD/VGL →VGH →Video &Logic Signal
Power Off：Video &Logic Signal→ VGH→AVDD/VGL→VDD



$0 < T1 \leqq 10ms$
$20ms < T2$
$10ms < T3$
$0 < T4 \leqq 10ms$

$0 < T5 \leqq 10ms$
$0 < T6$
$0 < T7$
$0 < T8$

6.3 Backlight

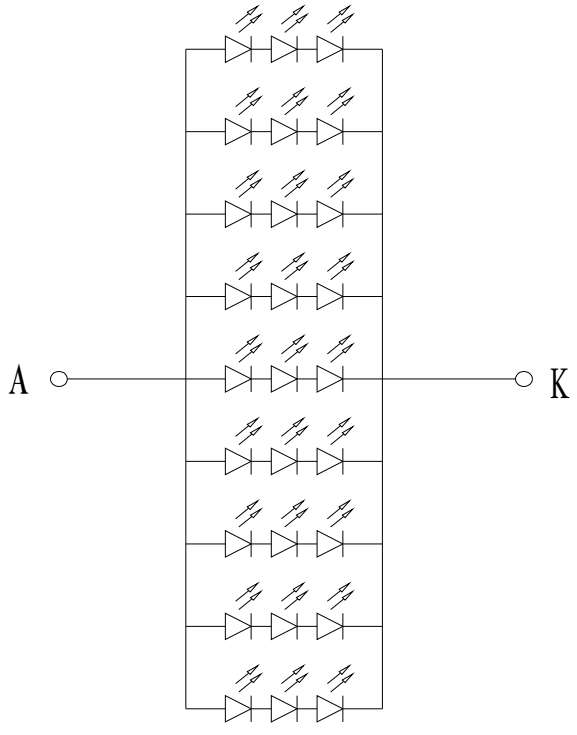
Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
VF	(BL+) - (BL-)	9	9.6	10	V	Ta=25℃
IF	LED Current	-	180	-	mA	Ta=25℃
PLED	LED Power Consumption	--	2.5	--	W	Ta=25℃
LT	LED Life Time	10000	-	-	Hours	Ta=25℃ Note C

Note：

A: The LED life time define as the estimated time to 50% degradation of initial luminous.

B: Calculator value for reference PLED =VF(normal Distribution) x IF (Normal Distribution) / Efficiency

C: LED Circuit Diagram

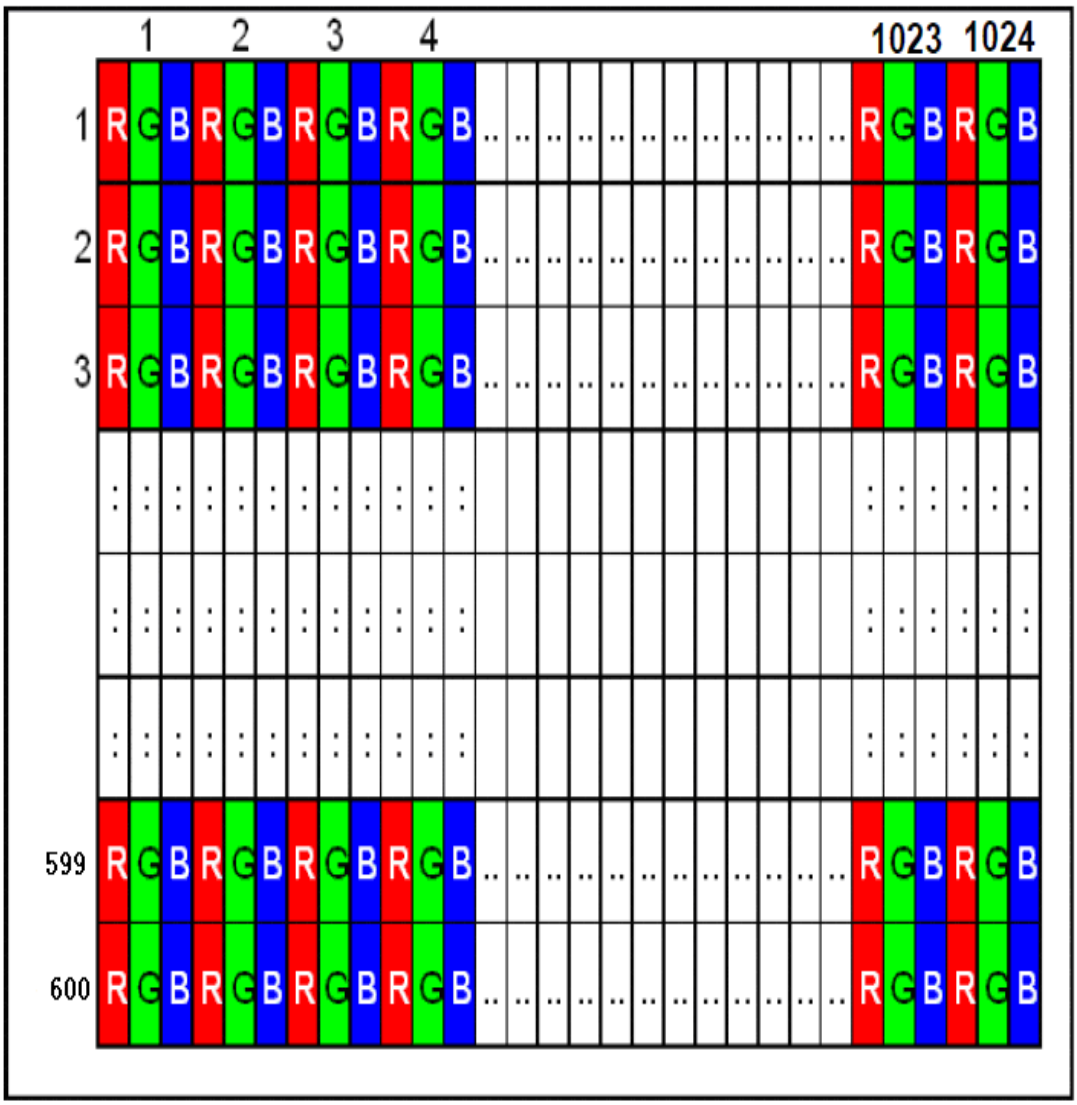


D: Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.

7.Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



8.Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 2 Optical Characteristics

Item	Conditions		Specification			
			Min.	Typ.	Max.	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	--	70	-	A,B
		Right	--	70	-	
	Vertical	Up	--	60	-	
		Down	--	70	-	
Contrast ratio	Center		--	600	--	A,C
Response Time [ms]	Rising + Falling		-	3+5	16	A,D
Color Chromaticity (CIE1931)	Red x		0.58	0.63	0.68	A,
	Red y		0.26	0.31	0.36	A,
	Green x		0.224	0.295	0.344	A,
	Green y		0.468	0.518	0.568	A,
	Blue x		0.093	0.143	0.193	A,
	Blue y		0.101	0.153	0.201	A,
	White x		0.245	0.295	0.345	A,
	White y		0.281	0.331	0.381	A,
White Luminance [cd/m^2]	I-LED=20.0mA		-	200	-	5point A, E
Luminance Uniformity [%]	I-LED=20.0mA 13points		-	-	-	A, F
	I-LED=20.0mA 5points		80	-	-	

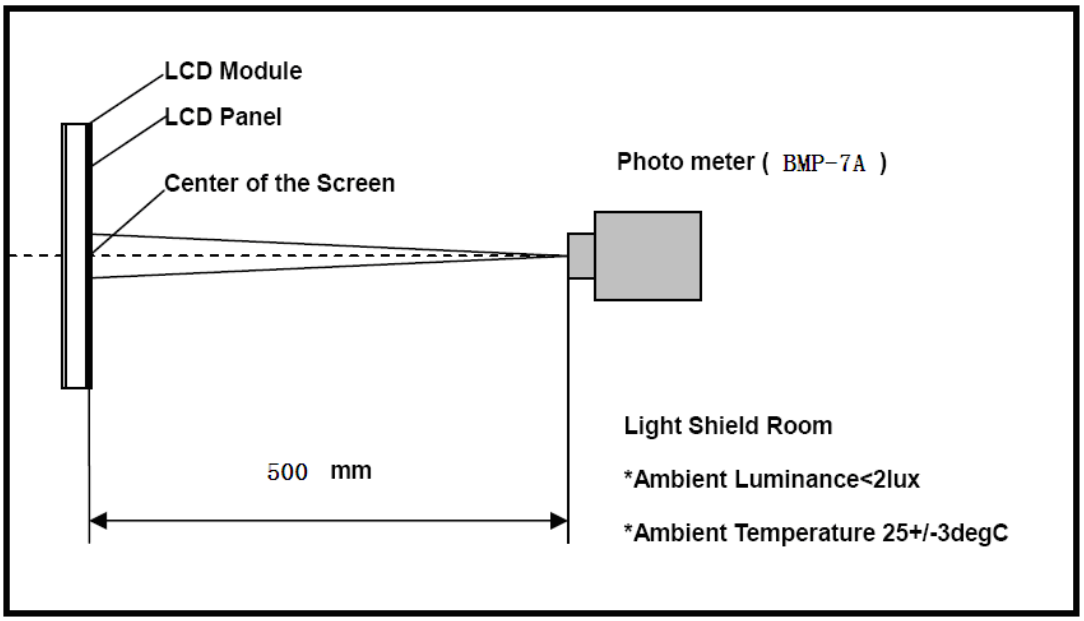
（Note: Backlight is M-BL-101-009V0）

Note:

A. Measurement Setup

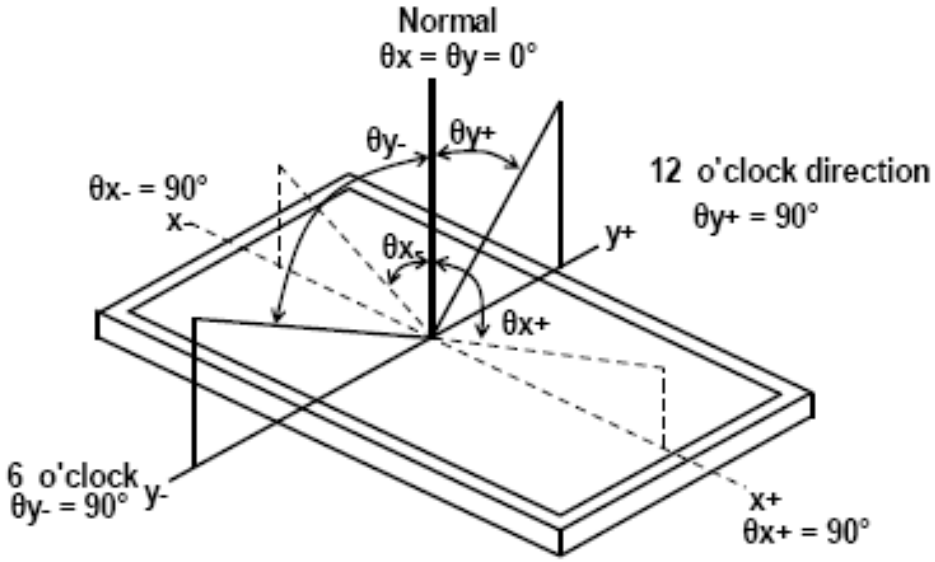
The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 3 Measurement Setup



B. Definition of Viewing Angle

Figure 4 Definition of Viewing Angle



C. Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

D. Definition of Response Time (TR, TF)

Figure 5 Definition of Response Time

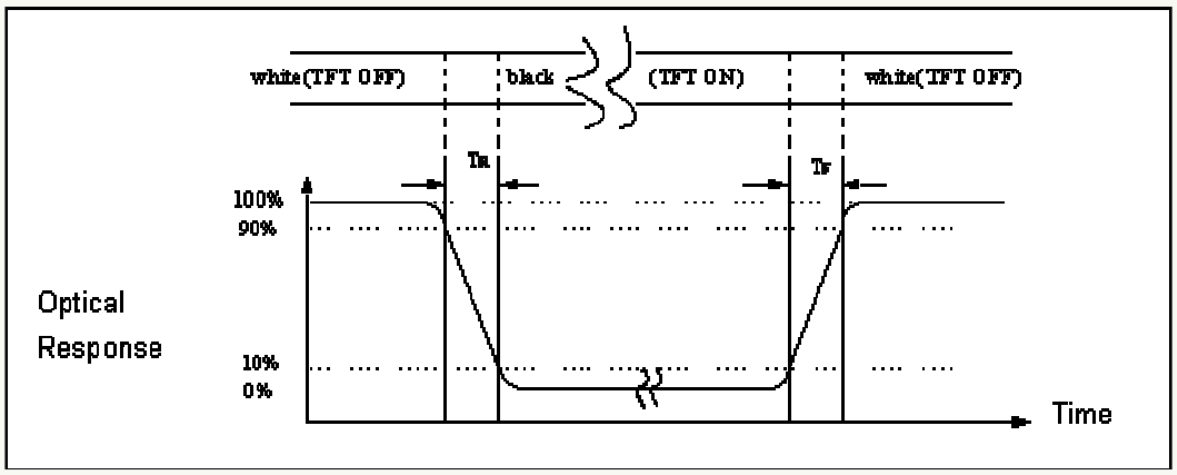
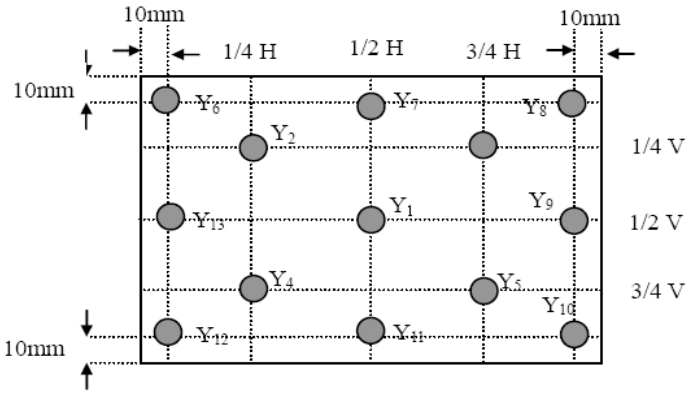


Figure 6 Measurement Locations of 13 Points



E. Definition of Luminance White

Measure the luminance of gray level 63 at center point and 5 points.

Center of Luminance = Y1

Average Luminance of 5 points = (Y1 + Y2 + Y3 + Y4 + Y5)/5

F. Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 63 at 13 points.

$$\text{Uniformity of 13 points} = \frac{\text{Min Luminance of Y1~Y13}}{\text{Max Luminance of Y1~Y13}} \times 100\%$$

$$\text{Uniformity of 5 points} = \frac{\text{Min Luminance of Y1~Y5}}{\text{Max Luminance of Y1~Y5}} \times 100\%$$

9.Interface Characteristics

9.1 CN1 (Input Signal)

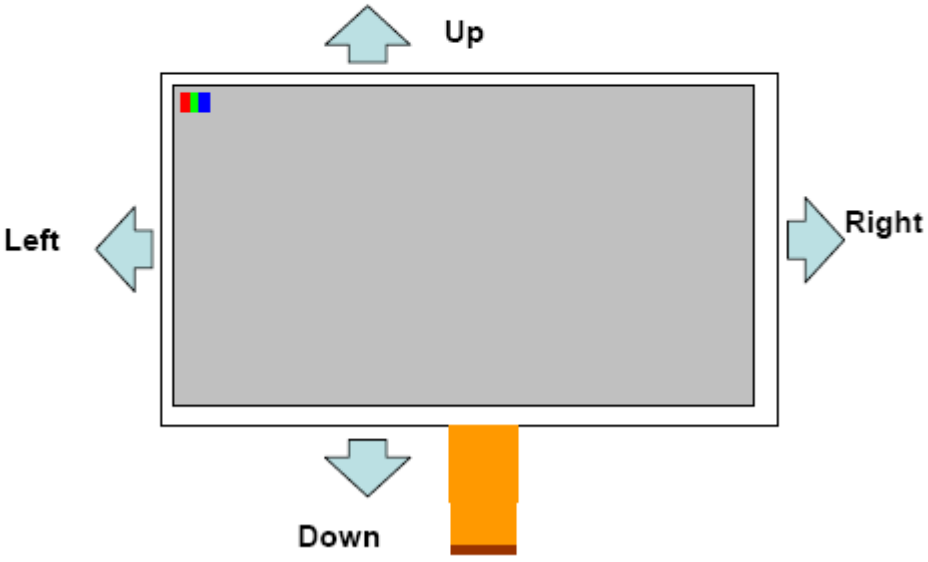
PIN NO	SYMBOL	DESCRIPTION	REMARK
1	NC	No connect	
2	NC	No connect	
3	NC	No connect	
4	NC	No connect	
5	GND	Digital ground	
6	VCOM	Common voltage	
7	VDD	Digital Power	
8	MODE	DE/HV SYNC mode select H: DE L: HV	
9	DE	Data Input Enable	
10	VSD	Vertical Sync Input	
11	HSD	Horizontal Sync Input	
12	B7	Blue data	
13	B6	Blue data	
14	B5	Blue data	
15	B4	Blue data	
16	B3	Blue data	
17	B2	Blue data	
18	B1	Blue data	
19	B0	Blue data	
20	G7	Green data	
21	G6	Green data	
22	5G	Green data	
23	G 4	Green data	
24	G3	Green data	
25	G2	Green data	
26	G1	Green data	
27	G0	Green data	
28	R7	Red data	
29	R6	Red data	
30	R5	Red data	
31	R4	Red data	
32	R3	Red data	
33	R2	Red data	
34	R1	Red data	
35	R0	Red data	
36	GND	Digital ground	

37	DCLK	Clock input	
38	GND	Digital ground	
39	L/R	Left or Right Display Comtrol	
40	U/D	Up or Down Display Comtrol	
41	VGH	Positive power for TFT	
42	VGL	Negative power for TFT	
43	AVDD	Analog power	
44	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit Normally pull high. (R=10KΩ， C=0.1μF)	
45	NC	No connect	
46	VCOM	Common voltage	
47	DITHB	Dithering function enable control. Normally pull low DITHER = “1”, Enable internal dithering function DITHER = “0”, Disable internal dithering function	
48	GND	Digital ground	
49	NC	No connect	
50	NC	No connect **(IBST，Reserve for MJK test)**	**Customer must be open**

Remarks：

1) UPDN and SHLR control function

UPDN	SHLR	FUNCTION
0	1	Normal display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down



9.2 CN2 (LED backlight)

PIN NO	SYMBOL	FUNCTION
1	A	Anode
2	K	Cathode

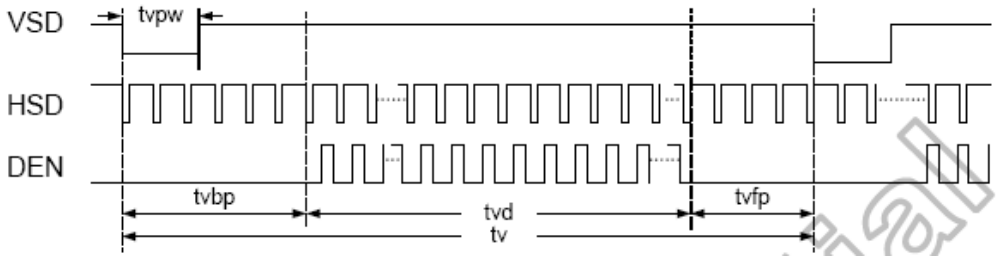
10.Interface Timings

10.1 TTL mode AC electrical characteristics

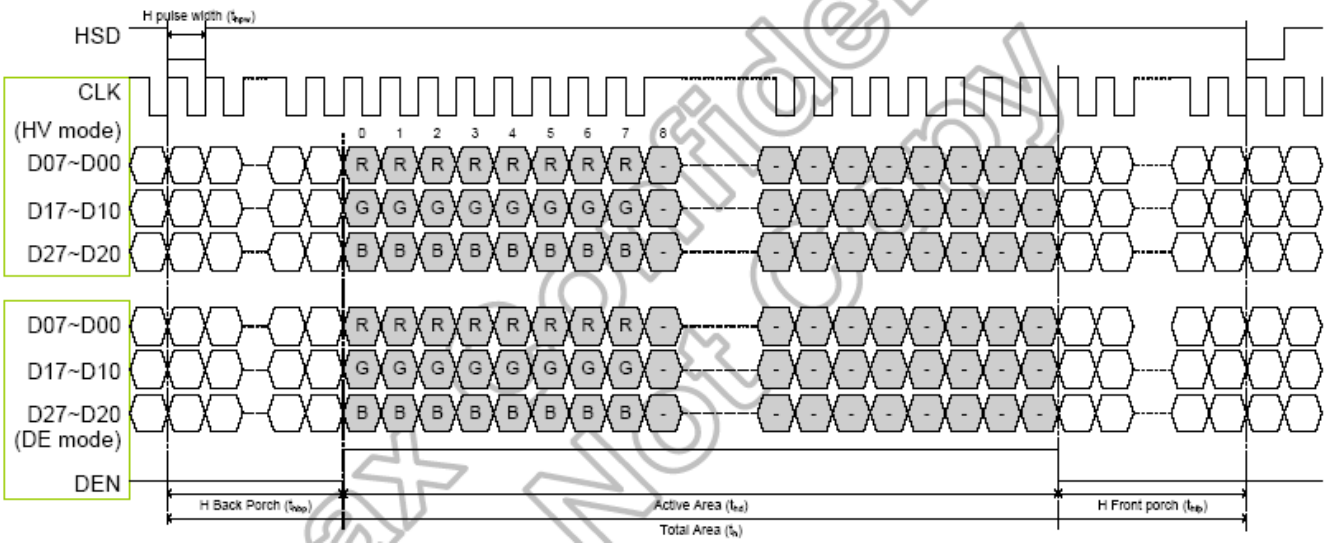
Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VDD Power On Slew rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB pulse width	T_{GRB}	50	-	-	μs	DCLK=65MHz
DCLK cycle time	T_{cph}	14	-	-	ns	-
DCLK pulse duty	T_{cwh}	40	50	60	%	-
VSD setup time	T_{vst}	5	-	-	ns	-
VSD hold time	T_{vhd}	5	-	-	ns	-
HSD setup time	T_{hst}	5	-	-	ns	-
HSD hold time	T_{hhd}	5	-	-	ns	-
Data set-up time	T_{dsu}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	T_{dhd}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	T_{esu}	5	-	-	ns	-
DE hold time	T_{ehd}	5	-	-	ns	-
Output stable time	T_{sst}	-	-	6	μs	10% to 90% target voltage. CL=90pF, R=10K ohm (Cascade)
				3		Dual gate

10.2 TTL mode data input format

Vertical timing



Horizontal timing



9.5 Parallel RGB input timing table: Resolution：1024x600

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd		600		T_H
VSD Period	tv	610	635	800	T_H
VSD Blanking	tvbp+ tvfp	10	35	200	T_H

Table 10.4: DE mode (1024x600)

- **HV mode**

Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp		160		DCLK
HSD Front Porch	thfp	16	160	216	DCLK

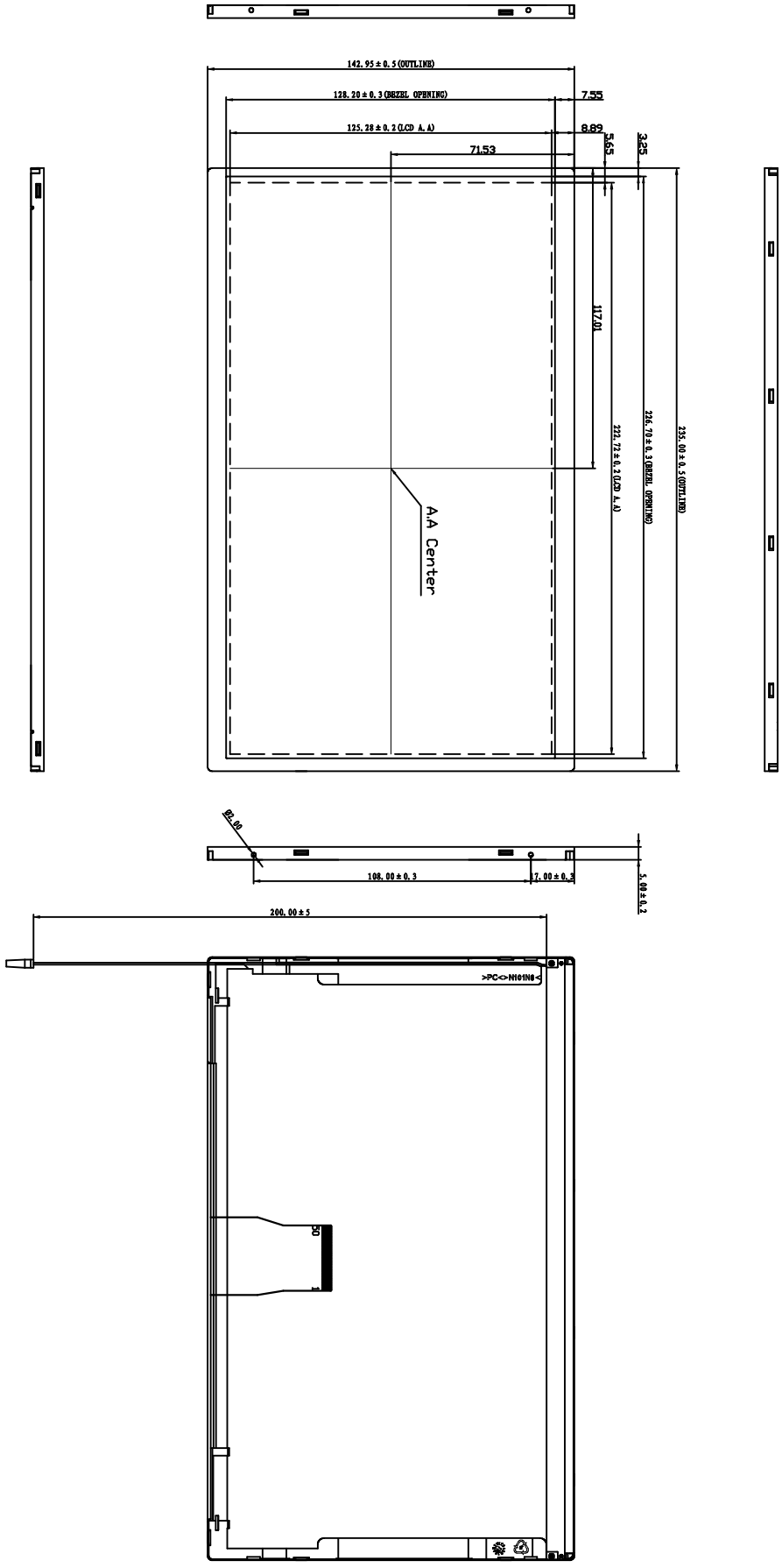
Table 10.5: HV mode horizontal timing (1024x600)

Vertical Timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		T_H
VSD Period	tv	624	635	750	T_H
VSD Pulse Width	tvpw	1	-	20	T_H
VSD Back Porch	tvbp		23		T_H
VSD Front Porch	tvfp	1	12	127	T_H

Table 10.6: HV Mode Vertical Timing (1024x600)

11.Mechanical Characteristics



TOLERANCE	.X	± 0.1	SCALE	N.T.S		
	.XX	±	UNITS	mm		
	∠	± 1°	MATERIAL			
APPROVED	CHK BY	DRG BY	DRG DATE			
P/N	DWG NO	TITLE:	MODEL:			
VER. 01	P 1 OF 1					

12.Package

TBD