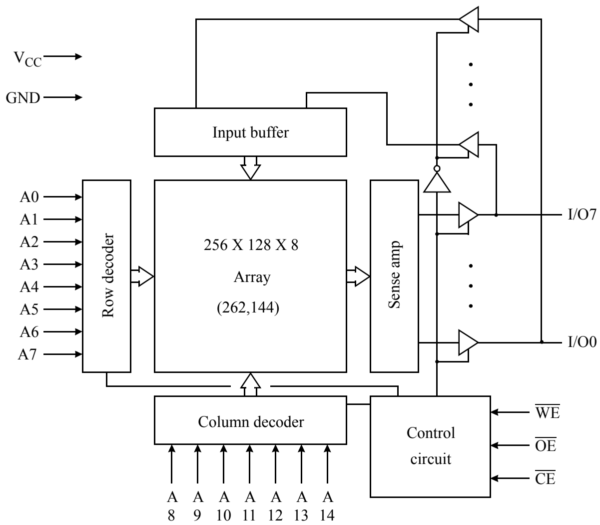
3.3V 32K X 8 CMOS SRAM (Common I/O)

Features

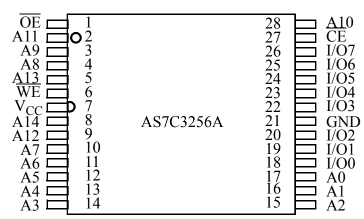
- Pin compatible with AS7C3256
- Industrial and commercial temperature options
- Organization: 32,768 words × 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 5, 6, 7, 8 ns output enable access time
- Very low power consumption: ACTIVE
  - 180mW max @ 10 ns
- Very low power consumption: STANDBY
  - 7.2 mW max CMOS I/O
- Easy memory expansion with CE and OE inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
  - 300 mil SOJ
  - 8 × 13.4 mm TSOP 1
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram

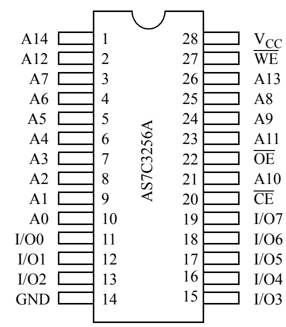


Pin arrangement

28-pin TSOP 1 (8×13.4 mm)



28-pin SOJ (300 mil)



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	50	45	40	35	mA
Maximum CMOS standby current	2	2	2	2	mA

Functional description

The AS7C3256A is a 3.3V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words × 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters *standby mode* when $\overline{CE}$ is high. CMOS standby mode consumes 7.2 mW. Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5, 6, 7, 8 ns are ideal for high-performance applications. The chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible. Operation is from a single 3.3 ±0.3V supply. The AS7C3256A is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.5	+5.0	V
Voltage on any pin relative to GND	V_{t2}	–0.5	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = Don't care, L = Low, H = High

Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage		V_{CC}	3.0	3.3	3.6	V
Input voltage		V_{IH}**	2.0	–	V_{CC}+0.5	V
		V_{IL}*	-0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

* V_{IL} min = –1.0V for pulse width less than 5ns.
** V_{IH} max = V_{CC} + 2.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range)[1]

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	V_{CC} = Max, V_{OUT} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE} \le V_{IL}$ f = f_{Max}, I_{OUT} = 0mA	–	50	–	45	–	40	–	35	mA
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE} \ge V_{IH}$ f = f_{Max}	–	20	–	20	–	20	–	20	mA
	I_{SB1}	V_{CC} = Max, $\overline{CE} \ge V_{CC}$–0.2V $V_{IN} \le$ 0.2V or $V_{IN} \ge V_{CC}$–0.2V, f = 0	–	2.0	–	2.0	–	2.0	–	2.0	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V

Capacitance (f = 1MHz, T_a = room temperature, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

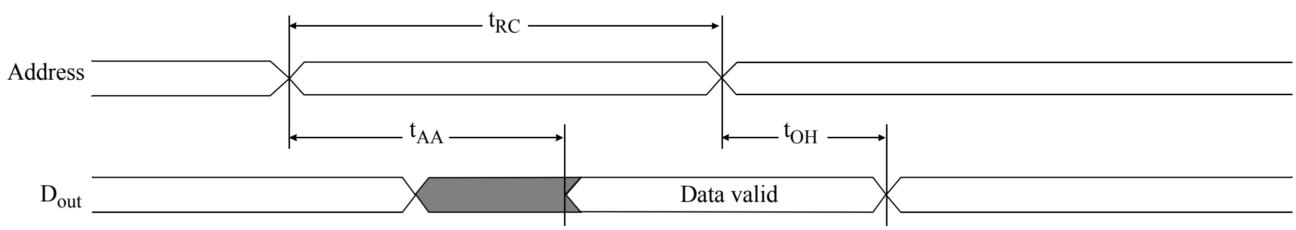
Read cycle (over the operating range)[3,9]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	6	–	7	–	8	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ LOW to output in low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ HIGH to output in high Z	t_{CHZ}	–	3	–	3	–	4	–	5	ns	4, 5
$\overline{OE}$ LOW to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ HIGH to output in high Z	t_{OHZ}	–	3	–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5

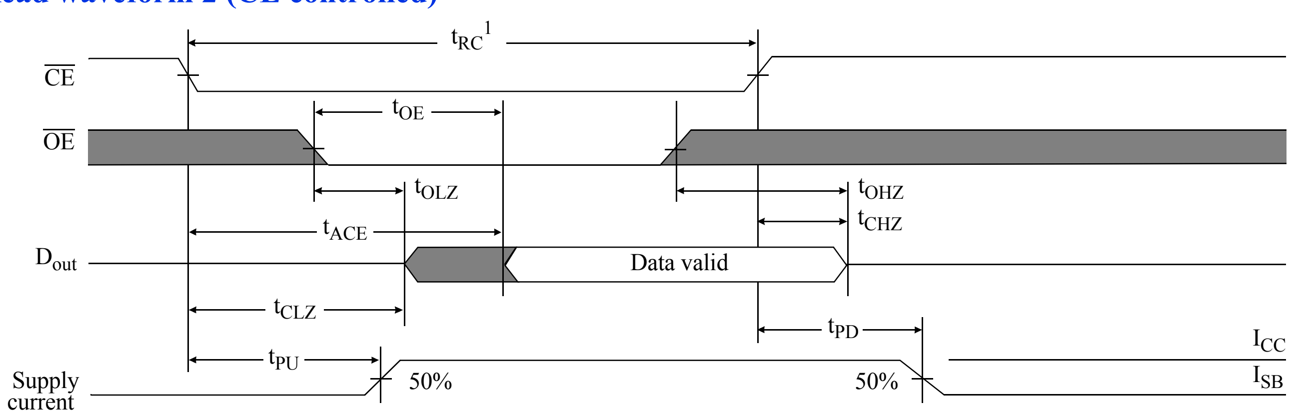
Key to switching waveforms

Rising input   Falling input   Undefined output/don't care

Read waveform 1 (address controlled)[3,6,7,9]



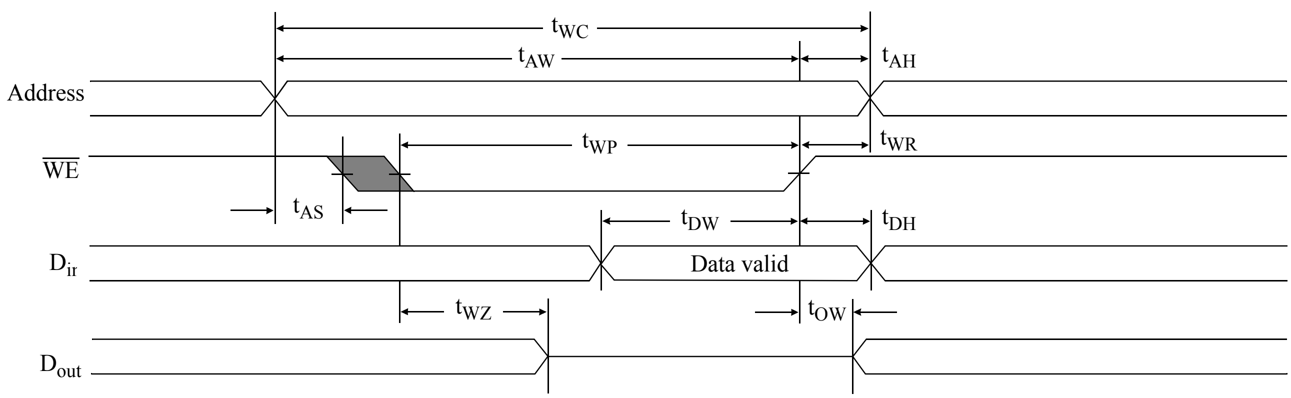
Read waveform 2 ($\overline{CE}$ controlled)[3,6,8,9]



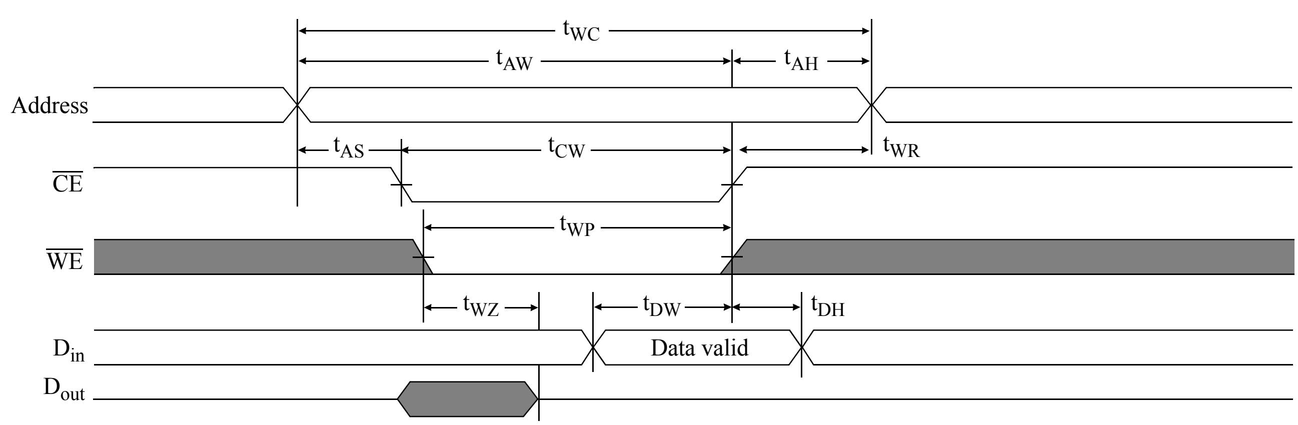
Write cycle (over the operating range)[11]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable to write end	t_{CW}	8	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	8	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	–	5	–	6	–	7	–	8	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



Write waveform 2 ($\overline{CE}$ controlled)[10,11]



AC test conditions

- Output load: see Figure B
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

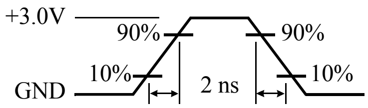


Figure A: Input pulse

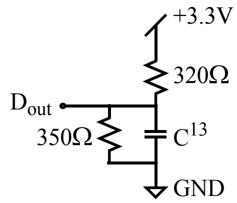


Figure B: Output load

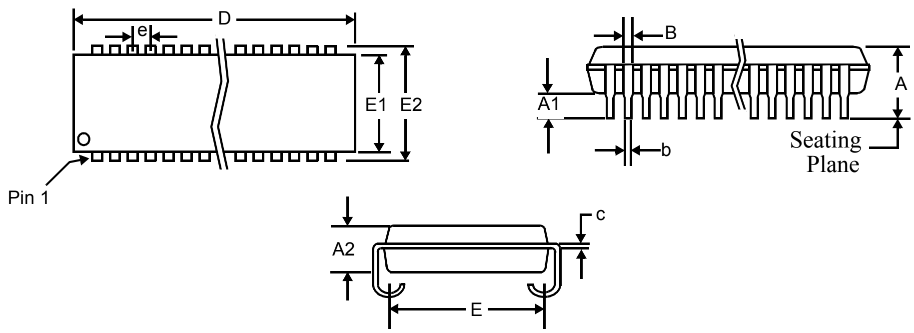
Thevenin equivalent

Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B.
4 These parameters are specified with CL = 5pF, as in Figures B. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 N/A
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A
13 C=30pF, except on High Z and Low Z parameters, where C=5pF.

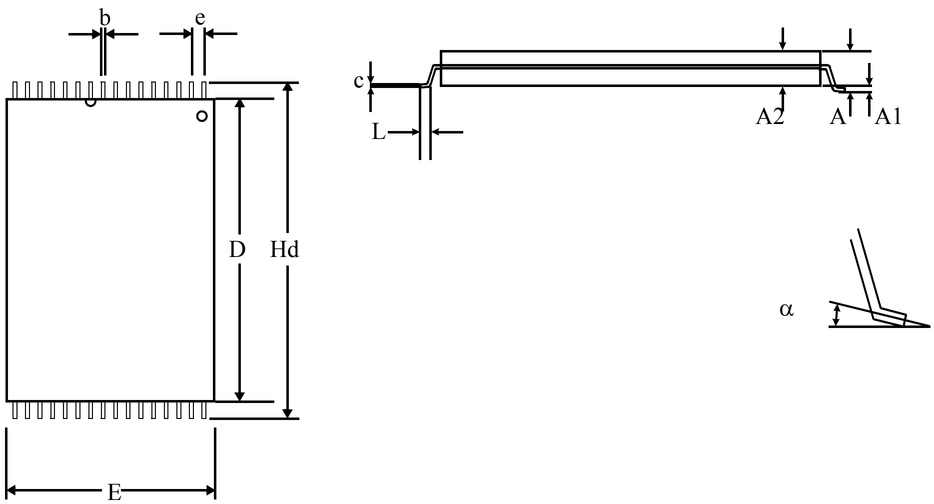
Package diagrams

28-pin SOJ



	28-pin SOJ	
	Min	Max
	in inches	
A	0.128	0.148
A1	0.026	-
A2	0.095	0.105
B	0.026	0.032
b	0.016	0.020
c	0.007	0.010
D	0.720	0.730
E	0.255	0.275
E1	0.295	0.305
E2	0.330	0.340
e	0.050 BSC	

28-pin TSOP1



	28-pin TSOP1 8×13.4 mm	
	Min	Max
A	1.00	1.20
A1	0.05	0.15
A2	0.91	1.05
b	0.17	0.27
c	0.10	0.20
D	11.70	11.90
e	0.55 nominal	
E	7.90	8.10
Hd	13.20	13.60
L	0.50	0.70
α	0°	5°

Ordering information

Package / Access time	Temperature	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 300 mil	Commercial	AS7C3256A-10JC	AS7C3256A-12JC	AS7C3256A-15JC	AS7C3256A-20JC
	Industrial	AS7C3256A-10JI	AS7C3256A-12JI	AS7C3256A-15JI	AS7C3256A-20JI
TSOP 8x13.4mm	Commercial	AS7C3256A-10TC	AS7C3256A-12TC	AS7C3256A-15TC	AS7C3256A-20TC
	Industrial	AS7C3256A-10TI	AS7C3256A-12TI	AS7C3256A-15TI	AS7C3256A-20TI

Note: Add suffix 'N'to the above part number for lead free parts. (Ex. AS7C3256A-10JIN)

Part numbering system

AS7C	3	256A	–XX	X	C or I	X
SRAM prefix	Voltage: 3 = 3.3V supply	Device number	Access time	Packages: J = SOJ 300 mil T = TSOP 8x13.4mm	Temperature range: C = 0 ^{o}C to 70 ^{0}C I = -40C to 85C	N= Lead Free Part

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