NCV1009

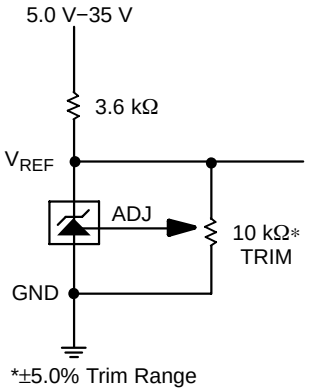
2.5 Volt Reference

The NCV1009 is a precision trimmed 2.5 V ±5.0 mV shunt regulator diode. The low dynamic impedance and wide operating current range enhances its versatility. The tight reference tolerance is achieved by on−chip trimming which minimizes voltage tolerance and temperature drift.

A third terminal allows the reference voltage to be adjusted ±5.0% to calibrate out system errors. In many applications, the NCV1009Z can be used as a pin−to−pin replacement of the LT1009CZ and the LM136Z−2.5 with the external trim network eliminated.

Features

- 0.2% Initial Tolerance Max.
- Guaranteed Temperature Stability
- Maximum 0.6 Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LT1009 and LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient
- Meets Mil Std 883C ESD Requirements
- Extended Operating Temperature Range for Use in Automotive Applications
- NCV Prefix, for Automotive and Other Applications Requiring Site and Change Control
- Pb−Free Packages are Available



If the external trim resistor is not used, the “ADJ. PIN” should be left floating. The 10k trim potentiometer does not effect the temperature coefficient of the device.

Figure 1. Application Diagram

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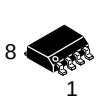
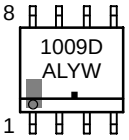
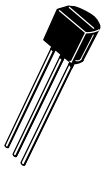
MARKING DIAGRAMS

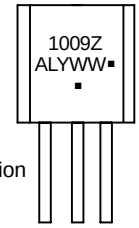


SOIC−8
D SUFFIX
CASE 751





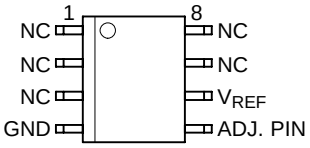
TO−92
Z SUFFIX
CASE 29

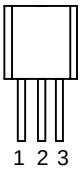


A = Assembly Location
L = Wafer Lot
Y = Year
WW, W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS





Pin 1. ADJ. PIN
2. V_{REF}
3. GND

ORDERING INFORMATION

Device	Package	Shipping
NCV1009D	SOIC−8	95 Units/Rail
NCV1009DR2	SOIC−8	2500 Tape & Reel
NCV1009DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
NCV1009Z	TO−92	2000 Units/Rail
NCV1009ZG	TO−92 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

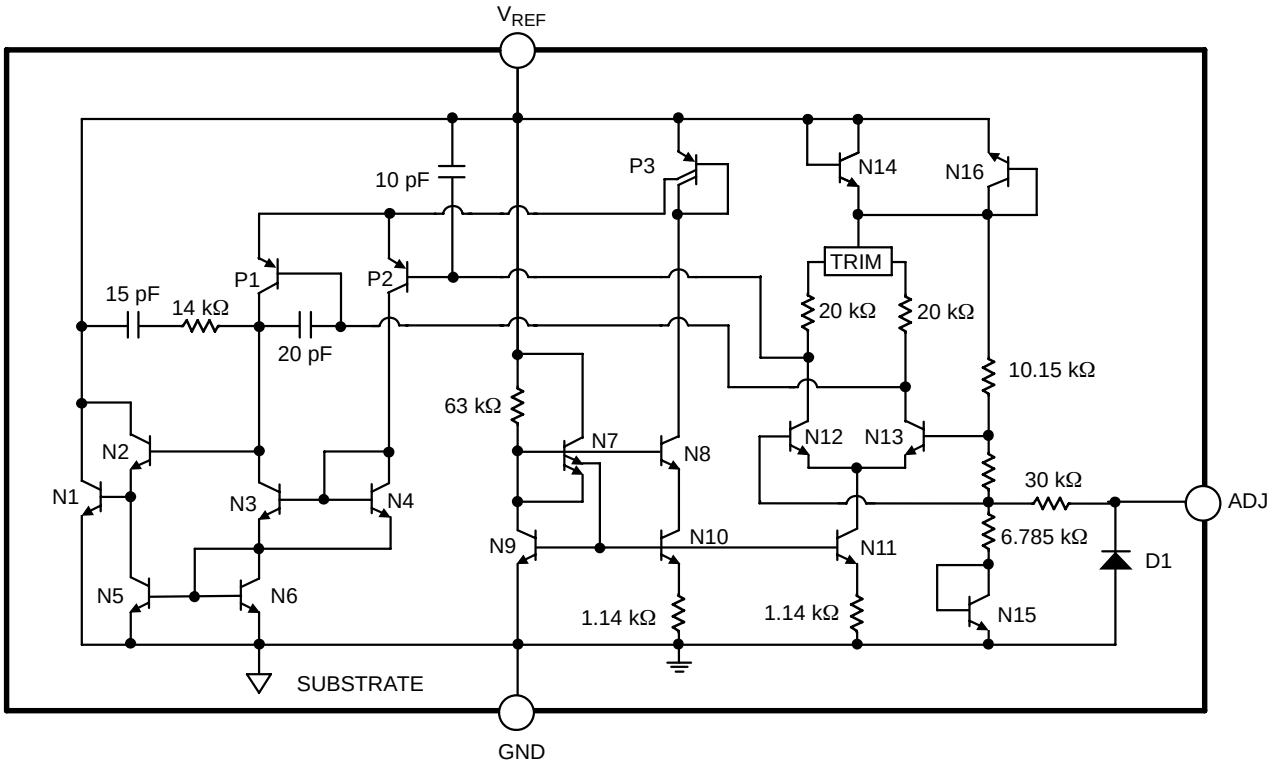


Figure 2. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Reverse Current		20	mA
Forward		10	mA
Package Thermal Resistance, SOIC−8: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$ Package Thermal Resistance, TO−92: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$		 45 165 – 170	 °C/W °C/W °C/W °C/W
Operating Temperature Range		−40 to +125	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Notes 2, 3)	260 peak 240 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
*The maximum package power dissipation must be observed.

1. 10 second maximum
2. 60 second maximum above 183°C.
3. −5°C / +0°C allowable conditions.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 1.0 mA	2.492	2.500	2.508	V
Reverse Breakdown Voltage	−40°C ≤ T_A ≤ 125°C	2.480	2.500	2.508	V
Reverse Breakdown Voltage Change with Current	400 μA ≤ I_R ≤ 10 mA (Note 4)	– –	2.6 3.0	5.0 6.0	mV mV
Reverse Dynamic Impedance	I_R = 1.0 mA (Note 4)	– –	0.2 0.4	1.0 1.4	Ω Ω
Temperature Stability Average Temperature Coefficient	0°C ≤ T_A ≤ 70°C, (Note 5) 0°C ≤ T_A ≤ 70°C, (Note 5)	– –	1.8 15	– –	mV ppm/°C
Long Term Stabilty	T_A = 25°C ±0.1 C, I_R = 1.0 mA	–	20	–	ppm/kHr

4. Denotes the specifications which apply over full operating temperature range.
5. Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

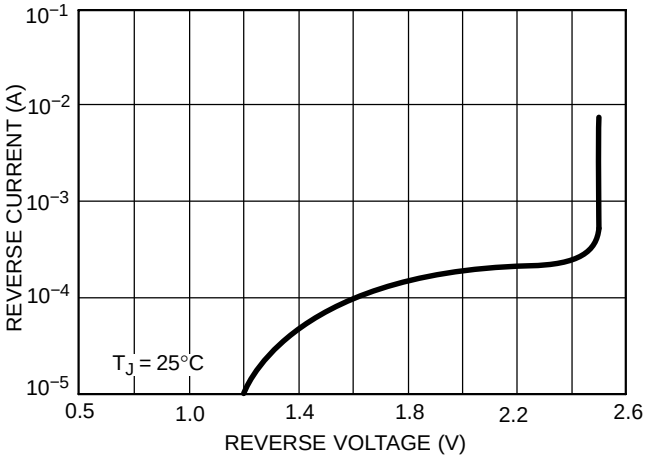


Figure 3. Reverse Current vs. Reverse Voltage

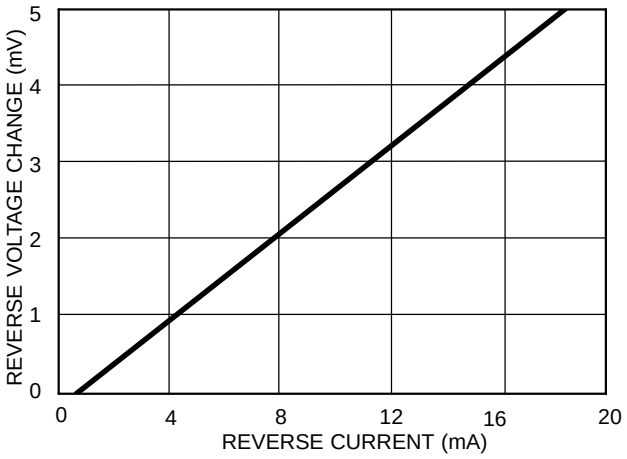


Figure 4. Change in Reverse Voltage vs. Reverse Current

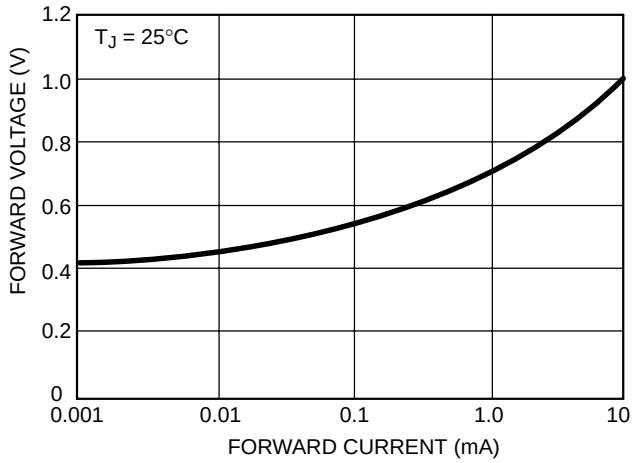


Figure 5. Forward Voltage vs. Forward Current

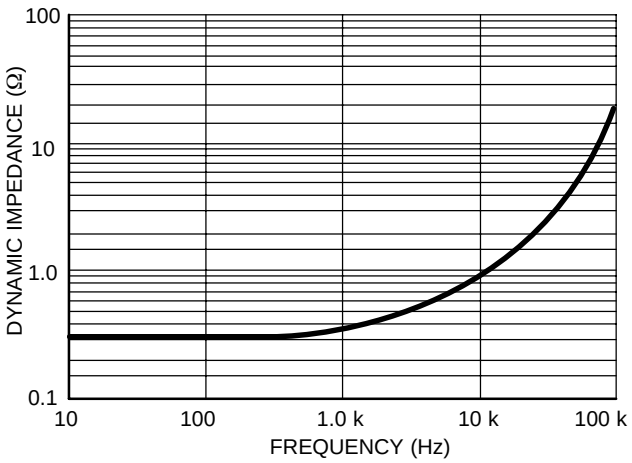


Figure 6. Dynamic Impedance vs. Frequency

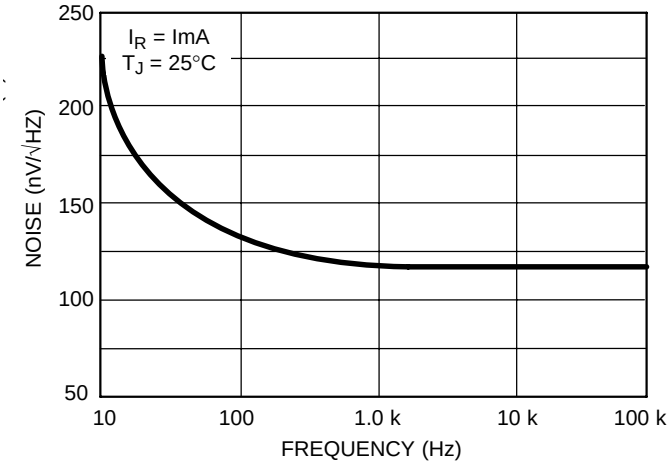


Figure 7. Zener Noise Voltage vs. Frequency

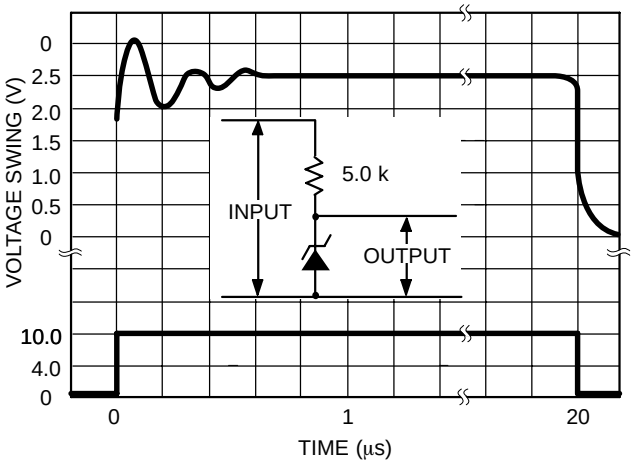
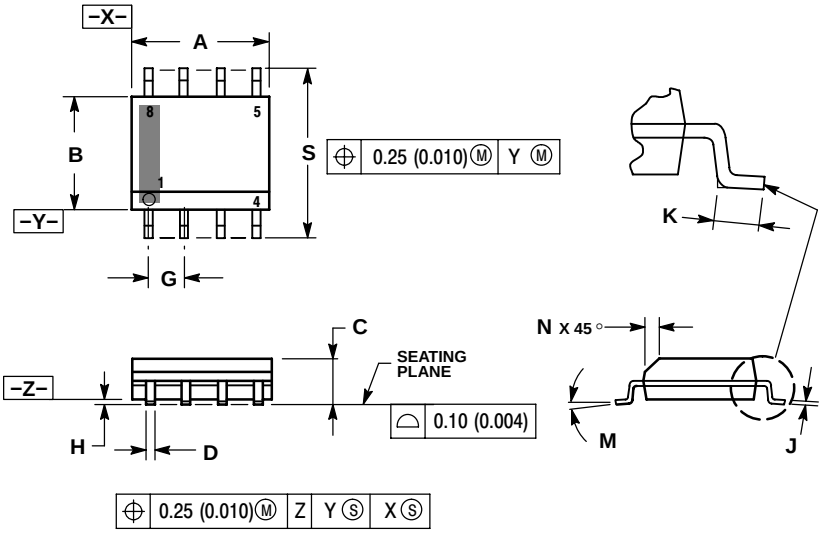


Figure 8. Response Time

PACKAGE DIMENSIONS

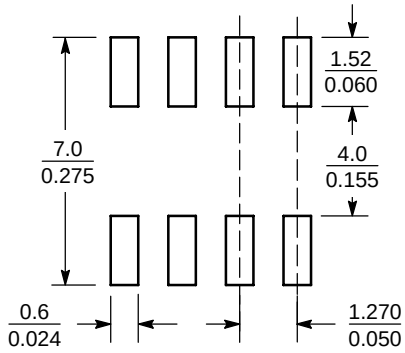
SOIC−8
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

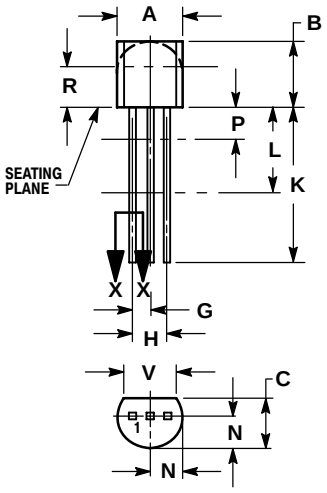


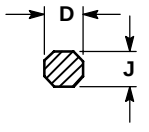
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−92
CASE 29−11
ISSUE AL





SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

PUBLICATION ORDERING INFORMATION

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