Document Number: A2G22S251-01S
Rev. 0, 5/2016

RF Power GaN Transistor

This 48 W RF power GaN transistor is designed for cellular base station applications covering the frequency range of 1805 to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1805 to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2000 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQ} = 200 mA, P_{out} = 48 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

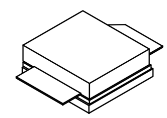
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	17.4	33.5	7.0	–34.7	–14
1990 MHz	17.3	34.3	7.1	–35.1	–11
2170 MHz	17.7	37.5	6.8	–33.2	–12

Features

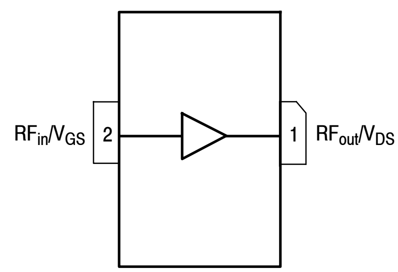
- High Terminal Impedances for Optimal Broadband Performance
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

A2G22S251-01SR3

1805–2200 MHz, 48 W AVG., 48 V AIRFAST RF POWER GaN TRANSISTOR



NI-400S-2S



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Gate-Source Voltage	V_{GS}	–8, 0	Vdc
Operating Voltage	V_{DD}	0 to +55	Vdc
Maximum Forward Gate Current @ T_C = 25°C	I_{GMAX}	24	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Operating Junction Temperature Range	T_J	–55 to +225	°C
Absolute Maximum Junction Temperature (1)	T_{MAX}	275	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 84°C, P_D = 88 W	$R_{\theta JC}$ (IR)	1.3 (2)	°C/W
Thermal Resistance by Finite Element Analysis, Junction-to-Case Case Temperature 85°C, P_D = 80 W	$R_{\theta JC}$ (FEA)	1.75 (3)	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	II

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = –8 Vdc, I_D = 20 mAdc)	$V_{(BR)DSS}$	150	—	—	Vdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 mAdc)	$V_{GS(th)}$	–3.8	–3.0	–2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 200 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	–3.6	–3.1	–2.3	Vdc
Gate-Source Leakage Current (V_{DS} = 0 Vdc, V_{GS} = –5 Vdc)	I_{GSS}	–7.5	—	—	mAdc

1. Functional operation above 225°C has not been characterized and is not implied. Operation at T_{MAX} (275°C) reduces median time to failure by an order of magnitude; operation beyond T_{MAX} could cause permanent damage.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
3. $R_{\theta JC}$ (FEA) must be used for purposes related to reliability and limitations on maximum junction temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the junction temperature in degrees Celsius, *A* = –10.3 and *B* = 8260.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQ} = 200 mA, P_{out} = 48 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. **[See note on correct biasing sequence.]**					
Power Gain	G_{ps}	16.2	17.7	19.2	dB
Drain Efficiency	η_D	33.5	37.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.2	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	–33.2	–30	dBc
Input Return Loss	IRL	—	–12	–5	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 200 mA, f = 1990 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 55 Vdc, 250 W Pulsed CW Output Power (3 dB Input Overdrive from 170 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQ} = 200 mA, 1805–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	158	—	W
P_{out} @ 3 dB Compression Point (2)	P3dB	—	195	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–2170 MHz bandwidth)	Φ	—	–16.9	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 365 MHz Bandwidth @ P_{out} = 48 W Avg.	G_F	—	0.36	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.014	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.002	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2G22S251-01SR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	NI-400S-2S

1. Part internally input matched.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P) voltage, typically –5 V
2. Turn on V_{DS} to nominal supply voltage (50 V)
3. Increase V_{GS} until I_{DS} current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce V_{GS} down to V_P, typically –5 V
3. Reduce V_{DS} down to 0 V (Adequate time must be allowed for V_{DS} to reduce to 0 V to prevent severe damage to device.)
4. Turn off V_{GS}

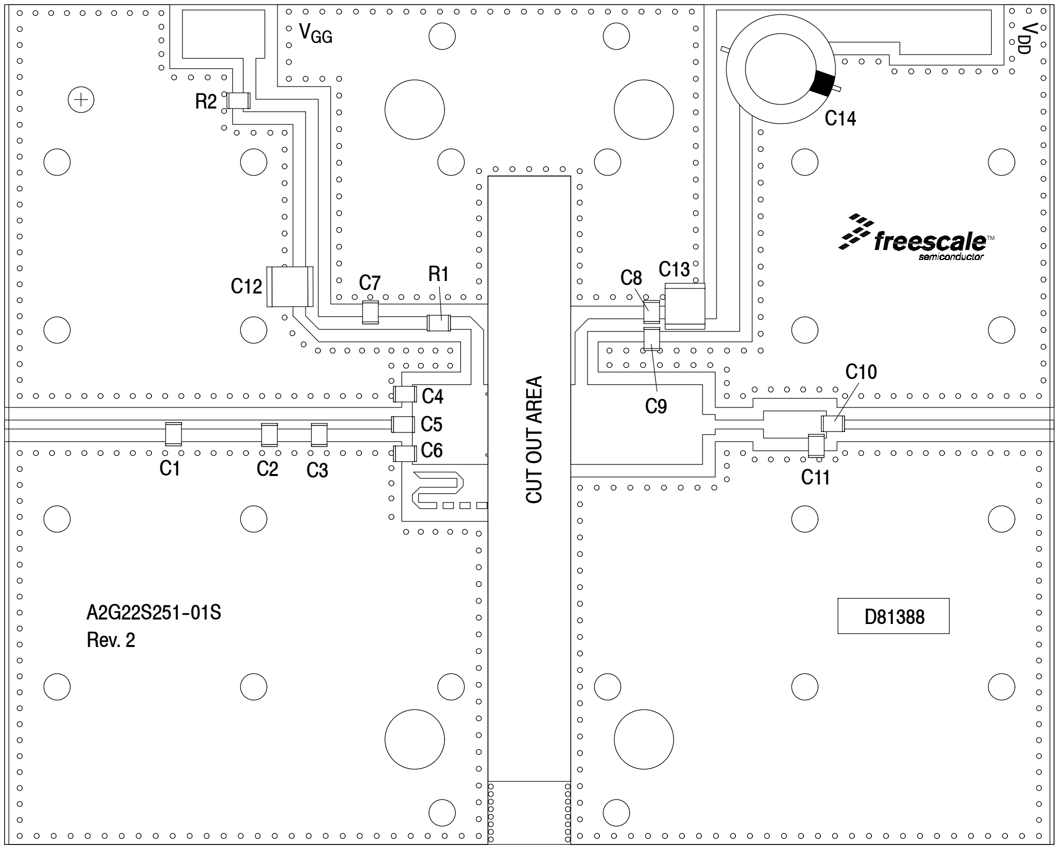


Figure 2. A2G22S251-01SR3 Test Circuit Component Layout

Table 6. A2G22S251-01SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C2, C3	1.5 pF Chip Capacitors	ATC600F1R5BT250XT	ATC
C4, C11	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C5, C7	11 pF Chip Capacitors	ATC600F110JT250XT	ATC
C6	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
C8, C9, C10	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C12, C13	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C14	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26-RH	Multicomp
R1	3.9 Ω, 1/4 W Chip Resistor	CRCW12063R90FKEA	Vishay
R2	1.5 kΩ, 1/4 W Chip Resistor	CRCW12061K50FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D81388	MTL

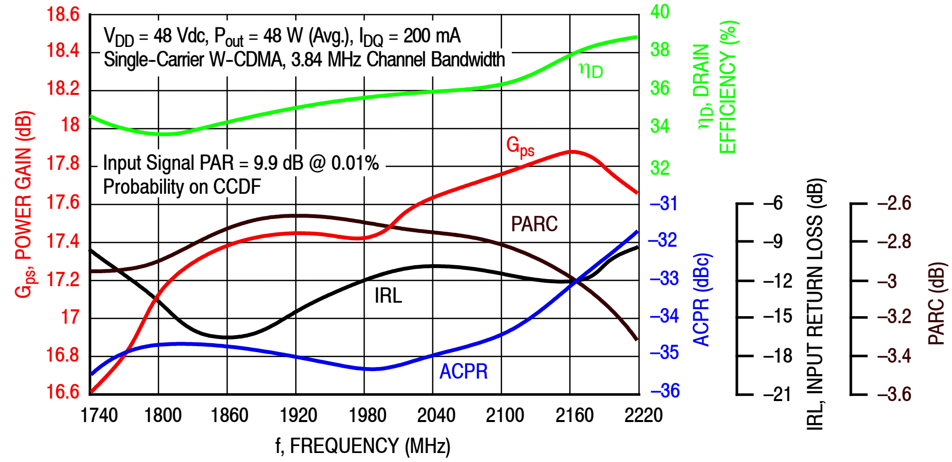


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 48 Watts Avg.

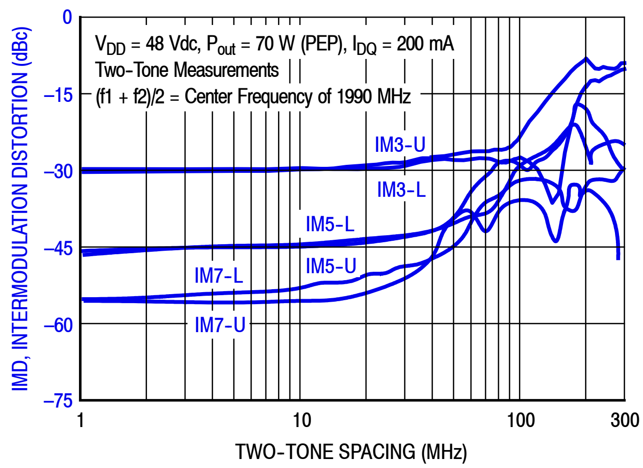


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

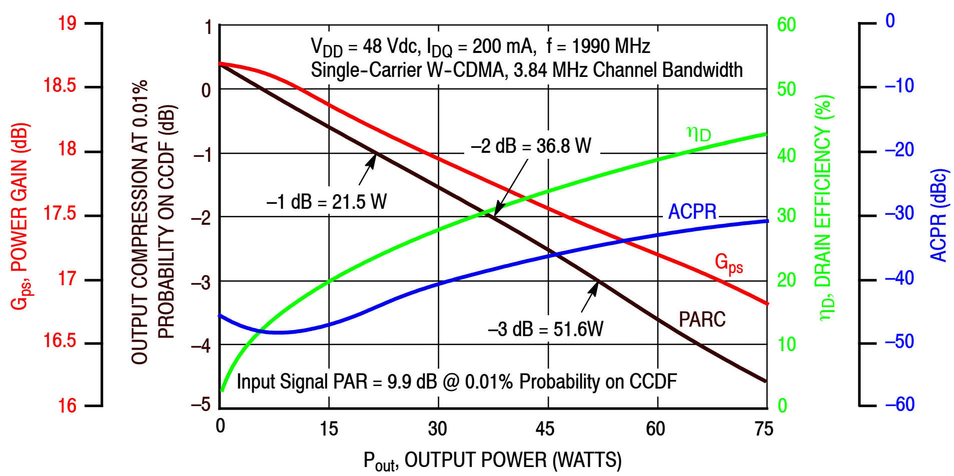


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

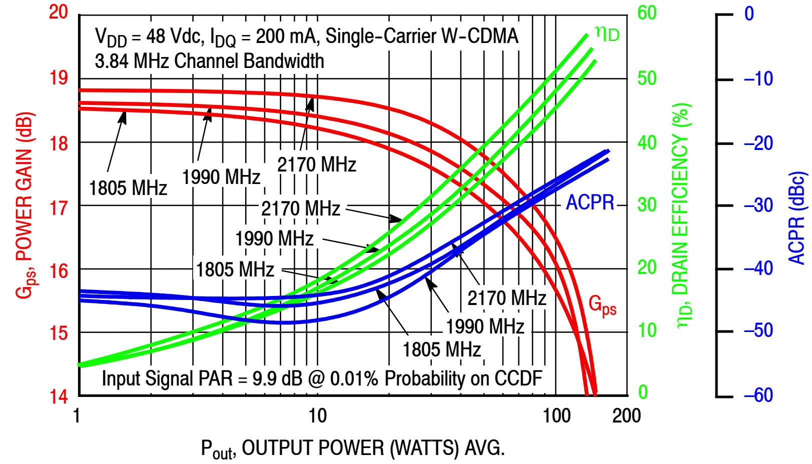


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

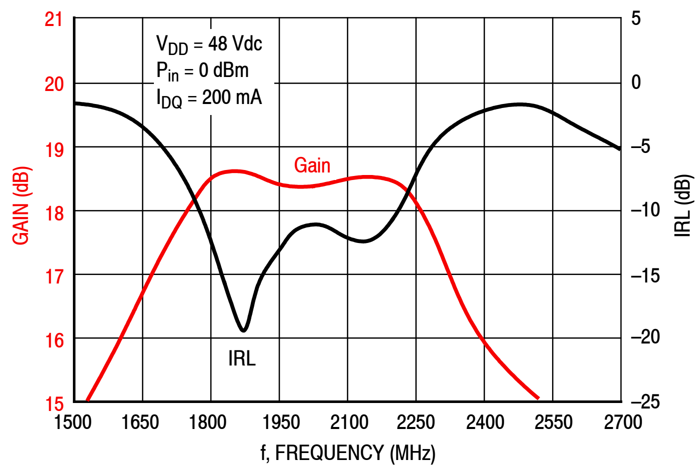


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 222 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.35 – j6.11	2.60 + j6.52	2.39 – j2.34	18.8	53.1	202	55.9	–13
1990	4.56 – j7.73	6.02 + j8.13	2.38 – j3.05	18.4	52.7	185	54.2	–13
2170	10.1 – j2.50	9.62 + j1.70	2.62 – j3.64	18.2	52.5	177	51.4	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.35 – j6.11	2.67 + j6.93	3.62 – j3.15	17.1	54.4	277	63.8	–15
1990	4.56 – j7.73	6.90 + j8.73	3.70 – j4.14	16.6	54.2	263	61.0	–16
2170	10.1 – j2.50	9.93 + j0.17	3.70 – j4.12	16.6	54.0	254	60.5	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

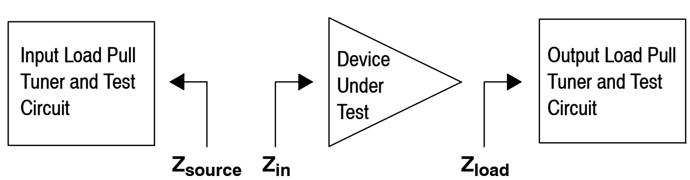
Table 8. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 222 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.35 – j6.11	2.07 + j7.17	2.18 – j0.08	20.5	50.9	124	68.5	–29
1990	4.56 – j7.73	5.77 + j9.93	2.25 – j0.84	20.2	50.5	113	65.5	–27
2170	10.1 – j2.50	12.1 – j0.35	2.03 – j1.14	20.2	50.2	104	63.8	–27

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.35 – j6.11	2.13 + j7.61	2.56 – j0.03	18.7	52.1	161	75.8	–37
1990	4.56 – j7.73	7.18 + j10.9	2.84 – j0.78	18.5	51.9	156	73.8	–36
2170	10.1 – j2.50	11.0 – j2.92	2.30 – j1.05	18.4	51.5	140	72.1	–39

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 1990 MHz

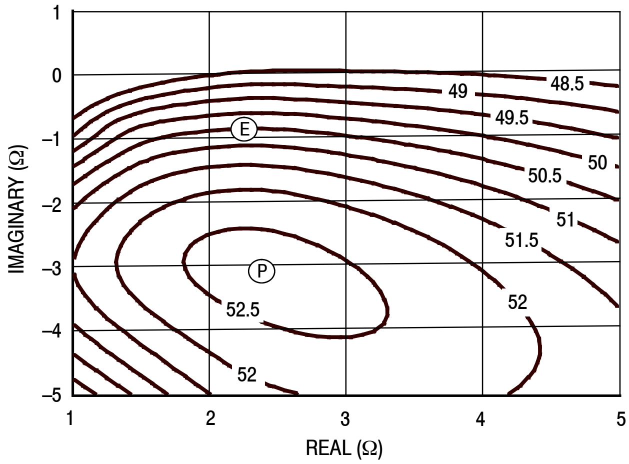


Figure 8. P1dB Load Pull Output Power Contours (dBm)

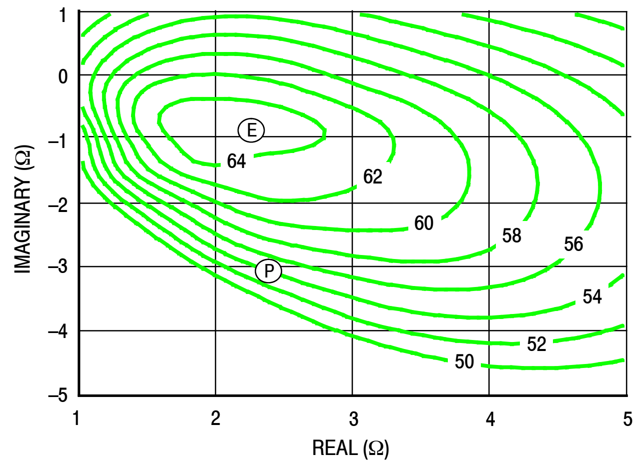


Figure 9. P1dB Load Pull Efficiency Contours (%)

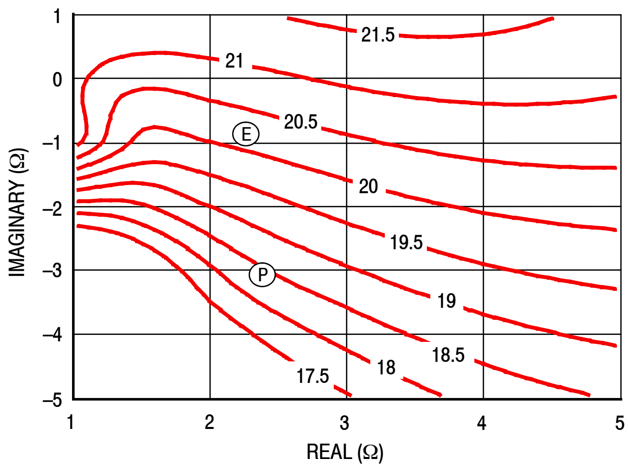


Figure 10. P1dB Load Pull Gain Contours (dB)

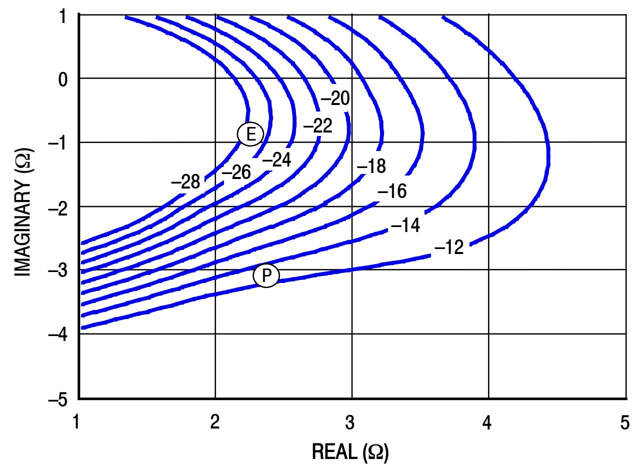


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 1990 MHz

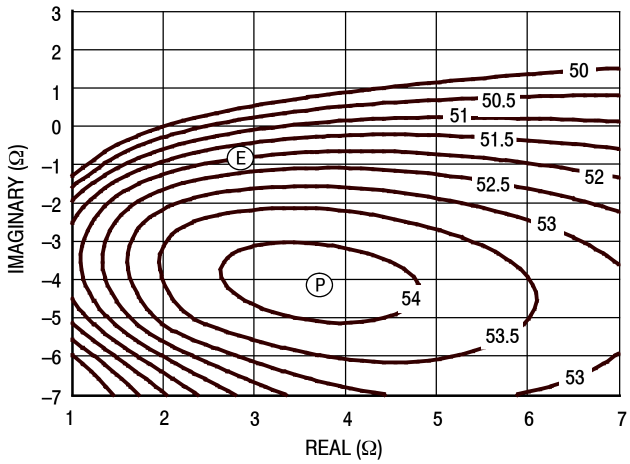


Figure 12. P3dB Load Pull Output Power Contours (dBm)

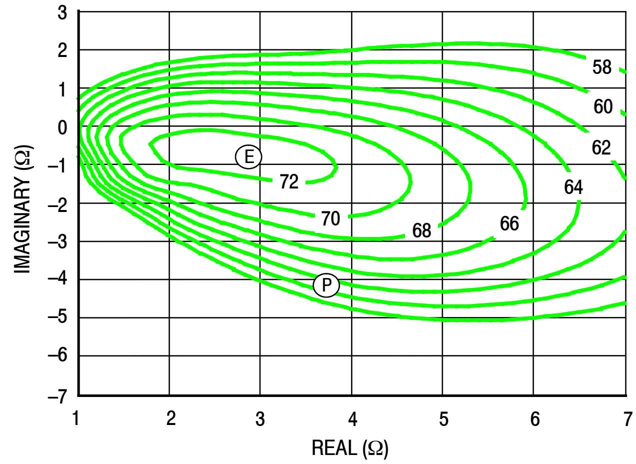


Figure 13. P3dB Load Pull Efficiency Contours (%)

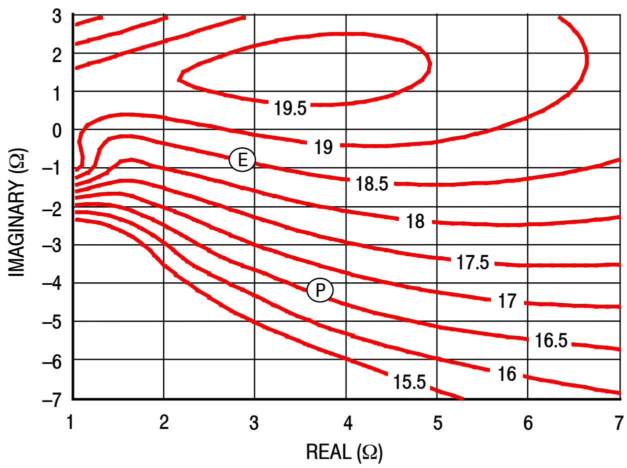


Figure 14. P3dB Load Pull Gain Contours (dB)

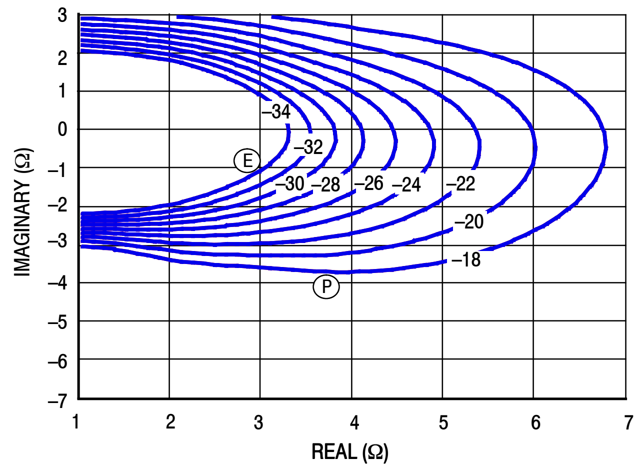


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

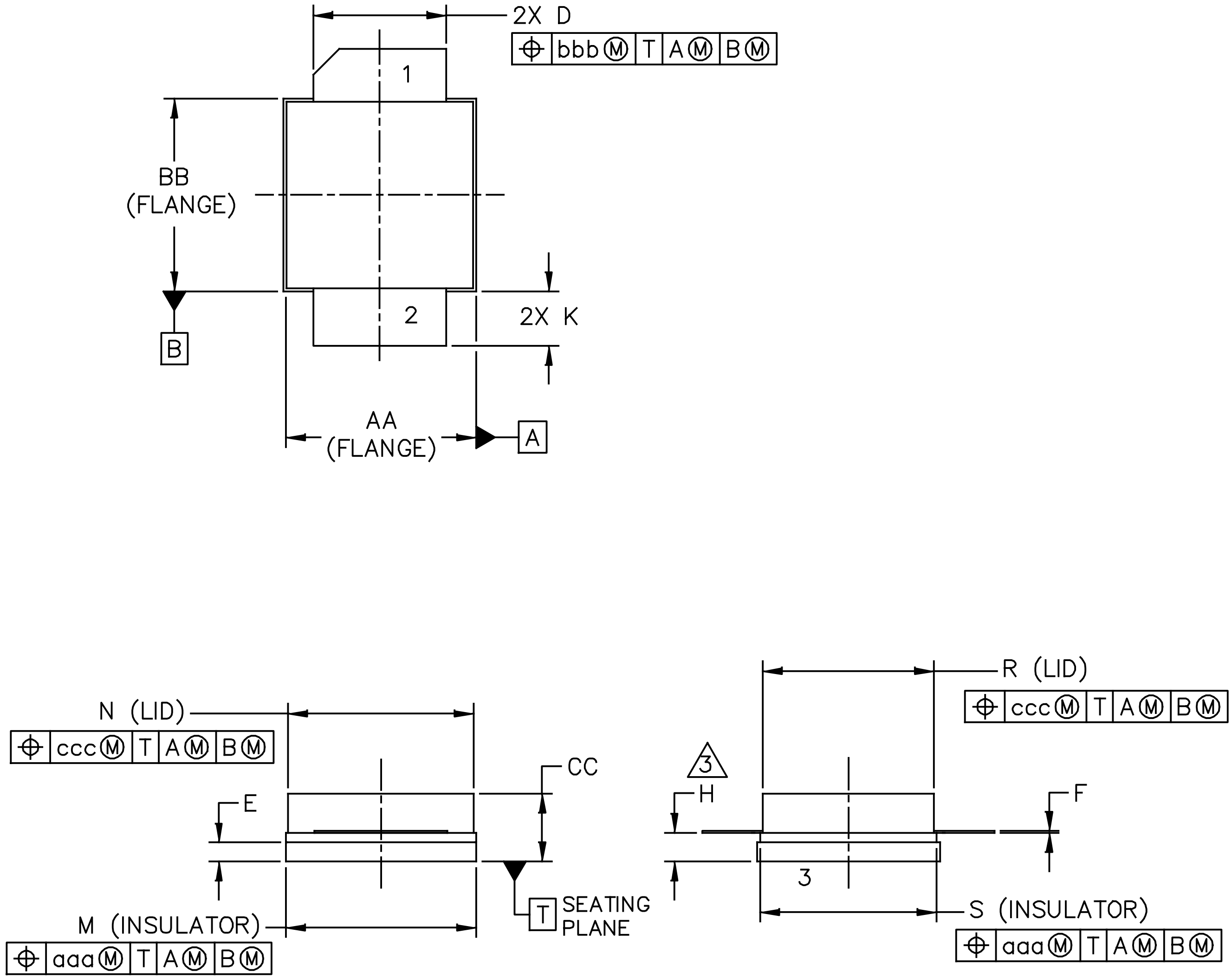
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI–400S–2S	DOCUMENT NO: 98ASA10732D REV: C	
	STANDARD: NON–JEDEC	
	SOT1828–1 13 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. (△) DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM THE FLANGE TO CLEAR THE EPOXY FLOW OUT REGION PARALLEL TO DATUM B.

4. INPUT & OUTPUT LEADS (PIN 1 & 2) MAY HAVE SMALL FEATURES SUCH AS SQUARE HOLES OR NOTCHES FOR MANUFACTURING CONVENIENCE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.395	.405	10.03	10.29	aaa	.005		0.13	
BB	.382	.388	9.70	9.86	bbb	.010		0.25	
CC	.125	.163	3.18	4.14	ccc	.015		0.38	
D	.275	.285	6.98	7.24					
E	.035	.045	0.89	1.14					
F	.004	.006	0.10	0.15					
H	.057	.067	1.45	1.70					
K	.0995	.1295	2.53	3.29					
M	.395	.405	10.03	10.29					
N	.385	.395	9.78	10.03					
R	.355	.365	9.02	9.27					
S	.365	.375	9.27	9.53					

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-400S-2S	DOCUMENT NO: 98ASA10732D	REV: C
	STANDARD: NON-JEDEC	
	SOT1828-1	13 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2016	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: A2G22S251-01S
Rev. 0, 5/2016