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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

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HAT2131R

Silicon N Channel Power MOS FET Power Switching

REJ03G1815-0100

Rev.1.00

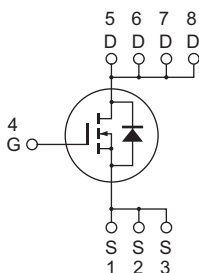
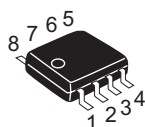
Jul 17, 2009

Features

- Low on-resistance
- Low drive current
- High density mounting
- Capable of 4 V gate drive

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	350	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.9	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	7.2	A
Body-drain diode reverse drain current	I_{DR}	0.9	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	7.2	A
Channel dissipation	P_{ch} ^{Note2}	2.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10 s$

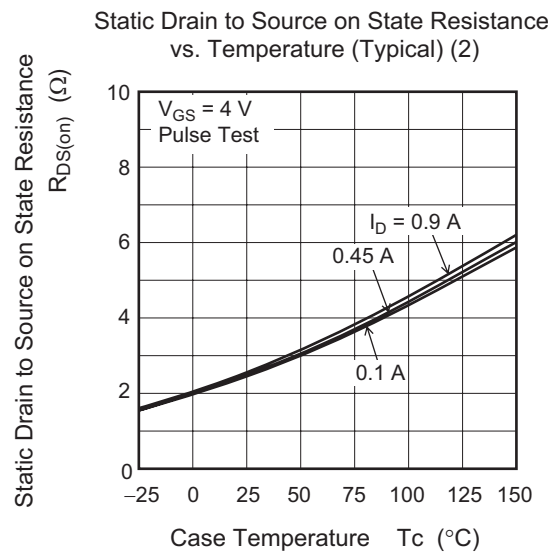
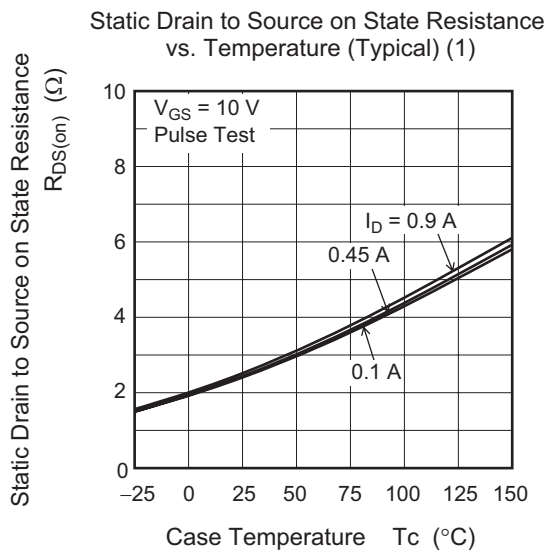
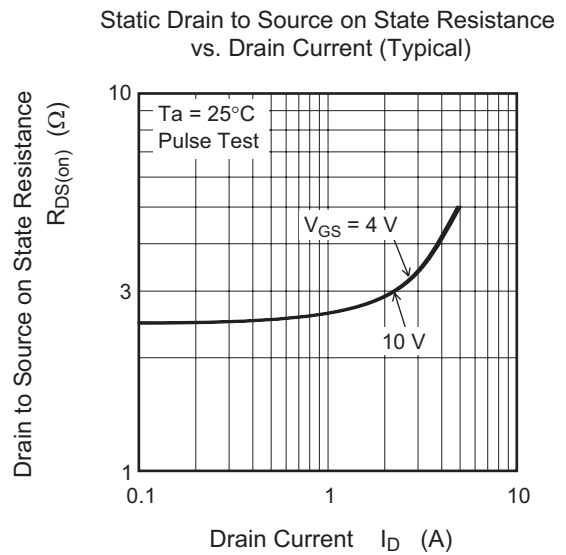
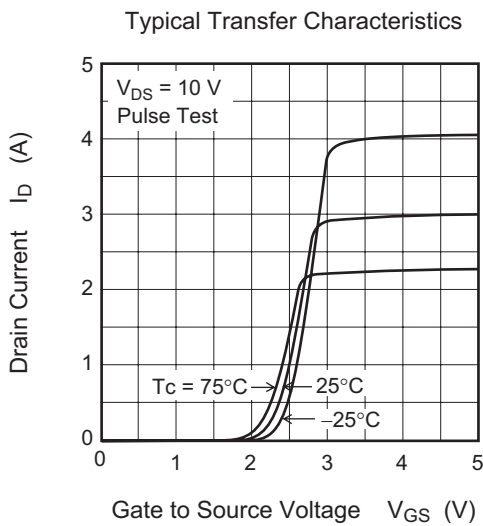
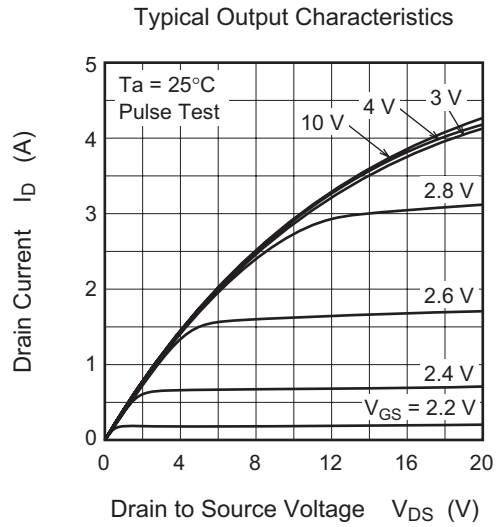
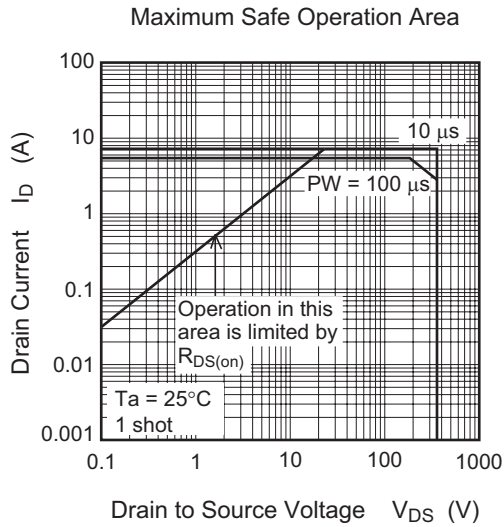
Electrical Characteristics

(Ta = 25°C)

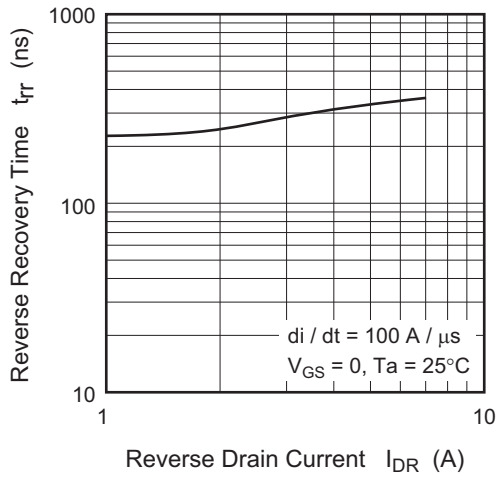
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	350	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	0.1	μA	$V_{DS} = 350 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = 0.45 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.0	Ω	$I_D = 0.45 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	2.6	3.2	Ω	$I_D = 0.45 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	460	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	32	—	pF	
Reverse transfer capacitance	C_{rss}	—	8	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 0.45 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 556 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	13	—	ns	
Turn-off delay time	$t_{d(off)}$	—	76	—	ns	
Fall time	t_f	—	50	—	ns	
Total gate charge	Q_g	—	20	—	nC	$V_{DD} = 250 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 0.9 \text{ A}$
Gate to source charge	Q_{gs}	—	1	—	nC	
Gate to drain charge	Q_{gd}	—	6	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.8	1.2	V	$I_F = 0.9 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	220	—	ns	$I_F = 0.9 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 3. Pulse test

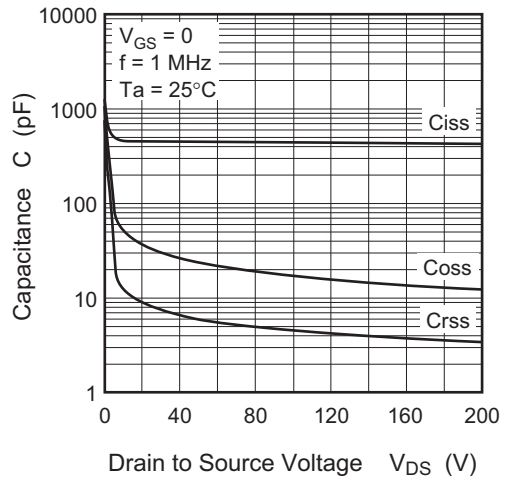
Main Characteristics



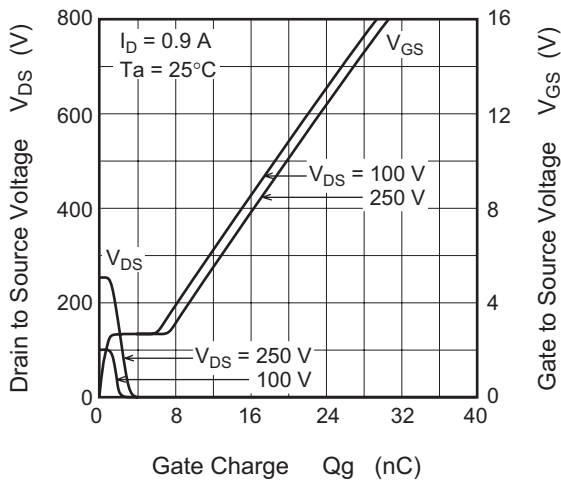
Body-Drain Diode Reverse Recovery Time (Typical)



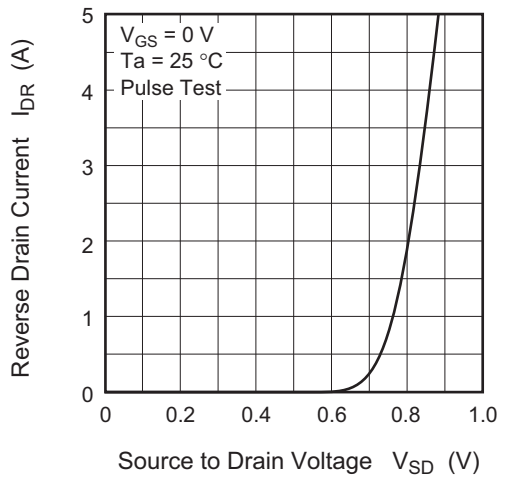
Typical Capacitance vs. Drain to Source Voltage



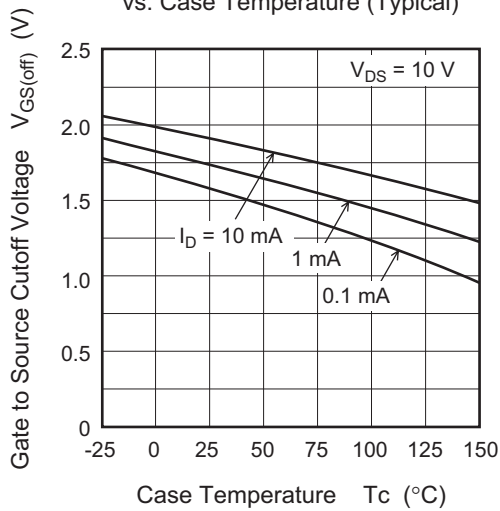
Dynamic Input Characteristics (Typical)

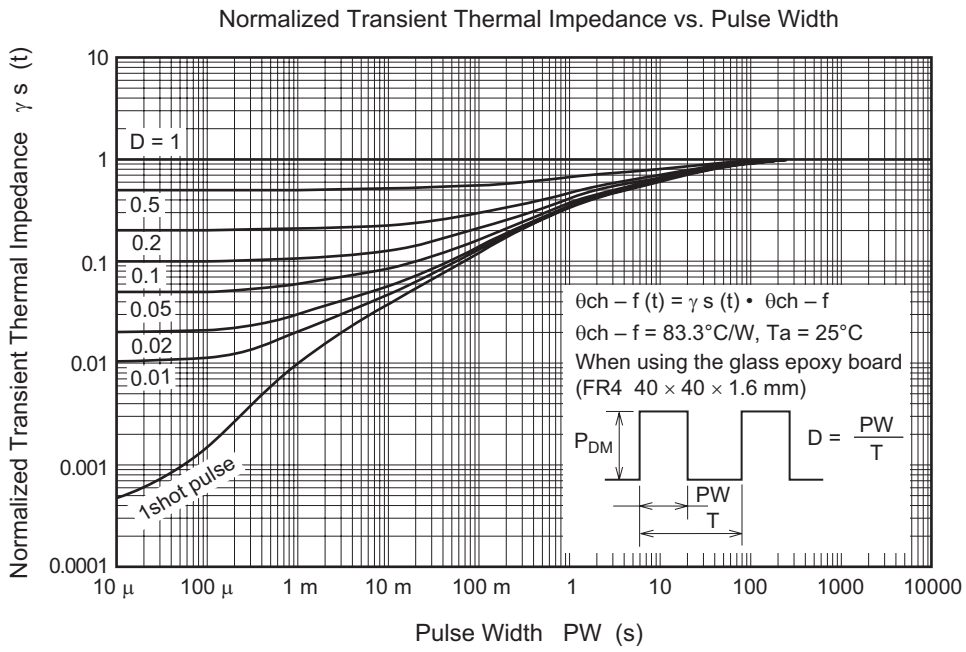


Reverse Drain Current vs. Source to Drain Voltage (Typical)

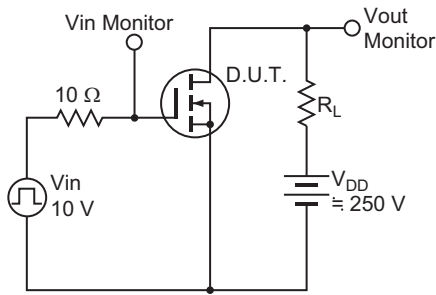


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

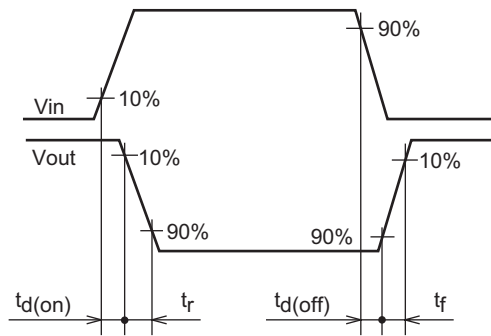




Switching Time Test Circuit

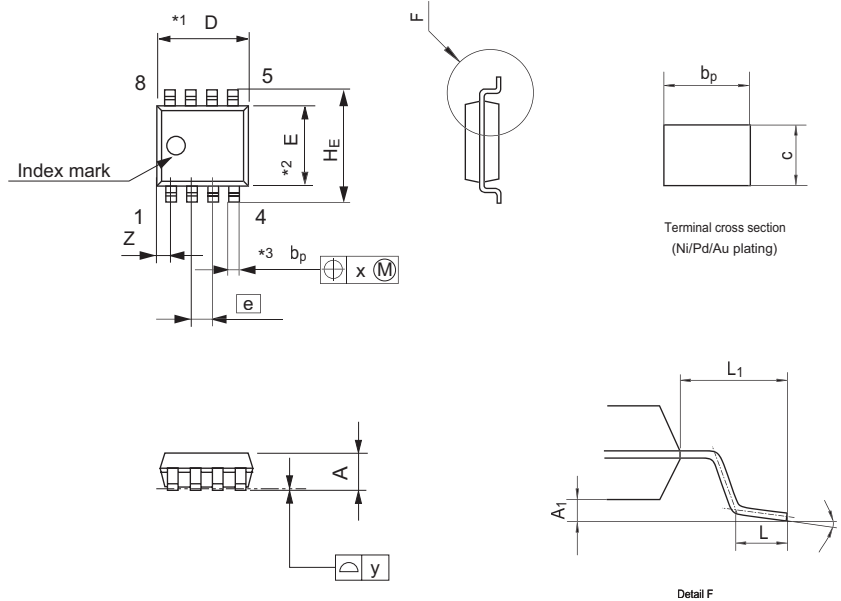


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
 1. DIMENSIONS *1(Nom)* AND *2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A ₂	—	—	—
A ₁	0.10	0.14	0.25
A	—	—	1.75
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	5.80	6.10	6.20
Ⓜ	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L ₁	—	1.08	—

Ordering Information

Part No.	Quantity	Shipping Container
HAT2131R-EL-E	2500 pcs	Taping

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