UG130: Si86xxT-EVB User's Guide

The Si864xxT devices, the latest addition to the Si86xx isolator family, are 4-channel CMOS-based galvanic digital isolators surge rated at 10 kV. Operating up to 150 Mbps, they are available in wide body 16-pin SOIC packages and designed for the stringent isolation needs of the industrial, commercial, and automotive markets. Various channel configurations dictating the number of reverse channels and default output states are also available per the Si86xx data sheet's ordering guide.

The Si864xxT-EVB allows designers to quickly evaluate the Si8642ET's capabilities and functionality, either by driving inputs to logic low via shunts, or injecting signals to the header pins via single wires or a 2x6 ribbon cable (not included).

For more information on our Si86xxT isolators, visit the Silicon Labs website at: http://www.silabs.com/isolation. The product data sheet and application notes can be referenced to help facilitate designs.

KEY POINTS

- Discusses kit contents and equipment.
- Describes hardware setup and demonstration.
- Shows EVB schematic and layout.
- Includes bill of materials and the ordering guide for Si864xxT-KIT.

1. Kit Contents

The Si864xxT Evaluation Kit contains the following items:

- Si864xxT-EVB evaluation board, shown in the figure below.
- Si8642ET-IS, 4-channel (Reverse: 3 and 4), 150 Mbps, 10 kV, Wide Body, Default High I/O.

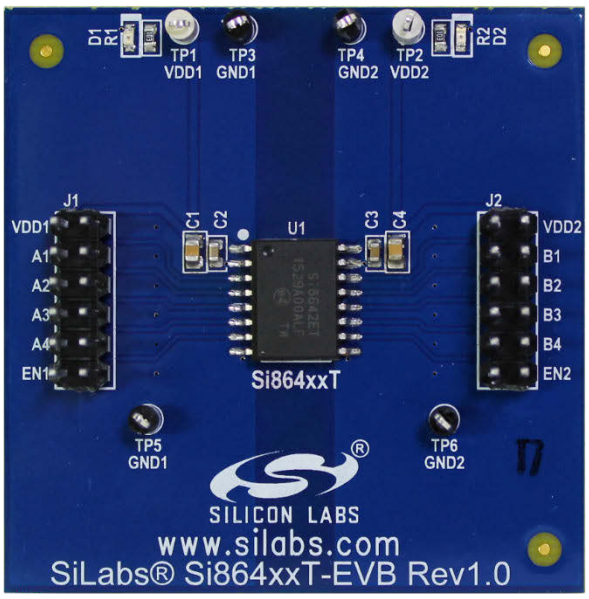


Figure 1.1. Si86xxT-EVB

2. Required Equipment

The following equipment is required to demonstrate the evaluation board:

- Two DC Power supplies 2.5–5.5 V, 100 mA.
  - (Optionally) Isolated from one another.
- Four banana-to-test-clip cables with clips to supply power to the board.
- Two 2-pin header shunts (included).
- One DMM.
- One DMM Voltage Probe Set.

2.1 Optional Equipment

The following equipment is optional and can be used to demonstrate more of the evaluation board functionalities, including signal propagation statistics:

- One Signal generator.
- Two BNC Coaxial cables.
- One BNC splitter.
- One BNC to test-clip connector.
- One 2-Channel Oscilloscope.
- One 10x Voltage Probe.

3. Hardware Setup and Demonstration

3.1 Powering the Supplies

Both sides of the Si8642ET isolator accept supplies between 2.5-5.5 V. See the figure below.

Perform the following steps to set up the Si864xxT-EVB:

- Remove all shunts.
- Power Side-A.
  - Clip 5.0 V from the first power supply to TP1 (VDD1) and its GND to TP3 or TP5 (GND1).
  - LED, D1, will light up, confirming power is supplied.
- Power Side-B.
  - Clip 5.0 V from the second power supply to TP2 (VDD2) and its GND to TP4 or TP6 (GND2).
  - LED, D2, will light up, confirming power is supplied.

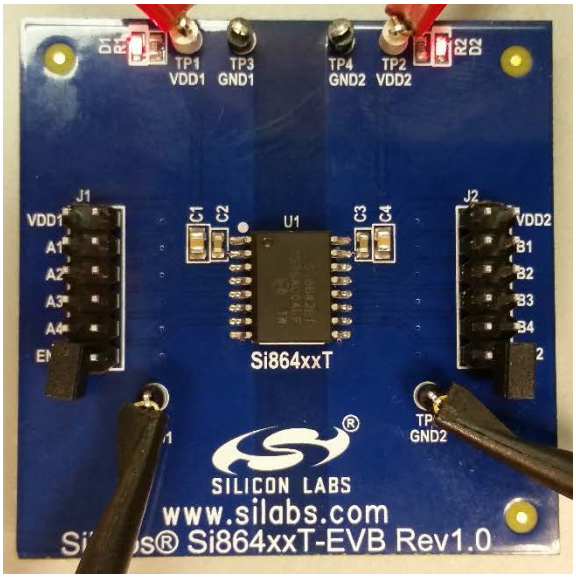


Figure 3.1. EVB — Powered Up

3.2 DC Signal Demonstration

3.2.1 Defaults

The default output signal state of the Si8642ET is a logic High, meaning that with all shunts removed (EN1 and EN2 floating), all digital inputs (A1, A2, B3, B4) and all digital outputs will (B1, B2, A3, A4) will be at their respective High voltage level. These values can be measured and confirmed using the DMM.

- Remove all shunts.
  - Measure with the DMM that all digital inputs (A1, A2, B3, B4) are logic High.
  - Measure with the DMM that all digital outputs (B1, B2, A3, A4) are logic High.

See Figure 3.1 EVB — Powered Up on page 3.

3.2.2 Fail-safes

When power is removed from one side of the isolator, the outputs at the other side of the isolator default to logic High.

- A-side
  - Remove all shunts.
  - Remove A-side power supply.
  - Measure B-side outputs, B1 and B2 and see that they are logic High.
  - Replace A-side power and see B1 and B2 driven to their appropriate states.
- B-side
  - Remove all shunts.
  - Remove B-side power supply.
  - Measure A-side outputs, A3 and A4 and see that they are logic High.
  - Replace B-side power and see A3 and A4 drive to their appropriate states.

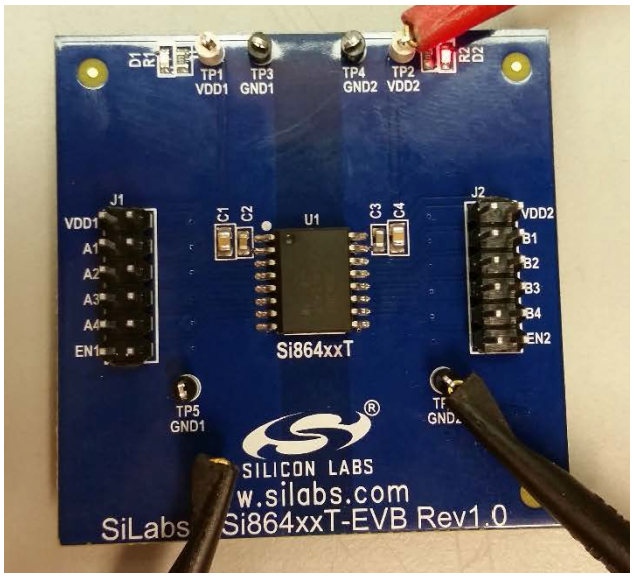


Figure 3.2. EVB — Failsafe, No VDDA

3.2.3 Configured

For an example, see the figure below.

- Place a shunt across J1 at A2.
  - This produces a logic Low input on forward channel A2. The SI88642ET will transmit this to the B-side, and the corresponding logic Low can be observed and measured with the DMM on J2, B2.
- Place a shunt across J2 at B3.
  - This produces a logic Low input on reverse channel B3. The SI88642ET will transmit this to the A-side, and the corresponding logic Low can be measured with the DMM on J1, A3.

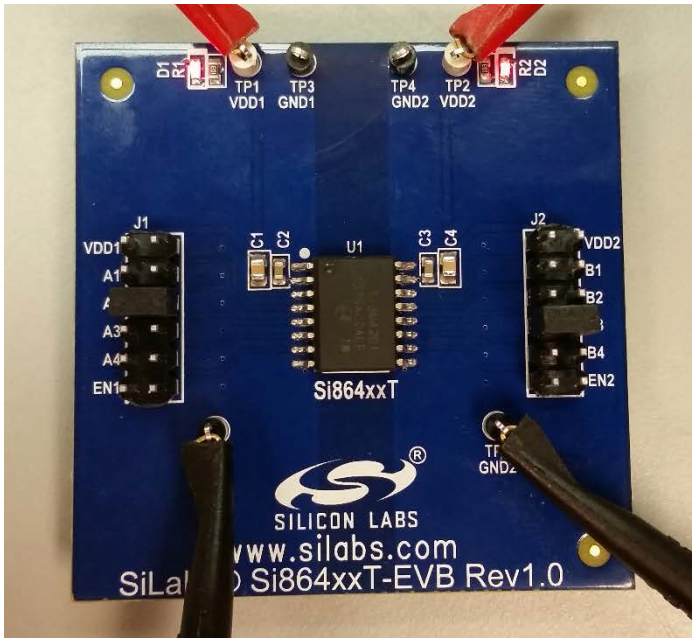


Figure 3.3. EVB Configured for DC Signal Demonstration without Enable

3.2.4 Utilizing Enable

For an example, see the figure below.

- Place a shunt across J1 at A2.
  - This produces a logic Low input on forward channel A2. The SI88642ET will transmit this to the B-side, and the corresponding logic Low can be observed and measured with the DMM on J2, B2.
- Place a shunt across J2 at EN2.
  - This drives EN2 to a logic Low input which tri-states outputs B1 and B2. A Hi-Z output can be observed on outputs B1 and B2 with the DMM (appearing as a high), even while A1 is a logic Low and A2 is a logic High.

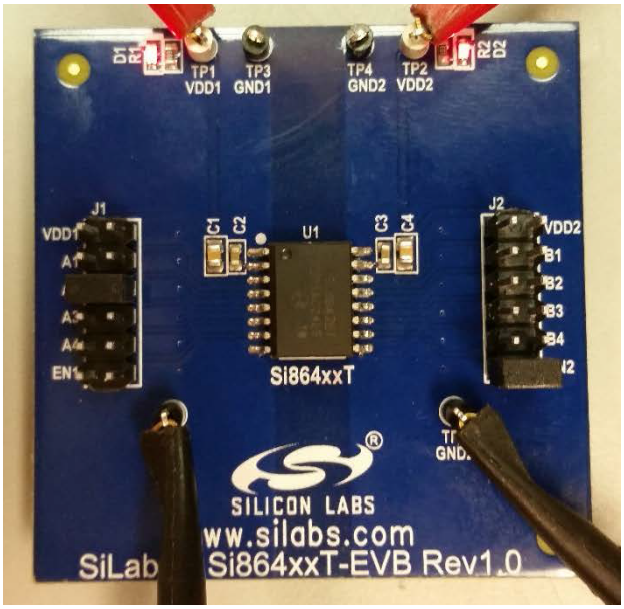


Figure 3.4. EVB Configured for DC Signal Demonstration with Enable

3.3 Optional Dynamic Signal Demonstration

Note: Logic inputs should NOT exceed the respective VDD.

For an example, see the figure below.

- Remove all shunts.
- Setup signal generator and oscilloscope.
  - Generate 0 V to VDD1 peak, square wave (up to 300 MHz, but within the oscilloscope's capabilities) on the signal generator.
  - Split the signal generator output to two separate BNC cables via the splitter.
  - Attach one BNC cable end to oscilloscope Channel 1 and configure the channel for 1x gain.
  - Attach the 10x oscilloscope probe to oscilloscope channel 2 configure the channel for 10x gain.
  - Connect the remaining BNC cable end to the BNC-to-test-clip adapter.
  - Clip the signal generator's output to A2 relative to GND1 (via either TP5 or TP3).
  - Clip the oscilloscope probe's signal line on B1 and reference to GND2 (via either TP4 or TP6).
- Observe Channel 1 (input – A2) and Channel 2 (output – B2) on the oscilloscope for various parametrics such as skew and jitter.

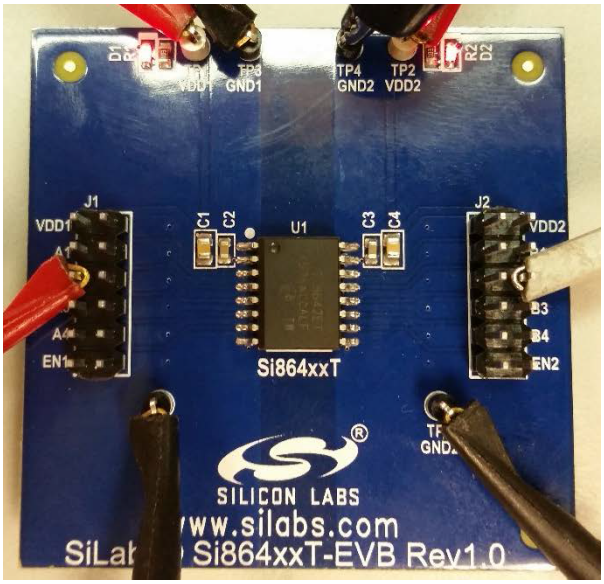


Figure 3.5. EVB Configured for Dynamic Signal Demonstration without Enable

4. Schematics

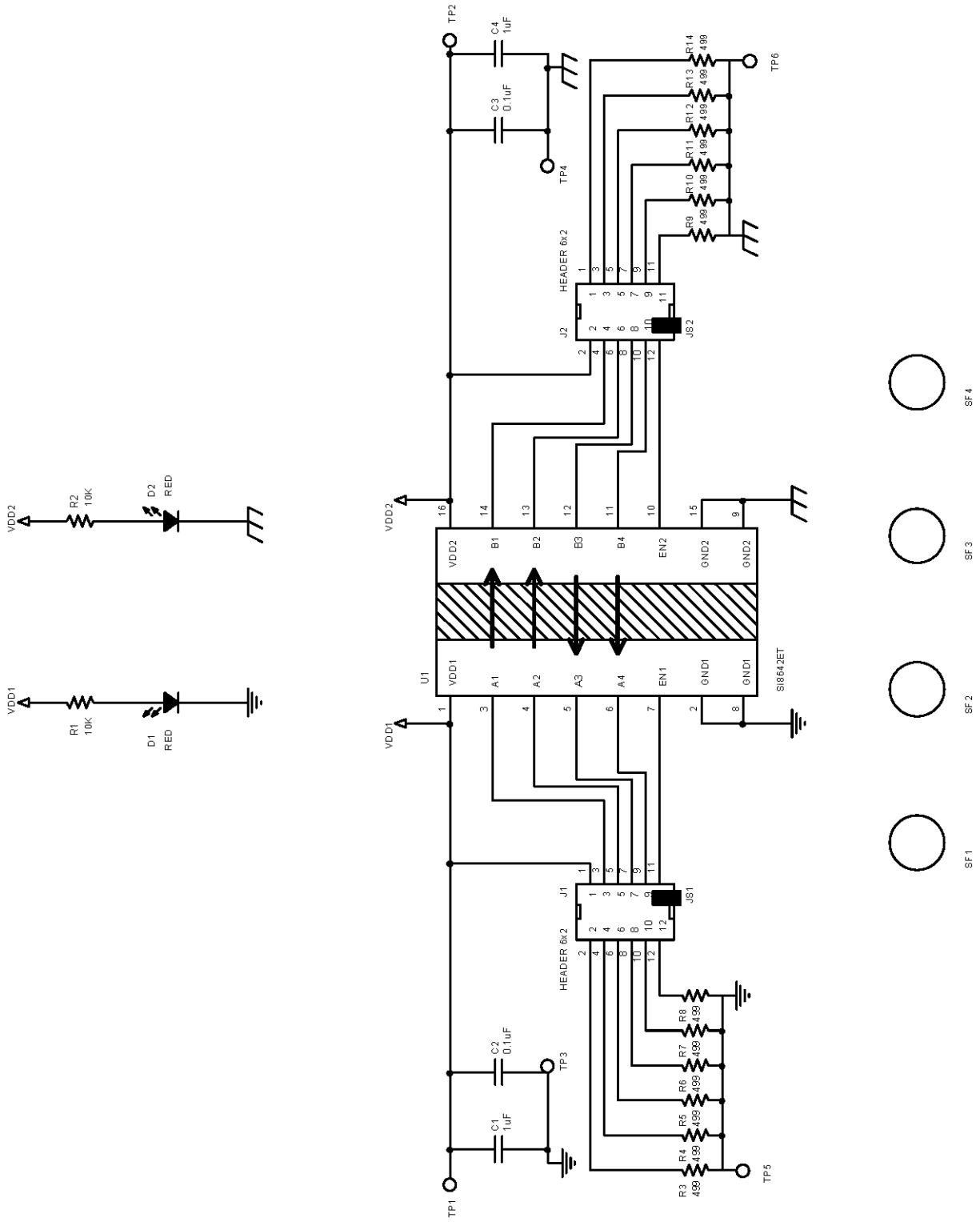


Figure 4.1. Si86xxT-EVB Schematic

5. Layout

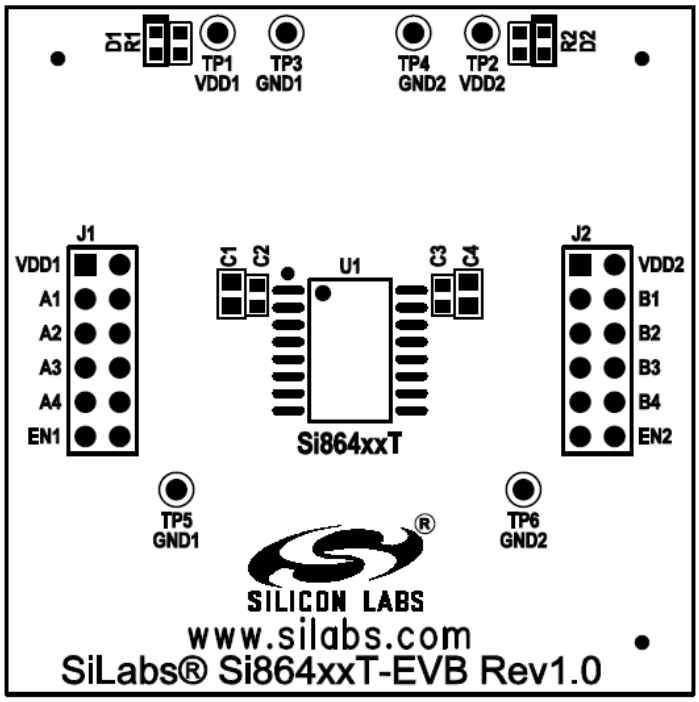


Figure 5.1. EVB — Top Silk

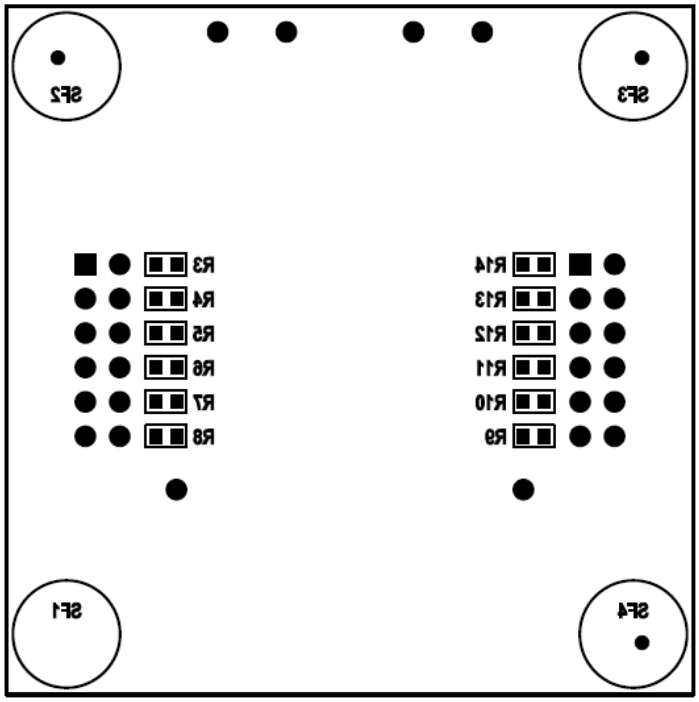


Figure 5.2. EVB — Bottom Silk

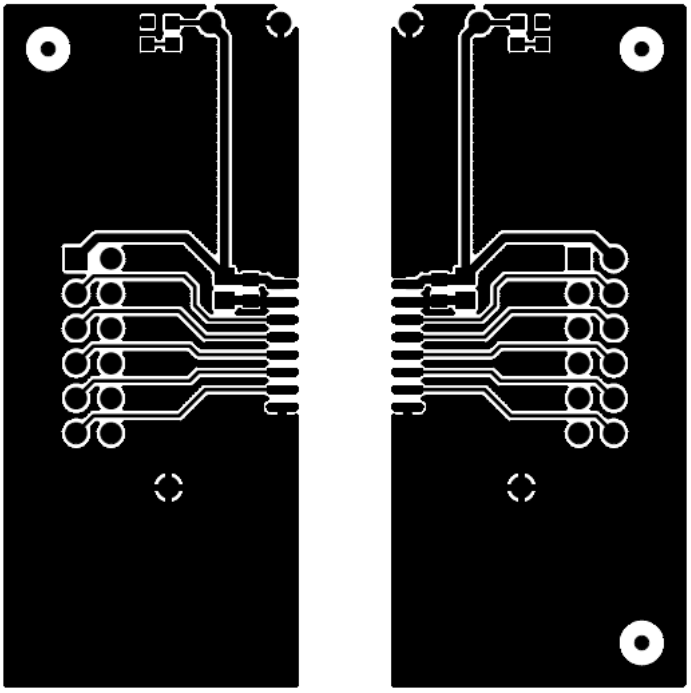


Figure 5.3. EVB — Top Copper

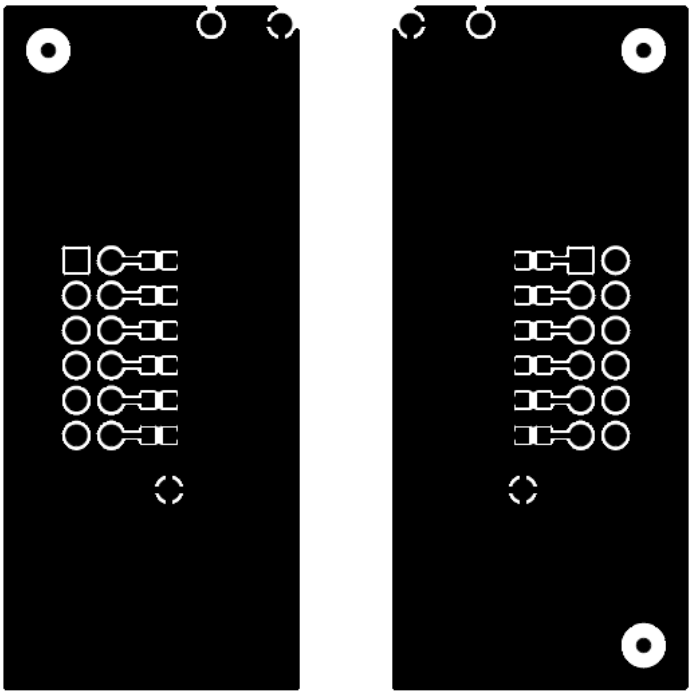


Figure 5.4. EVB — Bottom Copper

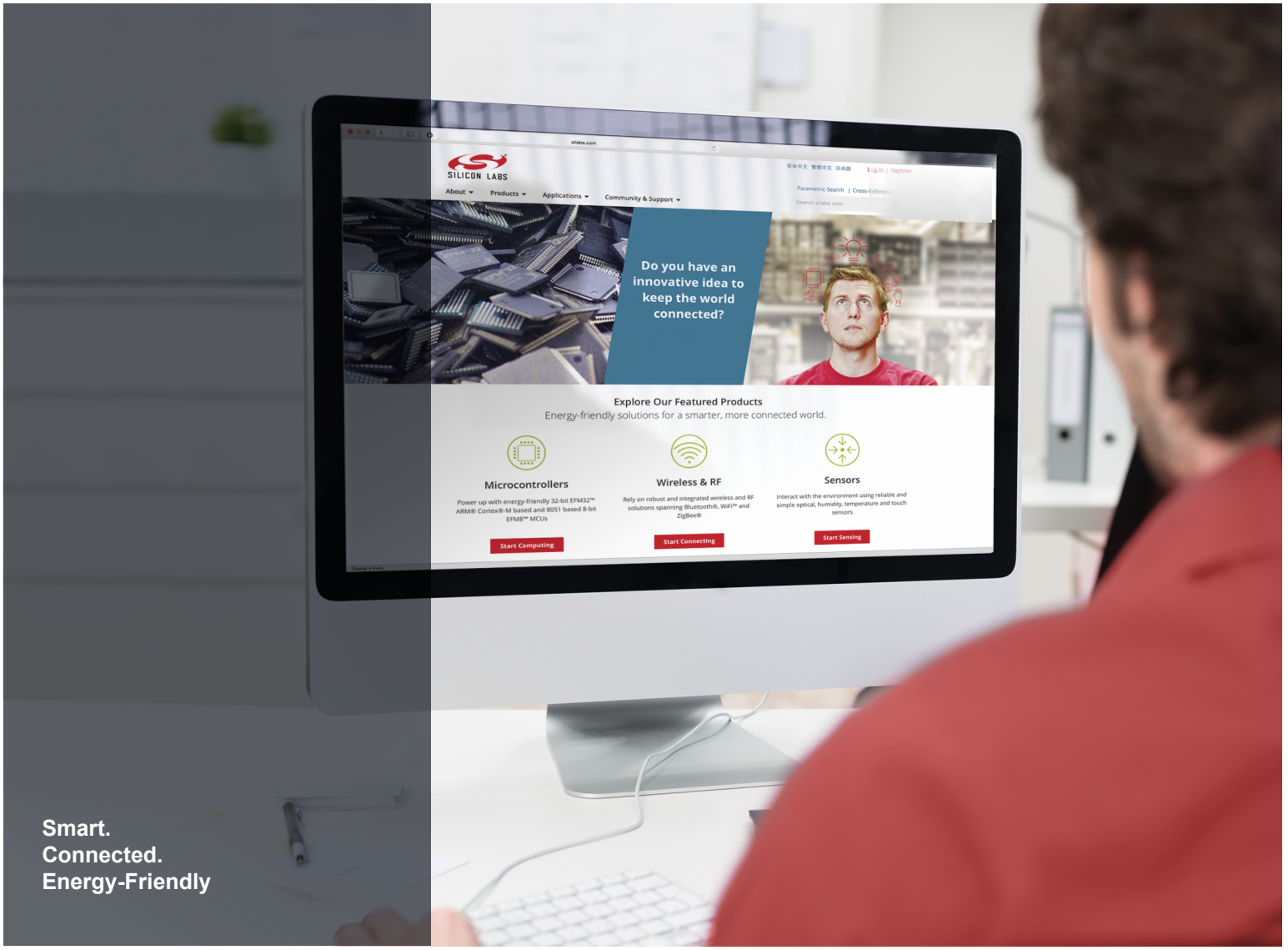
6. Bill of Materials

Table 6.1. Si86xxT-EVB Bill of Materials

Item No.	Quantity	Reference	Value	Manufacturer PN	Manufacturer
1	2	C1, C4	1 µF	CL21B105KBFNNNE	Samsung
2	2	C2, C3	0.1 µF	C0603X7R500-104K	Venkel
3	2	D1, D2	RED	LTST-C190KRKT	LITE-ON TECHNOLOGY CORP
4	2	J1, J2	HEADER 6x2	TSW-106-07-T-D	Samtec
5	2	JS1, JS2	Jumper Shunt	SNT-100-BK-T	Samtec
6	1	PCB1	Si864xxT-EVB REV 1.0	Si864xxT-EVB REV 1.0	SiLabs
7	2	R1, R2	10K	CR0603-10W-103J	Venkel
8	12	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14	499	CR0603-10W-4990F	Venkel
9	4	SF1, SF2, SF3, SF4	BUMPER	SJ61A6	3M
10	2	TP1, TP2	WHITE	151-201-RC	Kobiconn
11	4	TP3, TP4, TP5, TP6	BLACK	151-203-RC	Kobiconn
12	1	U1	Si8642ET	Si8642ET-IS	SiLabs

7. Ordering Guide

Ordering Part Number (OPN)	Description
Si864xxT-KIT	Si8642ET 4-channel 10 kV Isolator Evaluation Kit



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