

## N-channel 600 V, 0.72 $\Omega$ typ., 5.5 A MDmesh II Plus™ low $Q_g$ Power MOSFETs in TO-220FP and I<sup>2</sup>PAKFP packages

Datasheet - production data

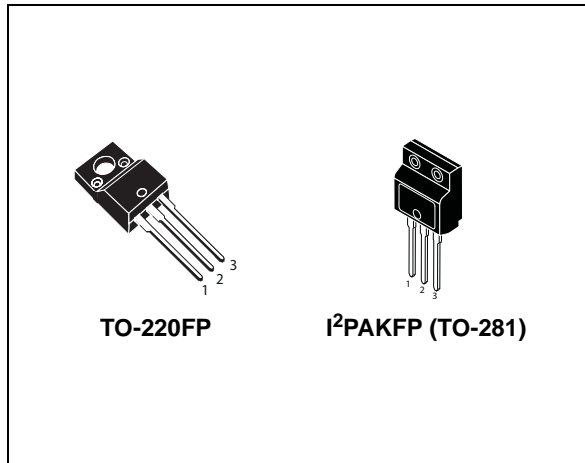
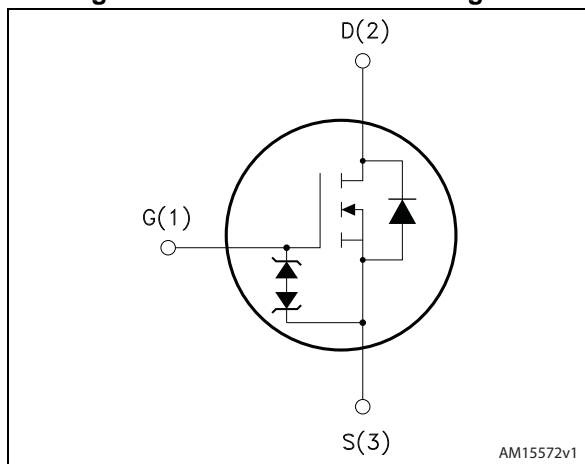


Figure 1. Internal schematic diagram



### Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STF9N60M2	650 V	0.78 $\Omega$	5.5 A
STFI9N60M2			

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF9N60M2	9N60M2	TO-220FP	Tube
STFI9N60M2		I <sup>2</sup> PAKFP	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.5 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.6 <sup>(1)</sup>	A
$I_{DM}^{(1)}$	Drain current (pulsed)	22 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	20	W
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C=25\text{ }^\circ\text{C}$ )	2500	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 5.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	6.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ ; $V_{DD}=50$ )	105	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		0.72	0.78	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	320	-	pF
$C_{oss}$	Output capacitance		-	18	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.68	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$	-	88	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	10	-	nC
$Q_{gs}$	Gate-source charge		-	2	-	nC
$Q_{gd}$	Gate-drain charge		-	5.1	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> and <a href="#">Figure 19</a> )	-	8.8	-	ns
$t_r$	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
$t_f$	Fall time		-	13.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		22	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.5 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16</a> )	-	265		ns
$Q_{rr}$	Reverse recovery charge		-	1.65		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	377		ns
$Q_{rr}$	Reverse recovery charge		-	2.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

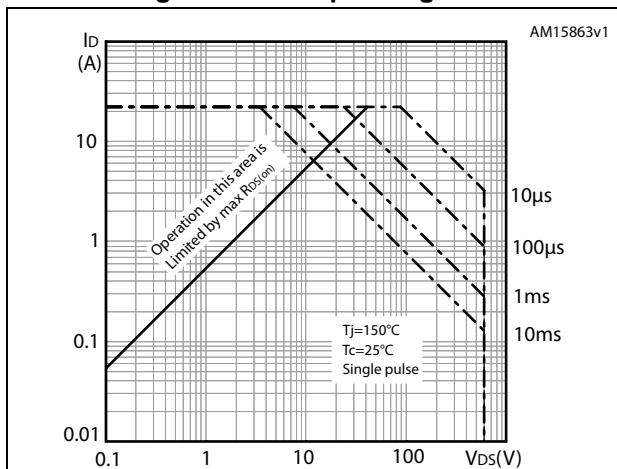


Figure 3. Thermal impedance

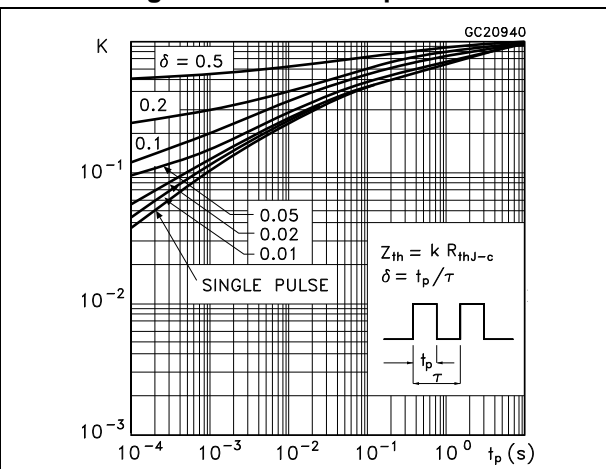


Figure 4. Output characteristics

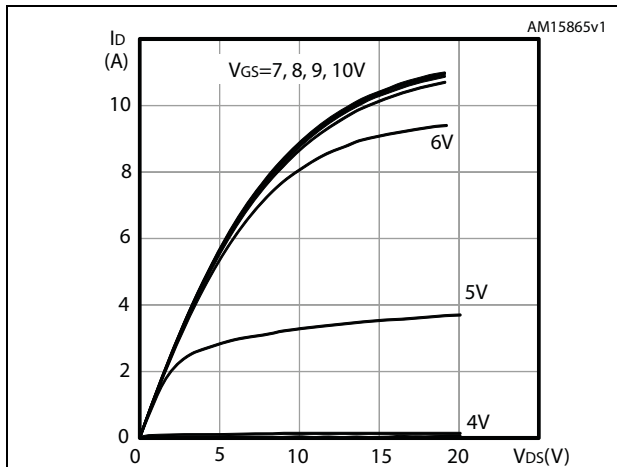


Figure 5. Transfer characteristics

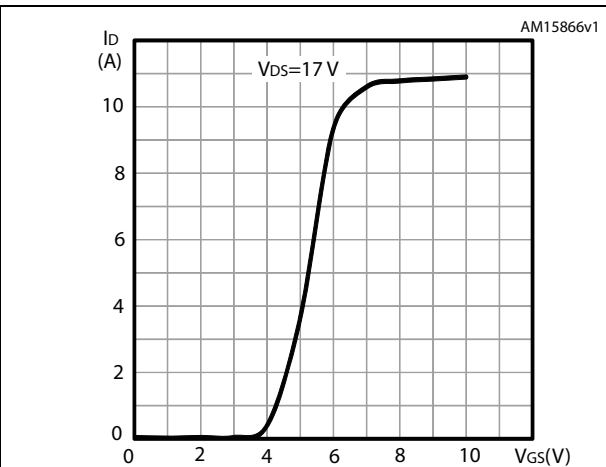


Figure 6. Gate charge vs gate-source voltage

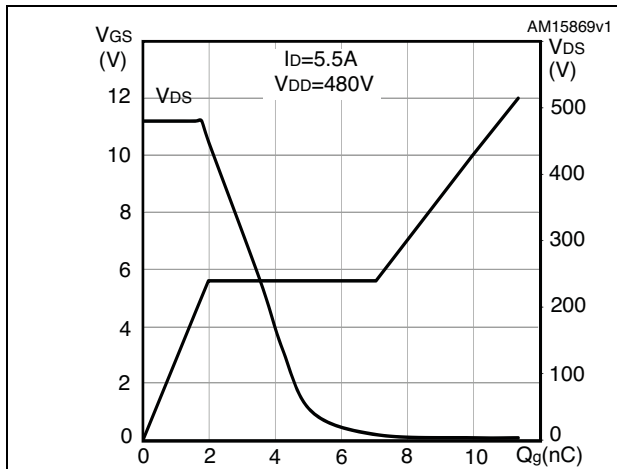


Figure 7. Static drain-source on-resistance

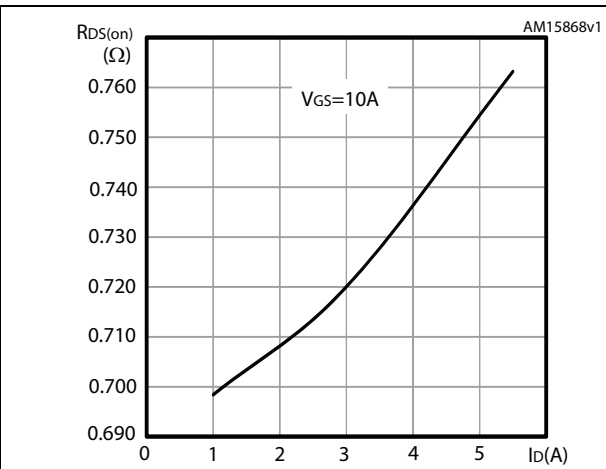


Figure 8. Capacitance variations

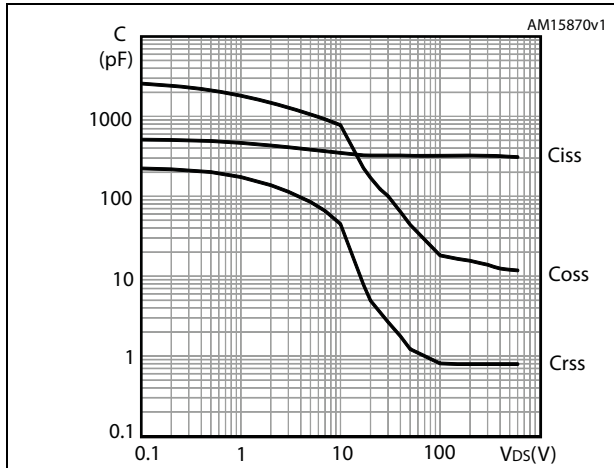


Figure 9. Output capacitance stored energy

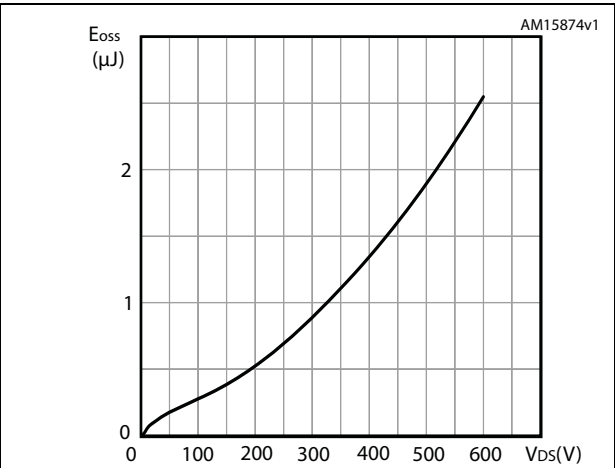


Figure 10. Normalized gate threshold voltage vs temperature

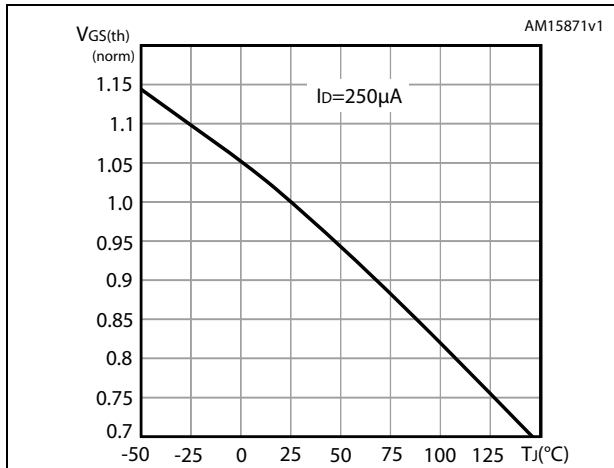


Figure 11. Normalized on-resistance vs temperature

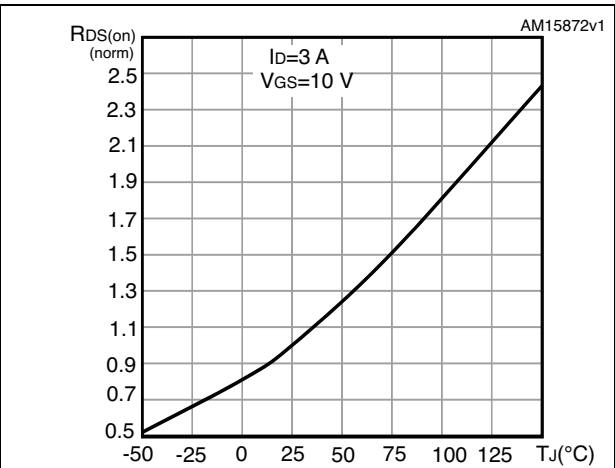


Figure 12. Source-drain diode forward characteristics

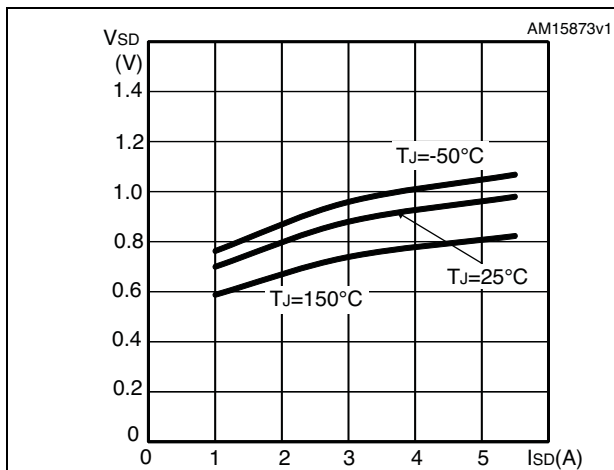
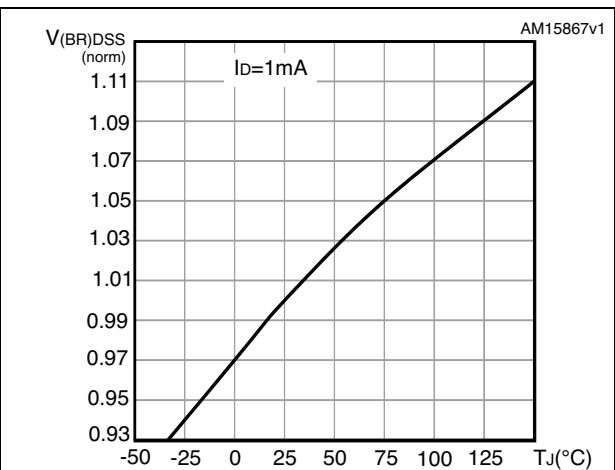


Figure 13. Normalized V(BR)DSS vs temperature



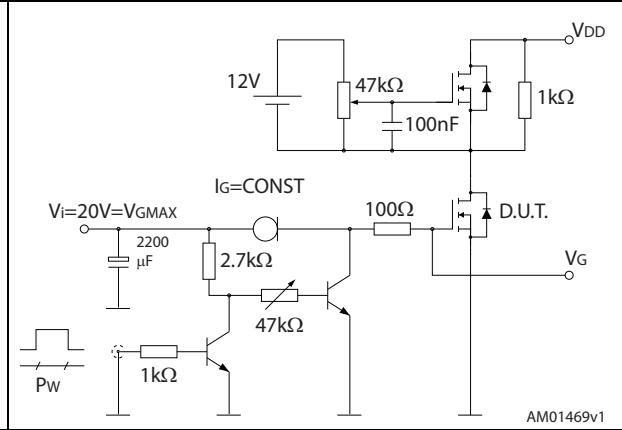
### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



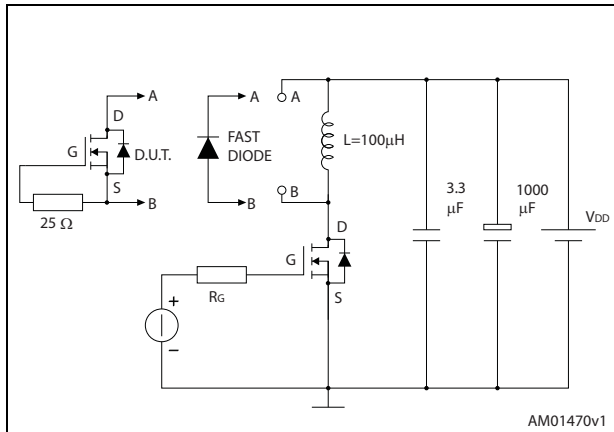
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Figure 15. Gate charge test circuit



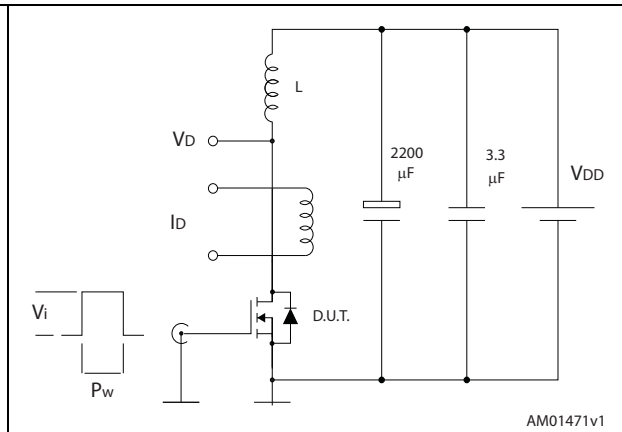
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Figure 16. Test circuit for inductive load switching and diode recovery times



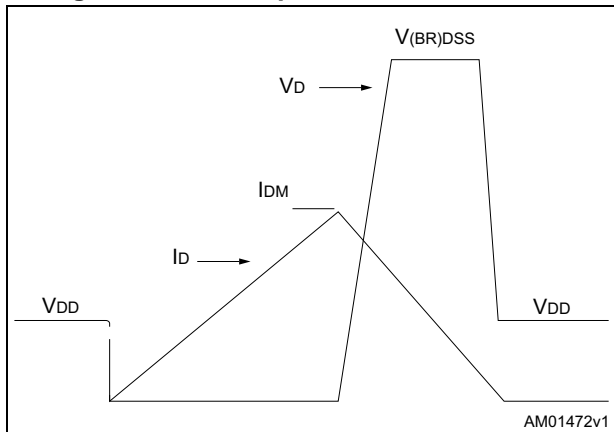
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Figure 17. Unclamped inductive load test circuit



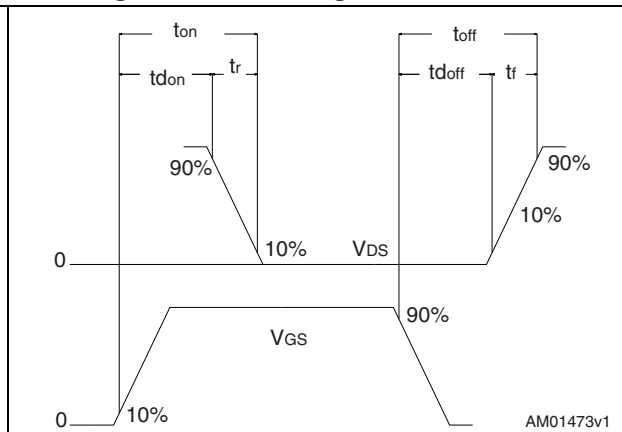
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Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

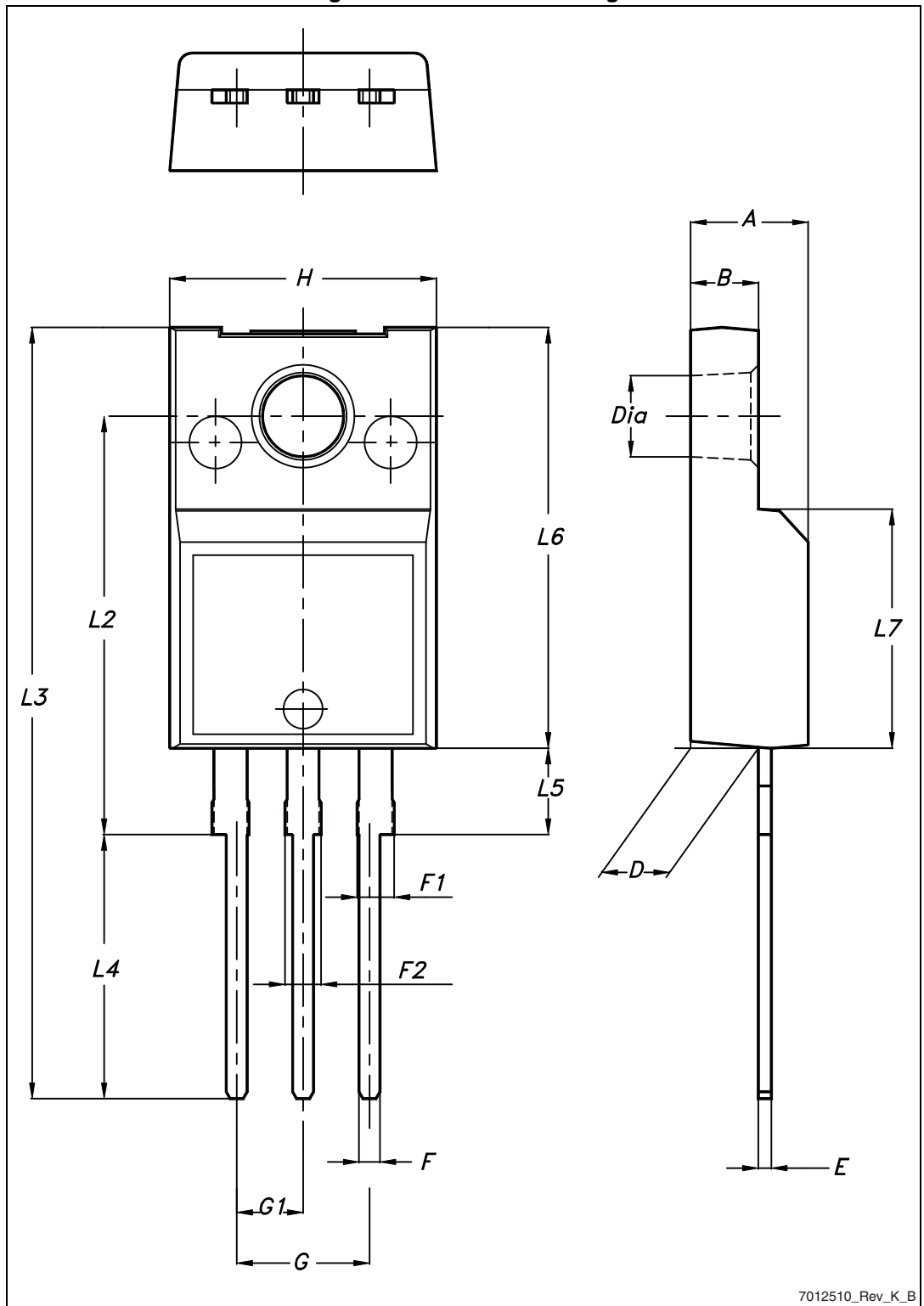


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220FP, STF9N60M2

Figure 20. TO-220FP drawing



7012510\_Rev\_K\_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## 4.2 I<sup>2</sup>PAKFP (TO-281), STF19N60M2

Figure 21. I<sup>2</sup>PAKFP (TO-281) drawing

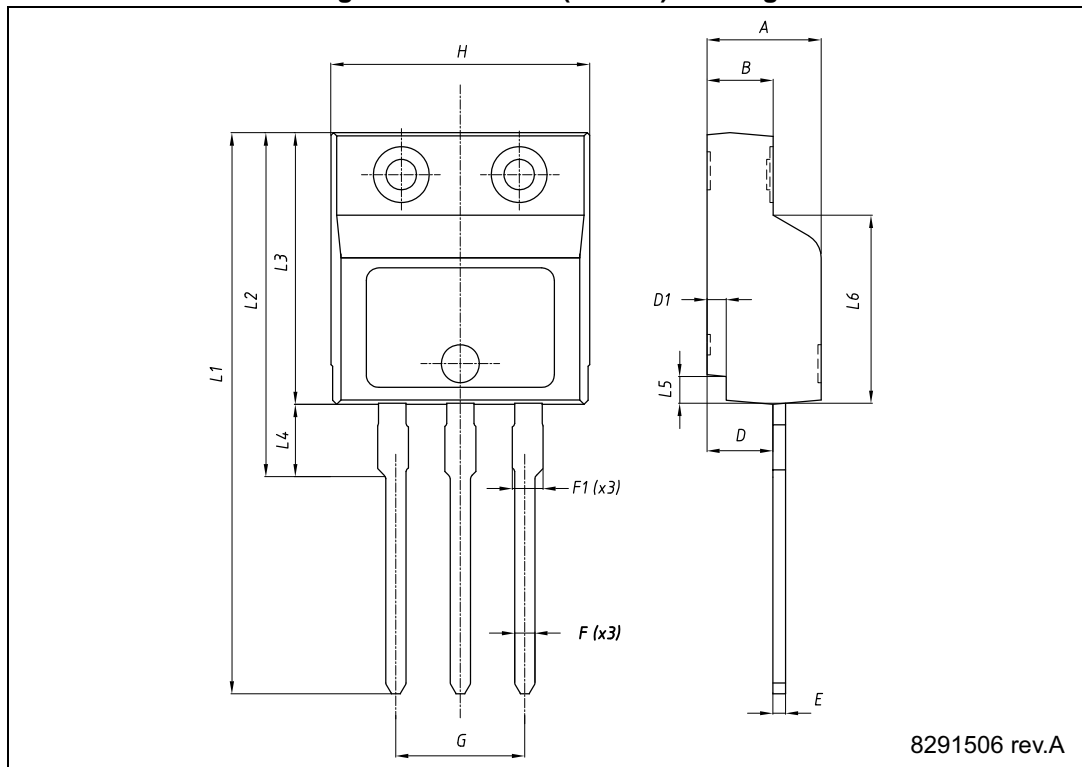


Table 10. I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

## 5 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
03-Jun-2013	1	First release. The part number was previously included in datasheet DocID024399.
10-Mar-2014	2	Added: I <sup>2</sup> PAKFP package Minor text changes

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