AP1151ADS

14V Input Adjustable Voltage LDO Regulator

1. General Description

The AP1151ADS is a low dropout linear regulator with ON/OFF control, which can supply 200mA load current. The IC is an integrated circuit with a silicon monolithic bipolar structure. The output voltage can be set from 1.3V to 14.5V by external resistors. The output capacitor is available to use a small 0.22µF ceramic capacitor. The over current, thermal and reverse bias protections are integrated, and also the package is small and thin type. The IC is designed for space saving requirements.

2. Features

- Available to use a small 0.22µF ceramic capacitor
- Dropout Voltage V_{DROP}=120mV at 100mA
- Output Current 200mA, Peak 320mA
- High Precision reference voltage 1.27V ± 20mV
- Programmable output voltage 1.3V to 13.5V
- High ripple rejection ratio 80dB at 1kHz
- Wide operating voltage range 2.1V to 14.0V
- Very low quiescent current I_{QUT}=78µA at I_{OUT}=0mA
- On/Off control (High active)
- Built-in Short circuit protection, thermal shutdown
- Built-in reverse bias over current protection
- Available very low noise application
- Very small surface mount package SOT23-6

3. Applications

- Automotive accessory equipment
- Any Electronic Equipment
- Battery Powered Systems
- Mobile Communication

4. Table of Contents

5. Block Diagram

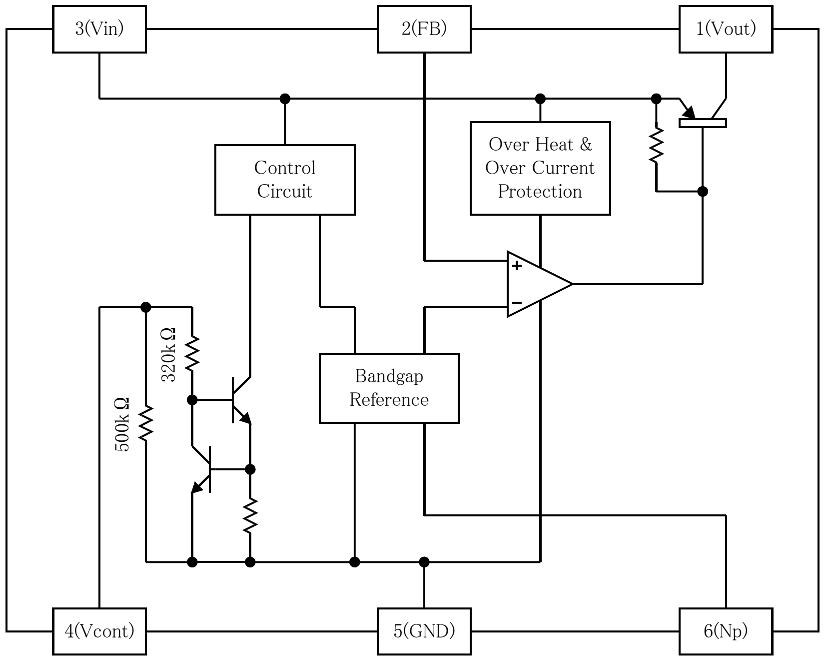


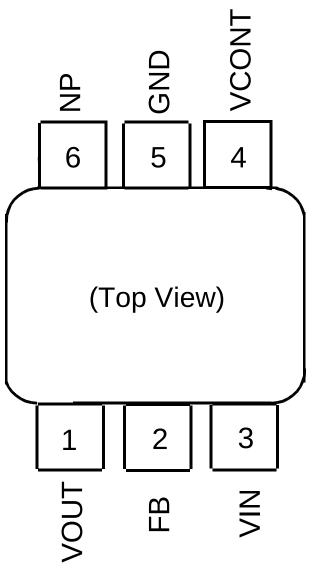
Figure 1. Block Diagram

6. Ordering Information

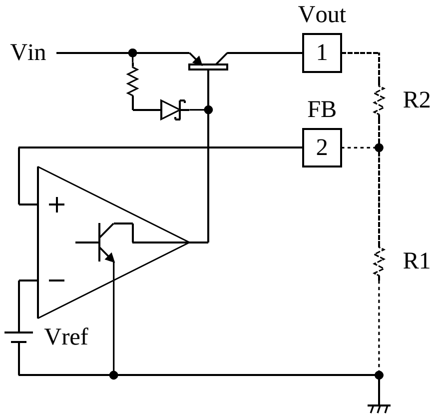
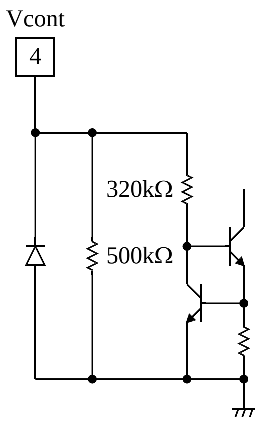
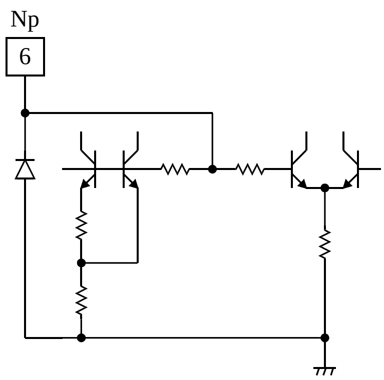
AP1151ADS Ta = -40 to 85°C SOT23-6

7. Pin Configurations and Functions

■ Pin Configurations



■ Function

Pin No.	Pin Description	Internal Equivalent Circuit	Description
1	VOUT		Output Terminal The output voltage is decided by the following formulas. $VOUT = V_{FB} \times \frac{R1+R2}{R1}$
2	FB		Feedback Terminal Connect a resistance R1 between GND, and a resistance R2 between Vout.
3	VIN		Input Terminal
4	VCONT		On/Off Control Terminal V_{CONT} > 1.8V: ON V_{CONT} < 0.35V: OFF The pull-down resister (500kΩ) is built-in.
5	GND		GND Terminal
6	NP		Noise Bypass Terminal Connect a bypass capacitor between GND.

8. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Condition
Supply Voltage	Vcc_{MAX}	-0.4	16	V	
Reverse Bias	$Vrev_{MAX}$	-0.4	6	V	$Vout_{TYP} \leq 2.0V$
		-0.4	14.5	V	$2.0V < Vout_{TYP}$
FB Pin Voltage	Vfb_{MAX}	-0.4	5	V	
Np Pin Voltage	V_{NPMAX}	-0.4	5	V	
Control Pin Voltage	$V_{CONTMAX}$	-0.4	16	V	
Junction temperature	Tj	-	150	°C	
Storage Temperature Range	T_{STG}	-55	150	°C	
Power Dissipation	P_D	-	500	mW	Mounted on PCB (Note 1)

Note 1. P_D must be decreased at rate of 4.0mW/°C for operation above 25°C. θJA= 250°C /W.

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

9. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Operating Temperature Range	Ta	-40	-	85	°C	
Operating Voltage Range	V_{OP}	2.1	-	14	V	
Output Voltage Range	Vout	1.3	-	13.5	V	

10. Electrical Characteristics

■ Electrical Characteristics of Ta=Tj=25°C

The parameters with min or max values will be guaranteed at Ta=Tj=25°C.

(Vin=4.0V, R1=51kΩ, R2=68kΩ, Vcont=1.8V, Ta=Tj=25°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
FB pin Voltage	Vfb	Iout = 5mA	1.250	1.270	1.290	V
Line Regulation	LinReg	ΔVin = 5V	-	0.0	5.0	mV
Load Regulation (Note 2)	LoaReg	Iout = 5mA ~ 100mA	-	11	27	mV
		Iout = 5mA ~ 200mA	-	26	61	mV
Dropout Voltage	Vdrop	Iout = 50mA	-	80	140	mV
		Iout = 100mA	-	120	210	mV
		Iout = 200mA	-	200	350	mV
Maximum Output Current (Note 3)	$Iout_{MAX}$	When Vout drops 0.3V	240	320	-	mA
Quiescent Current	Iq	Iout = 0mA	-	78	125	μA
Standby Current	Istandby	Vcont = 0V	-	0.0	0.1	μA
GND Pin Current	Ignd	Iout = 50mA	-	1.0	1.8	mA
Control Terminal						
Control Current	Icont	Vcont = 1.8V	-	5.0	15.0	μA
Control Voltage	Vcont	Vout ON state	1.8	-	-	V
		Vout OFF state	-	-	0.35	V
Reference Value						
Np Terminal Voltage	Vnp		-	1.27	-	V
Output Voltage / Temp.	Vo/Ta		-	35	-	ppm /°C
Output Noise Voltage	Vno	Cout=1.0μF, Cnp=0.01μF Cfb=100pF, Iout=30mA	-	34	-	μVrms
Ripple Rejection	R.R	Cout=1.0μF, Cnp=0.01μF Cfb=100pF, Iout=10mA, f=1kHz	-	80	-	dB
Rise Time	tr	Cout=1.0μF, Cnp=0.001μF Cfb=100pF Vcont : Pulse Wave (100Hz) Vcont ON → Vout×95% point	-	40	-	μs

Note 2. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at R1=51kΩ, R2=68kΩ (set at $Vout_{TYP}$=3.0V).

Note 3. The maximum output current is limited by power dissipation.

■ Electrical Characteristics of Ta=-40°C~85°C

The parameters with min or max values will be guaranteed at Ta=-40 ~ 85°C.

(Vin=4.0V, R1=51kΩ, R2=68kΩ, Vcont=1.8V, Ta= -40 ~ 85°C, unless otherwise specified.)

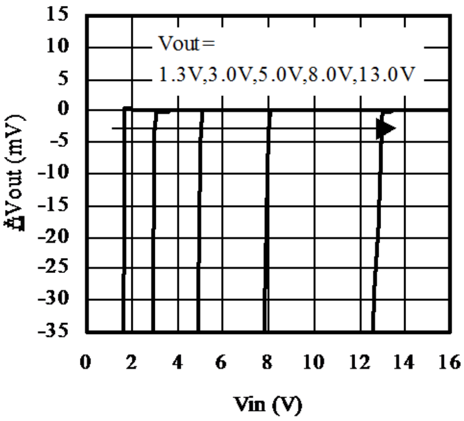
Parameter	Symbol	Condition	min	typ	max	Unit
FB pin Voltage	Vfb	Iout = 5mA	1.240	1.270	1.300	V
Line Regulation	LinReg	ΔVin = 5V	-	0.0	8.0	mV
Load Regulation (Note 4)	LoaReg	Iout = 5mA ~ 100mA	-	11	50	mV
		Iout = 5mA ~ 200mA	-	26	80	mV
Dropout Voltage	Vdrop	Iout = 50mA	-	80	180	mV
		Iout = 100mA	-	120	270	mV
		Iout = 200mA	-	200	390	mV
Maximum Output Current (Note 5)	$Iout_{MAX}$	When Vout drops 0.3V	220	320	-	mA
Quiescent Current	Iq	Iout = 0mA	-	78	150	μA
Standby Current	Istandby	Vcont = 0V	-	0.0	0.5	μA
GND Pin Current	Ignd	Iout = 50mA	-	1.0	2.2	mA
Control Terminal						
Control Current	Icont	Vcont = 1.8V	-	5.0	15.0	μA
Control Voltage	Vcont	Vout ON state	1.8	-	-	V
		Vout OFF state	-	-	0.35	V
Reference Value						
Np Terminal Voltage	Vnp		-	1.27	-	V
Output Voltage / Temp.	Vo/Ta		-	35	-	ppm /°C
Output Noise Voltage	Vno	Cout=1.0μF, Cnp=0.01μF Cfb=100pF, Iout=30mA	-	34	-	μVrms
Ripple Rejection	R.R	Cout=1.0μF, Cnp=0.01μF Cfb=100pF, Iout=10mA, f=1kHz	-	80	-	dB
Rise Time	tr	Cout=1.0μF, Cnp=0.001μF Cfb=100pF Vcont : Pulse Wave (100Hz) Vcont ON → Vout×95% point	-	40	-	μs

Note 4. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at R1=51kΩ, R2=68kΩ (set at $Vout_{TYP}$=3.0V).
Note 5. The maximum output current is limited by power dissipation.

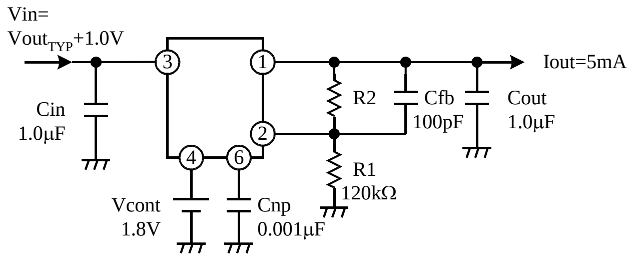
11. Description

11.1 DC Characteristics

■ Line Regulation

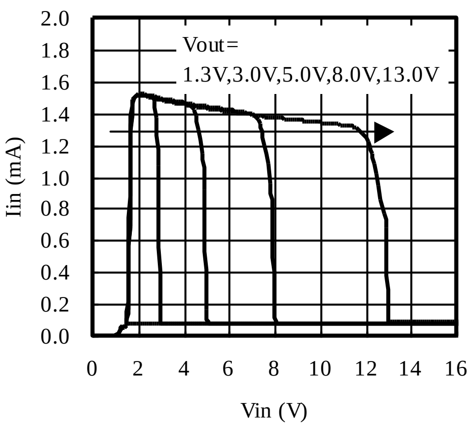


Test conditions

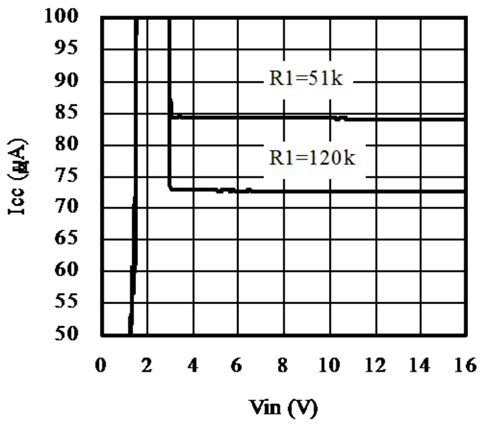


$Vout_{TYP}$= 1.3V: R1=120kΩ, R2=2.8kΩ
3.0V: R1=120kΩ, R2=163.5kΩ
5.0V: R1=120kΩ, R2=352kΩ
8.0V: R1=75kΩ, R2=397kΩ
13.0V : R1=51kΩ, R2=470kΩ

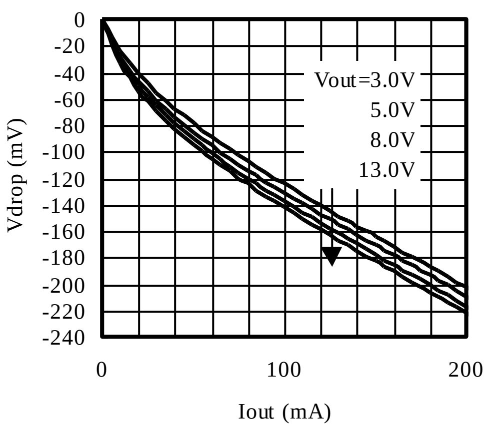
■ Iin vs Vin
Iout=0mA



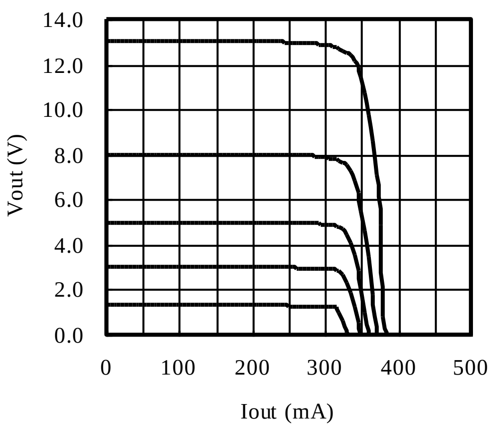
■ Supply Current
Iout=0mA, $Vout_{TYP}$=3.0V



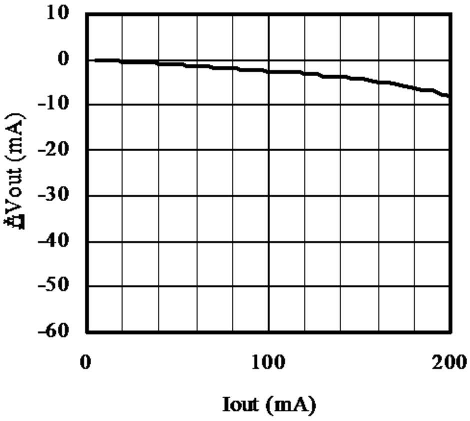
■ Dropout Voltage
2.1V ≤ $Vout_{TYP}$



■ Short Circuit Current



■ Load Regulation
$Vout_{TYP}$=1.3V



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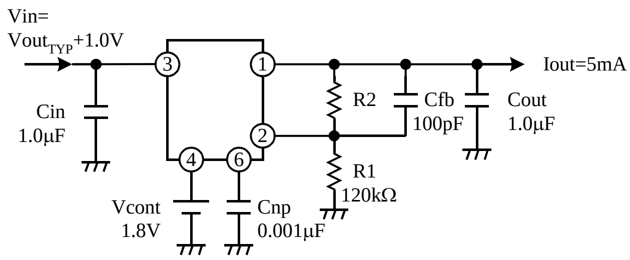
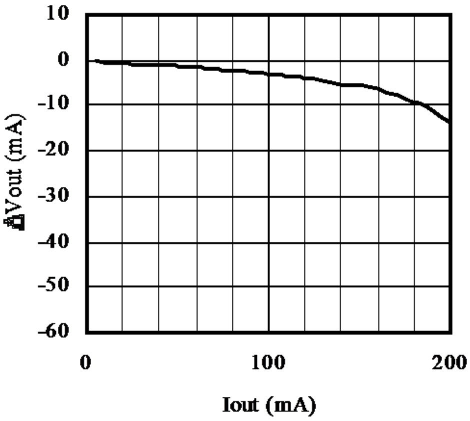
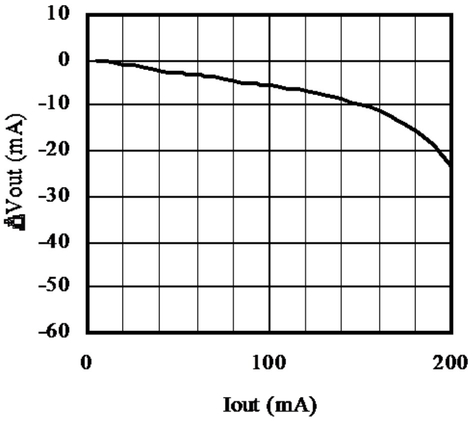


$Vout_{TYP}$= 1.3V: R1=120kΩ, R2=2.8kΩ
3.0V: R1=120kΩ, R2=163.5kΩ
5.0V: R1=120kΩ, R2=352kΩ
8.0V: R1=75kΩ, R2=397kΩ
13.0V : R1=51kΩ, R2=470kΩ

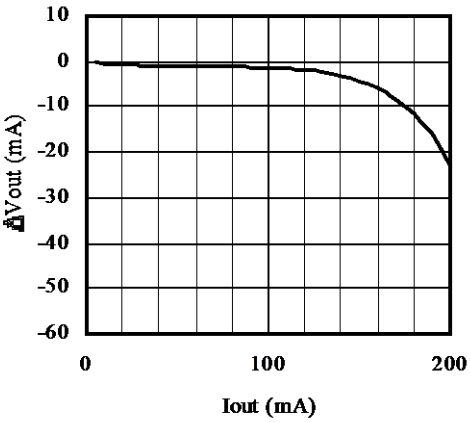
■ Load Regulation
$Vout_{TYP}$=3.0V



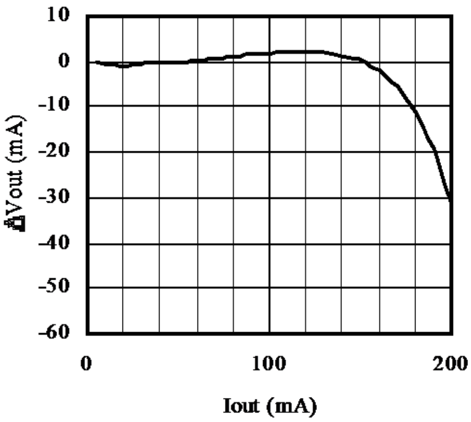
■ Load Regulation
$Vout_{TYP}$=5.0V



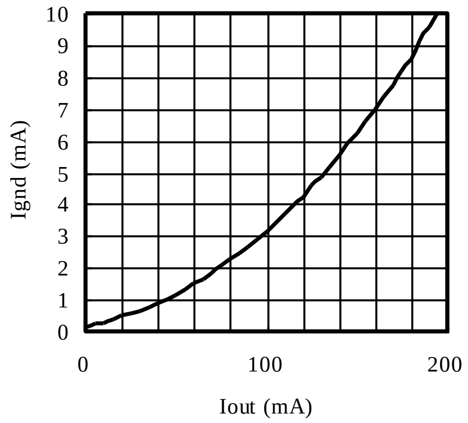
■ Load Regulation
$Vout_{TYP}$=8.0V



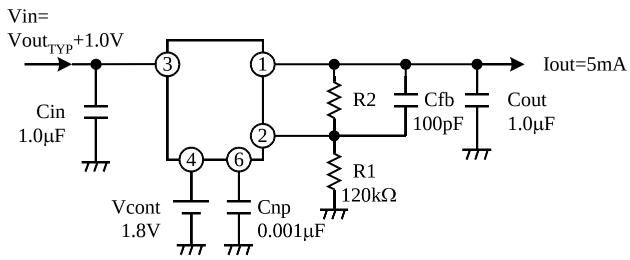
■ Load Regulation
$Vout_{TYP}$=13.0V



■ Quiescent Current

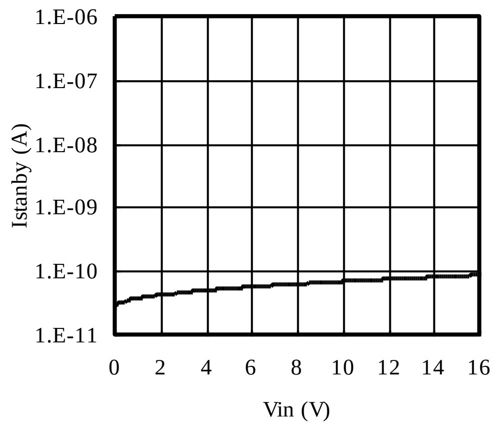


Test conditions

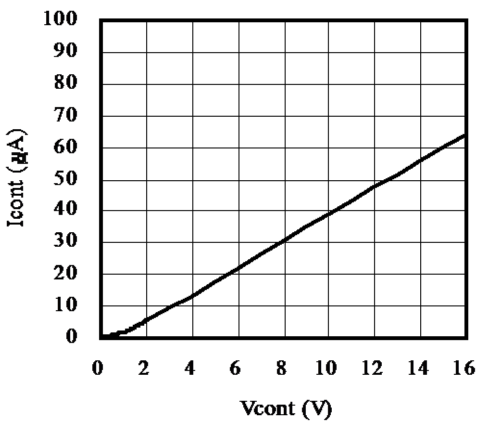


Vout$_{TYP}$= 1.3V : R1=120kΩ, R2=2.8kΩ
3.0V : R1=120kΩ, R2=163.5kΩ
5.0V : R1=120kΩ, R2=352kΩ
8.0V : R1=75kΩ, R2=397kΩ
13.0V: R1=51kΩ, R2=470kΩ

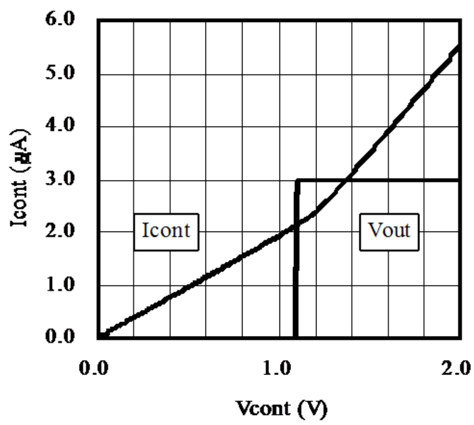
■ Standby Current (Off state)
Vcont=0V



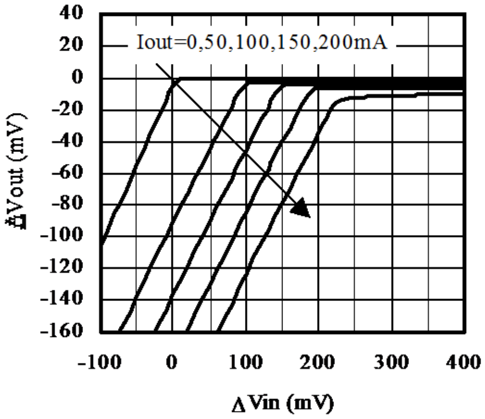
■ Control Current



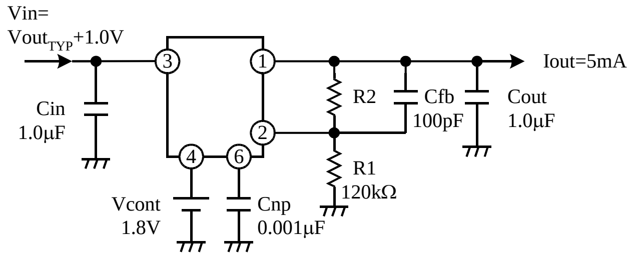
■ Control Current,ON/OFF Point



■ Vin vs Vout Regulation Point
2.1V ≤ $Vout_{TYP}$

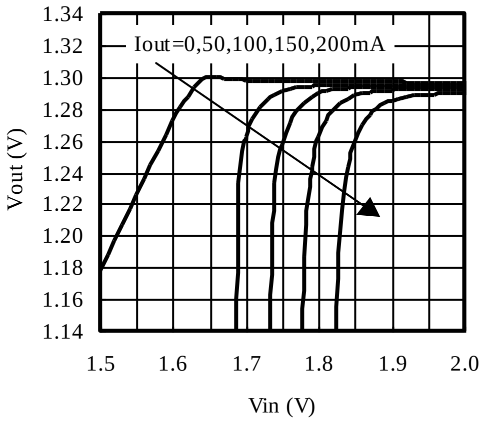


Test conditions

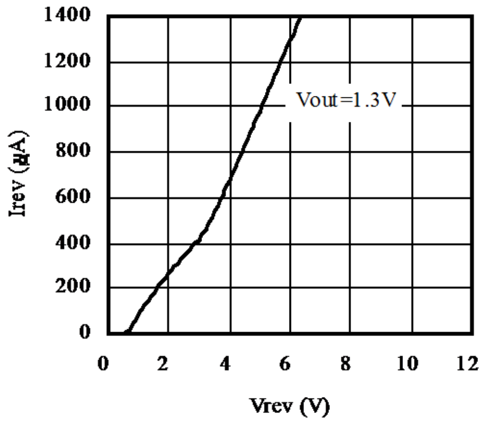


$Vout_{TYP}$= 1.3V : R1=120kΩ, R2=2.8kΩ
3.0V : R1=120kΩ, R2=163.5kΩ
5.0V : R1=120kΩ, R2=352kΩ
8.0V : R1=75kΩ, R2=397kΩ
13.0V: R1=51kΩ, R2=470kΩ

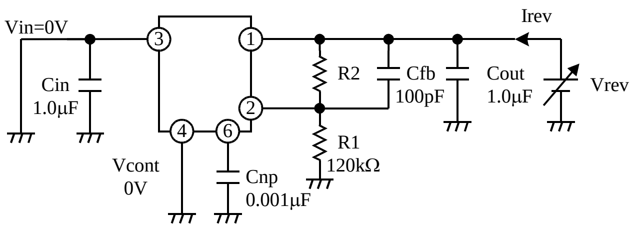
■ Vin vs Vout Regulation Point
$Vout_{TYP}$=1.3V



■ Reverse Bias Current
$Vout_{TYP}$=1.3V

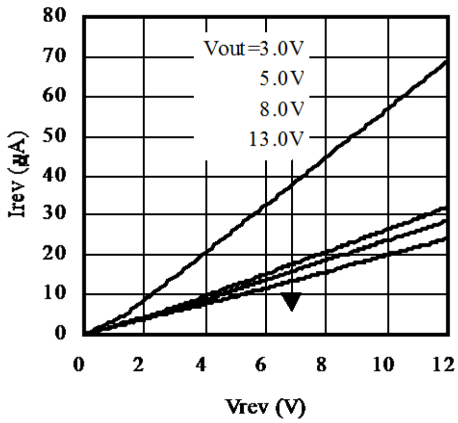


Test conditions (Reverse Bias Current)



$Vout_{TYP}$= 1.3V : R1=120kΩ, R2=2.8kΩ
3.0V : R1=120kΩ, R2=163.5kΩ
5.0V : R1=120kΩ, R2=352kΩ
8.0V : R1=75kΩ, R2=397kΩ
13.0V: R1=51kΩ, R2=470kΩ

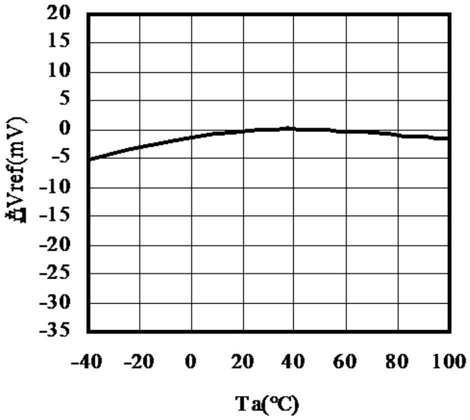
■ Reverse Bias Current
$Vout_{TYP}$=3.0V, 5.0V, 8.0V, 13.0V



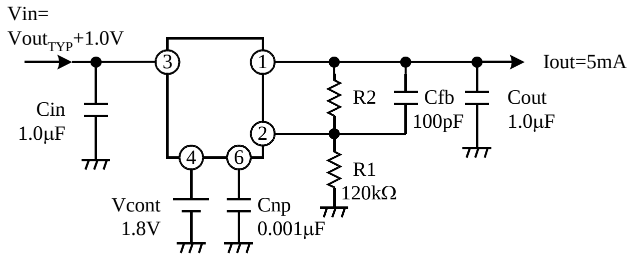
11.2 Temperature Characteristics

■ Vref

$Vref_{TYP}$=1.27V



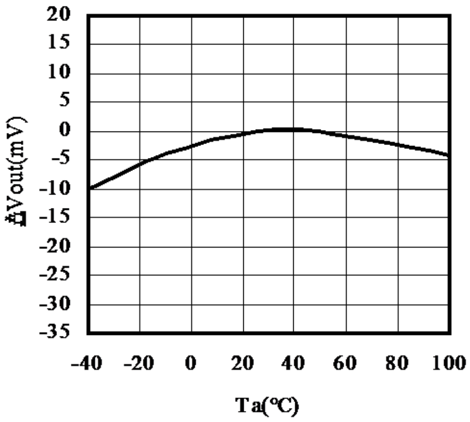
Test conditions



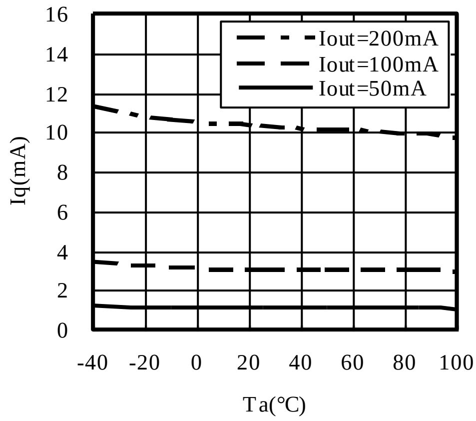
$Vout_{TYP}$=3.0V : R2=163.5kΩ

■ Vout

$Vout_{TYP}$=3.0V

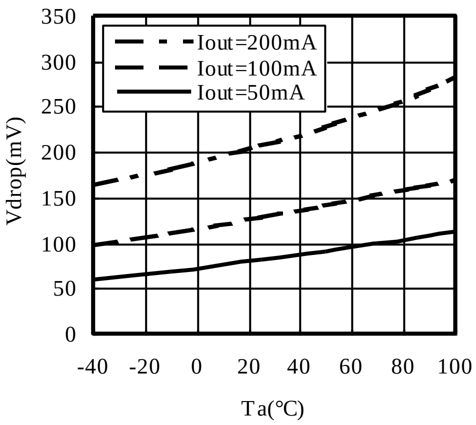


■ Quiescent Current



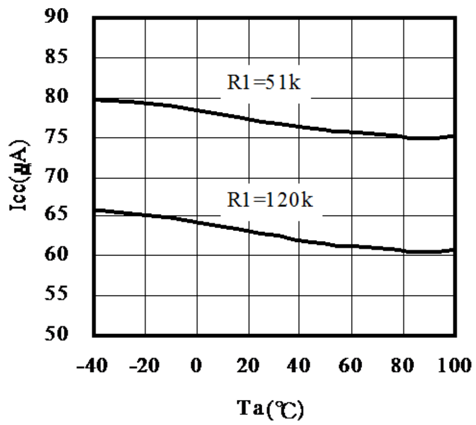
■ Dropout Voltage

2.1V ≤ $Vout_{TYP}$



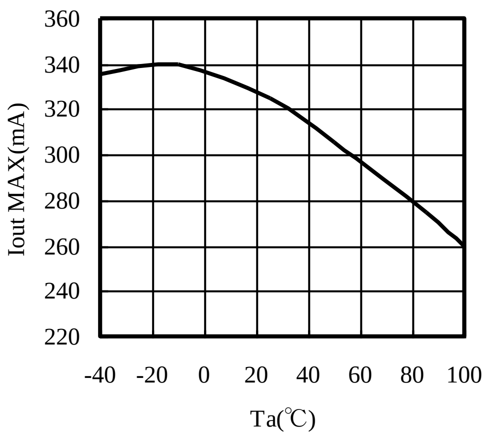
■ Supply Current

Iout=0mA



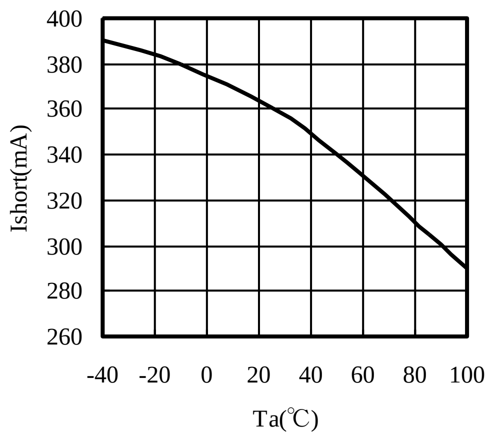
■ Maximum Output Current

Vout=Vout$_{TYP}$×90%, Ta=Tj



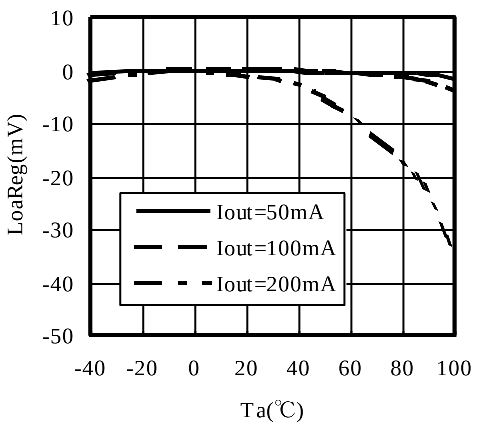
■ Short Circuit Current

Vout=0V, Ta=Tj

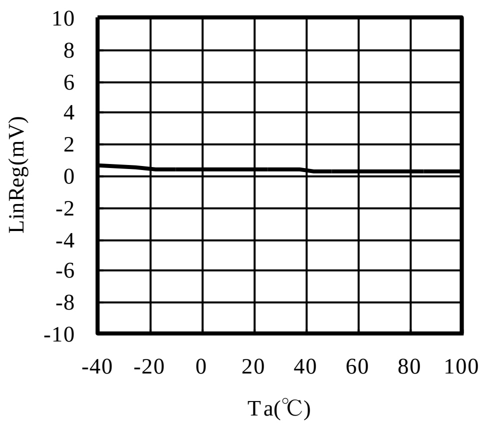


■ Load Regulation

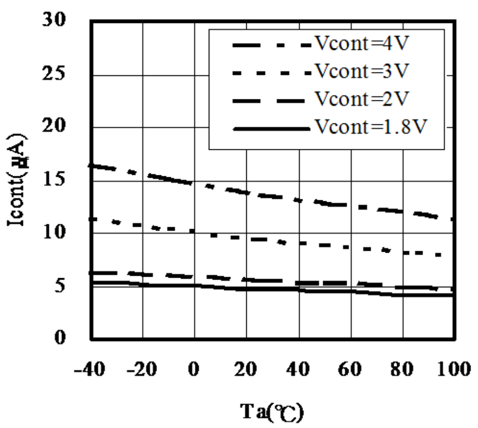
Vout$_{TYP}$=3.0V, Ta=Tj



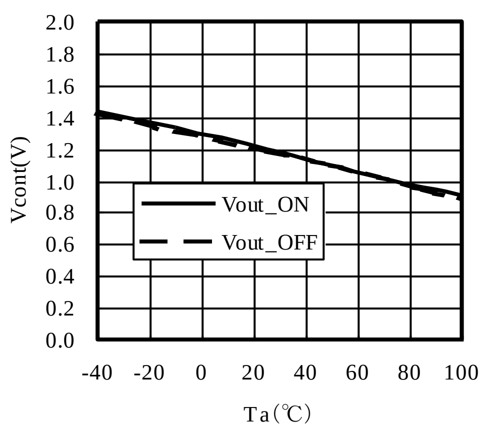
■ Line Regulation



■ Control Current



■ ON/OFF Point

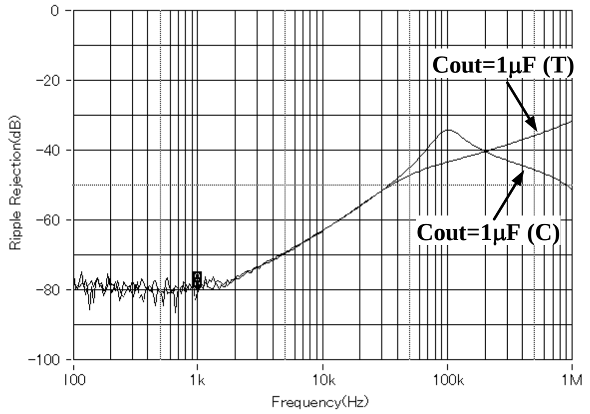


11.3 AC Characteristics

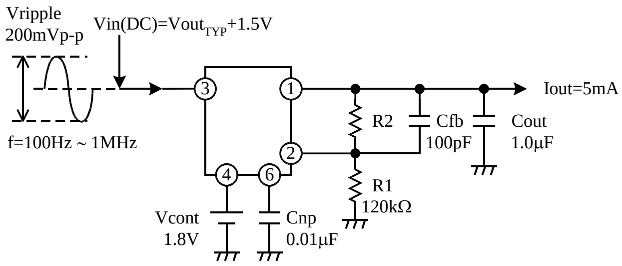
・Ripple Rejection

The ripple rejection (R.R) characteristic depends on the characteristic and the capacitance of the capacitor connected at the output side. Also it depends on the output voltage. The R.R characteristic at 50kHz or more varies greatly with the capacitor on the output side and PCB pattern. If necessary, please check stability during operation.

■ Cout=1.0μF: Ceramic (C), Tantalum (T)

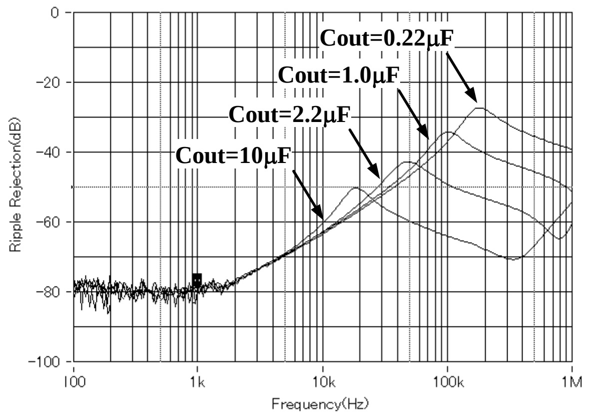


■ Test conditions

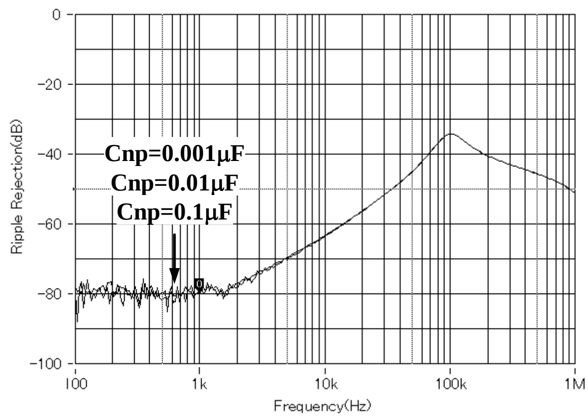


$Vout_{TYP}$=3.0V: R2=163.5kΩ

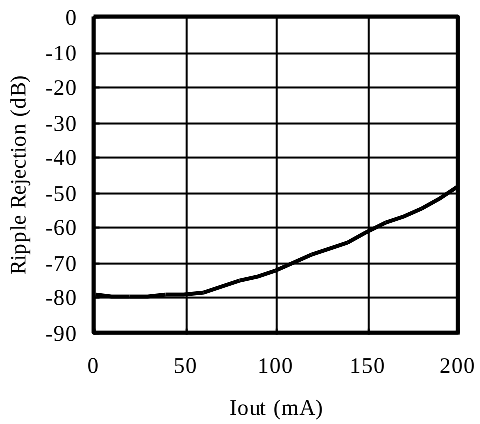
■ Cout=0.22μF, 1.0μF, 2.2μF, 10μF: Ceramic



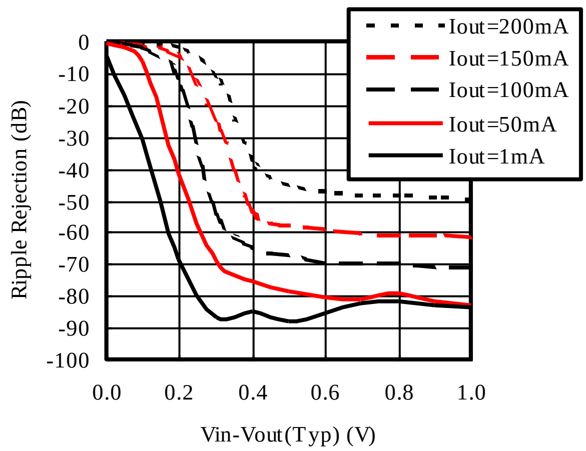
■ Cnp=0.001μF, 0.01μF, 0.1μF



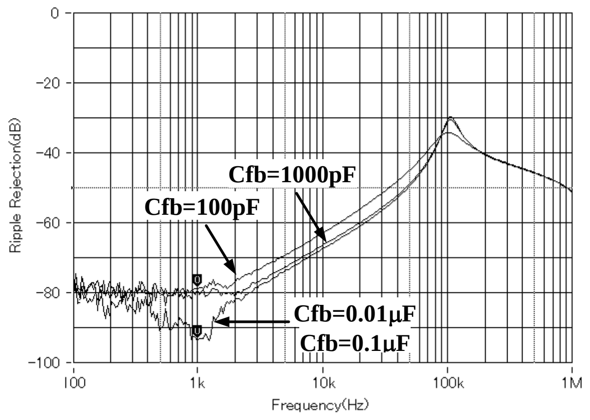
■ R.R vs. Iout: Frequency=1kHz



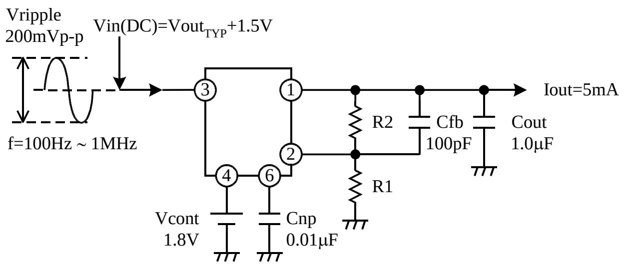
■ R.R vs. Low Vin: Frequency=1kHz



■ Cfb = 100pF, 1000pF, 0.01µF, 0.1µF
$Vout_{TYP}$=1.3V

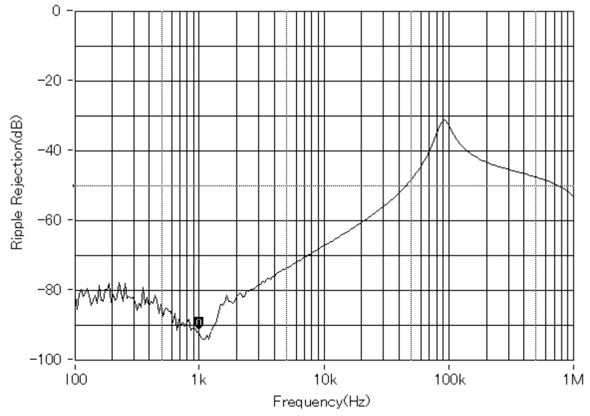


■ Test conditions

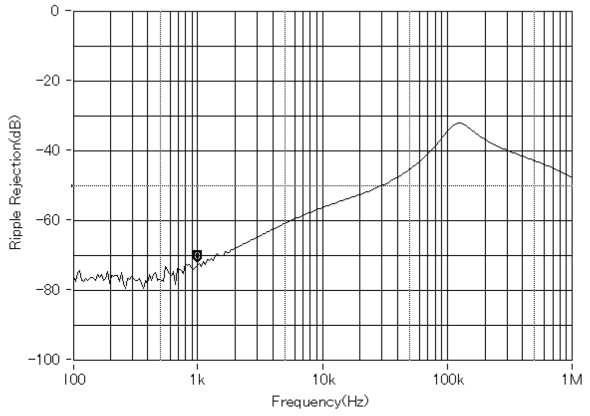


$Vout_{TYP}$= 1.3V : R1=120kΩ, R2=2.8kΩ
3.0V : R1=120kΩ, R2=163.5kΩ
5.0V : R1=120kΩ, R2=352kΩ
8.0V : R1=75kΩ, R2=397kΩ
13.0V: R1=51kΩ, R2=470kΩ

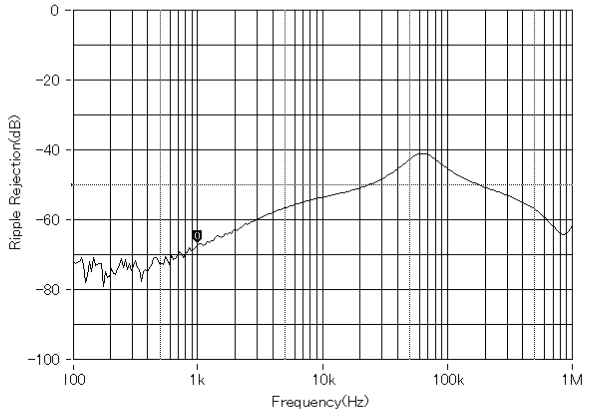
■ $Vout_{TYP}$=1.3V



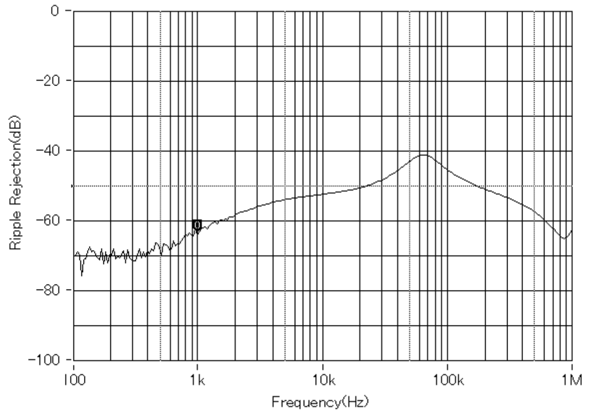
■ $Vout_{TYP}$=5.0V



■ $Vout_{TYP}$=8.0V

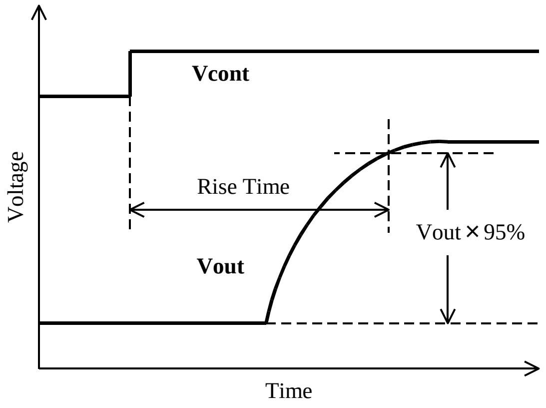


■ $Vout_{TYP}$=13V

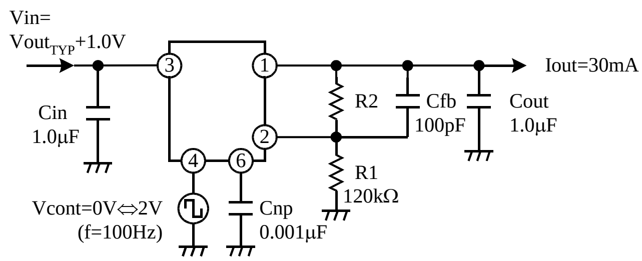


11.4 ON / OFF Transient

The rise time of the regulator depends on Cout and Cnp. The fall time depends on Cout.

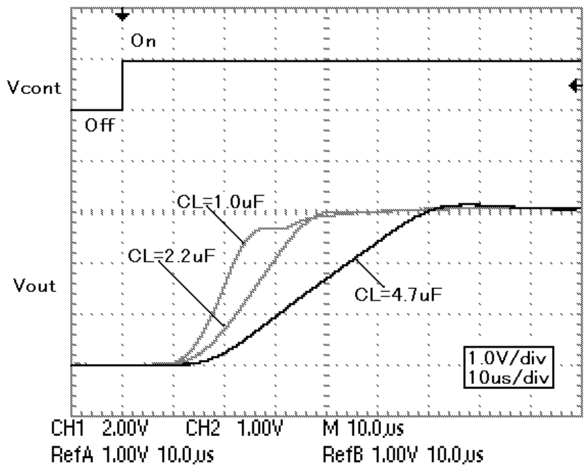


■ Test conditions

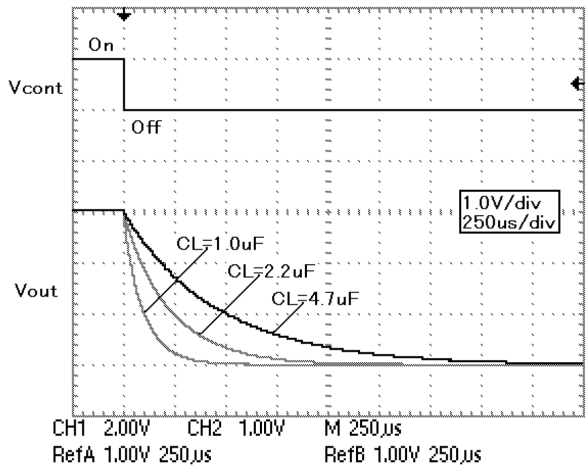


$Vout_{TYP}$=3.0V: R2=163.5kΩ

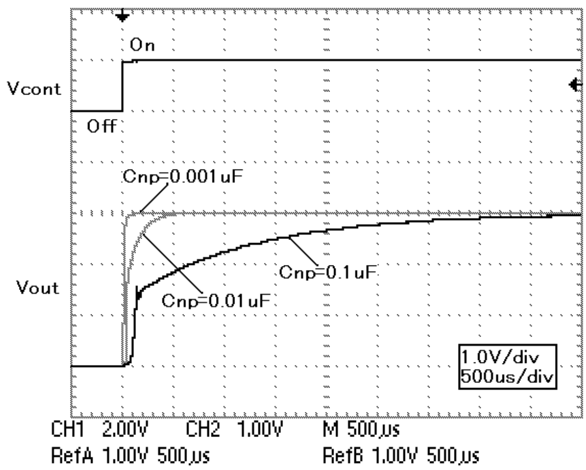
■ Cout=1.0μF, 2.2μF, 4.7μF



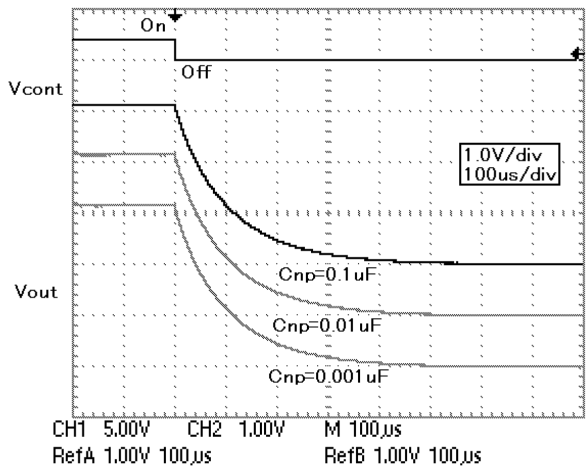
■ Cout=1.0μF, 2.2μF, 4.7μF



■ Cnp=0.001μF, 0.01μF, 0.1μF



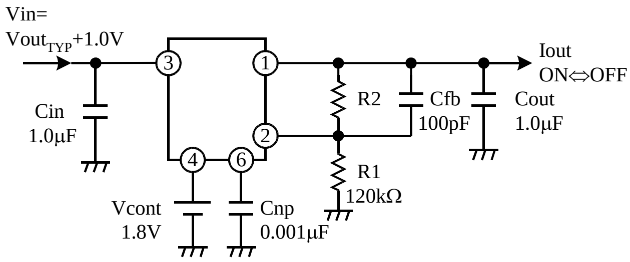
■ Cnp=0.001μF, 0.01μF, 0.1μF



11.5 LOAD Transient

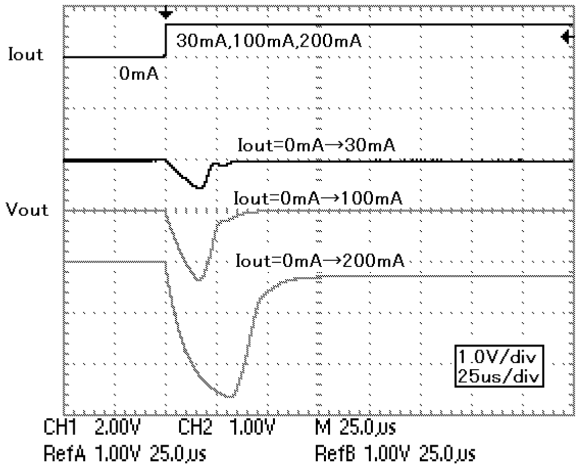
No load voltage change can be greatly improved by delivering small load current to ground. Increase the load side capacitor when the load change is fast or when there is a large current change. In addition, at no load, supplying small load current to ground can reduce the voltage change.

■ Test conditions

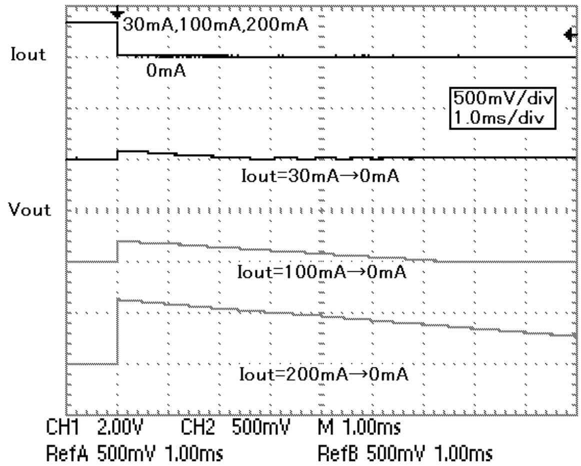


Vout$_{TYP}$=3.0V: R2=163.5kΩ

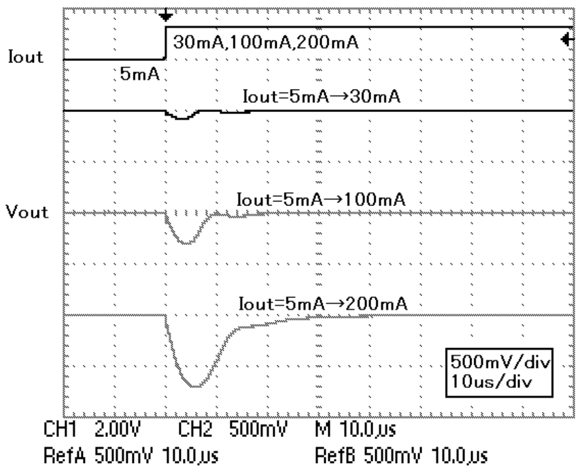
■ Iout=0→30mA, 0→100mA, 0→200mA



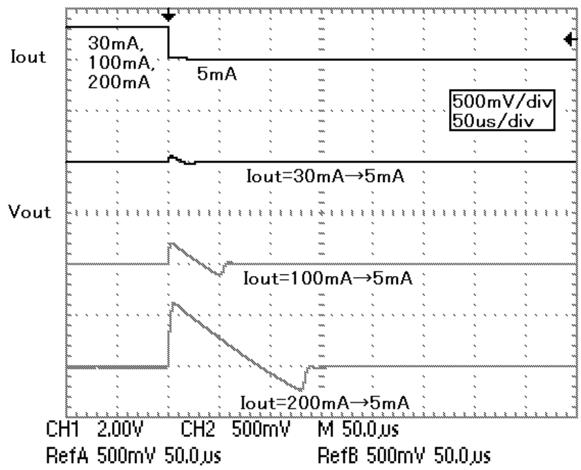
■ Iout=30→0mA, 100→0mA, 200→0mA



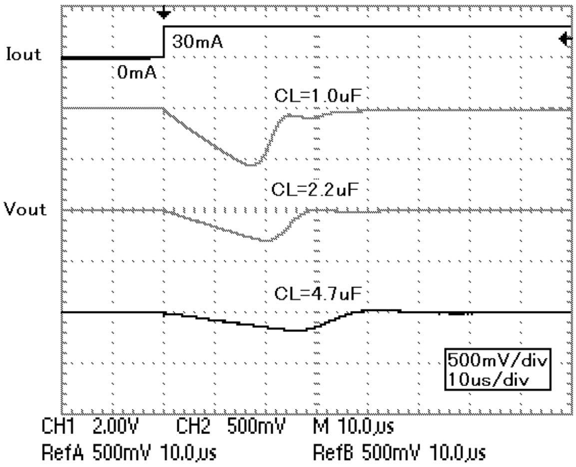
■ Iout=5→30mA, 5→100mA, 5→200mA



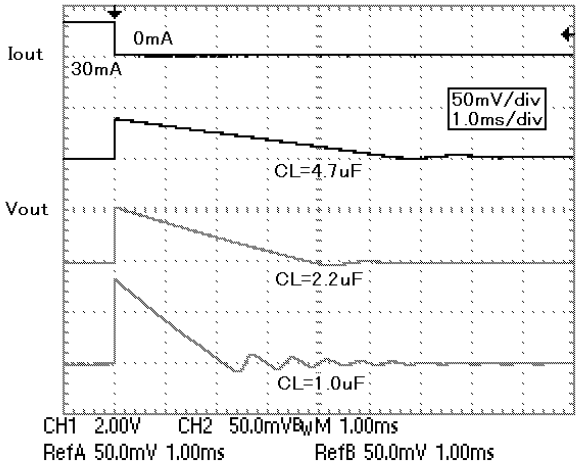
■ Iout=30→5mA, 100→5mA, 200→5mA



■ Cout=1.0μF, 2.2μF, 4.7μF: Iout=0→30mA

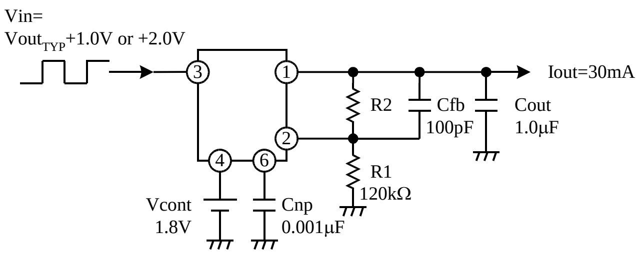


■ Cout=1.0μF, 2.2μF, 4.7μF: Iout=30→0mA



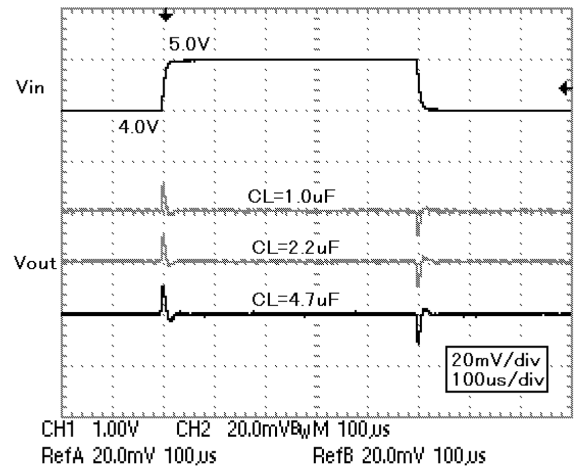
11.6 Line Transient

Test conditions

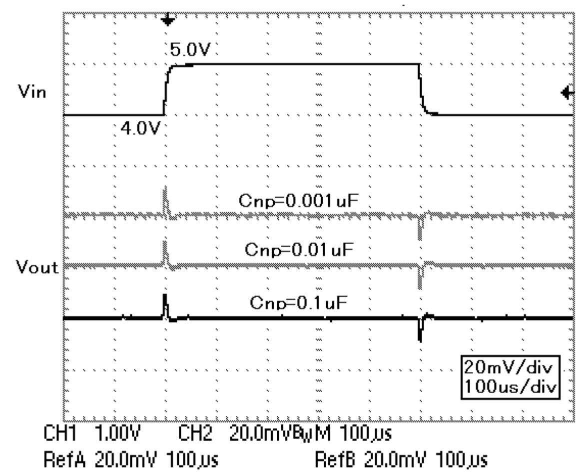


$Vout_{TYP}$=3.0V: R2=163.5kΩ

■ Cout=1.0μF, 2.2μF, 4.7μF



■ Cnp=0.001μF, 0.01μF, 0.1μF

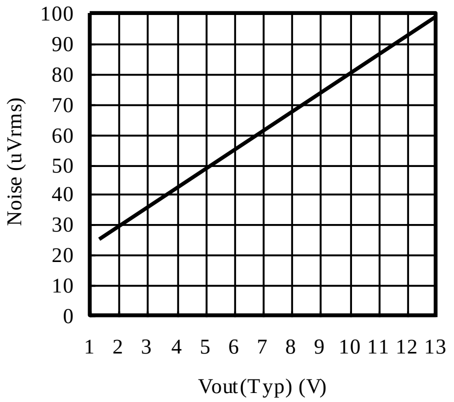


11.7 Output Noise Characteristics

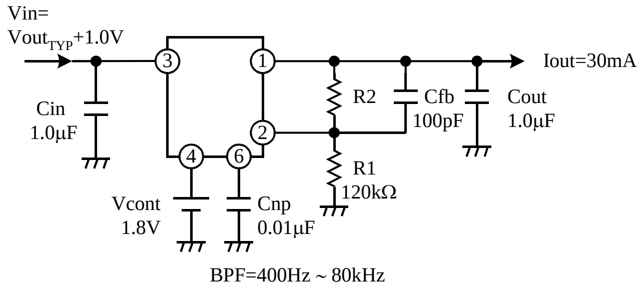
Increase Cnp to decrease the noise. The recommended Cnp capacitance is 0.01μF ~ 0.1μF. The amount of noise increases with the higher output voltages.

■ Vout vs. Noise

R1=51kΩ, R2=1.2kΩ ~ 470kΩ

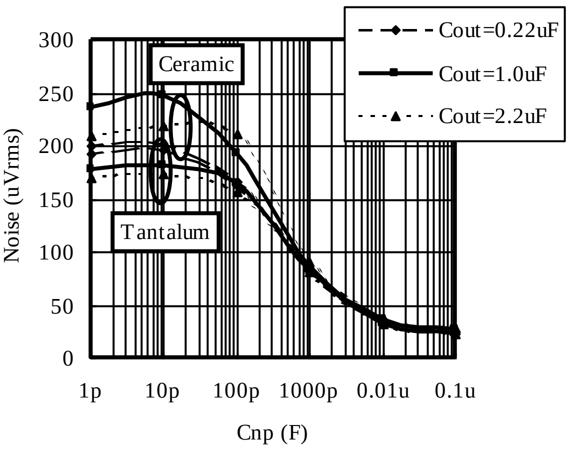


■ Test conditions

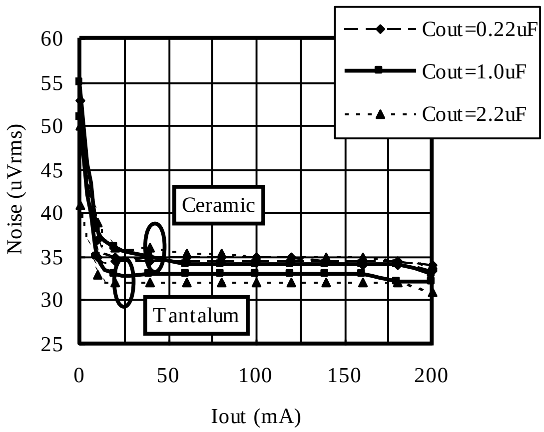


$Vout_{TYP}$=3.0V: R2=163.5kΩ

■ Cnp vs. Noise

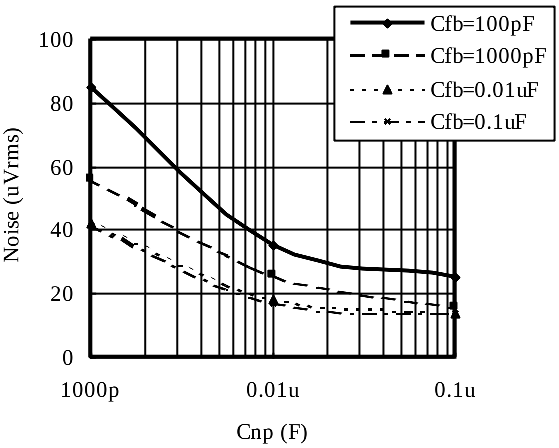


■ Iout vs. Noise



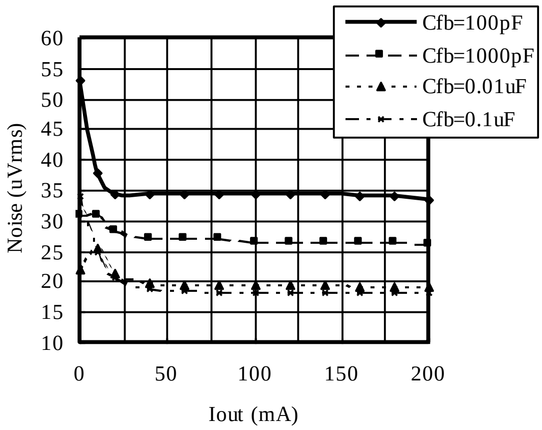
■ Cnp vs. Noise (Cout: Ceramic)

Cfb=100pF, 1000pF, 0.01μF, 0.1μF



■ Iout vs. Noise (Cout: Ceramic)

Cfb=100pF, 1000pF, 0.01μF, 0.1μF



11.8 ESR Stability

Linear regulators require input and output capacitors in order to maintain the regulator's loop stability. If a 0.22μF or larger capacitor is connected to the output side, the IC provides stable operation at any voltage (1.3V ≤ $Vout_{TYP}$ ≤ 14.5V). But due to the parts are uneven, please enlarge the capacitance as much as possible. With larger capacity, the output noise decreases more. In addition, the response to the load change, etc. can be improved. Enlarging the capacity won't damage the IC.
Moreover, increase the Cout capacitance when using the IC in the low current region and low voltage. Otherwise, the IC oscillates.
The equivalent series resistance (ESR) of the output capacitor must be in the stable operation area. However, it is recommended to use as large a value of capacitance as is practical. ESR values vary widely between ceramic and tantalum capacitors. However, tantalum capacitors are assumed to provide more ESR damping resistance, which provides greater circuit stability. This implies that a higher level of circuit stability can be obtained by using tantalum capacitors when compared to ceramic capacitors with similar values.
A recommended value of the application is as follows.

Cin=Cout≥0.22μF

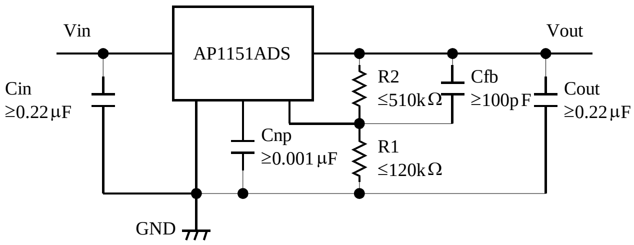
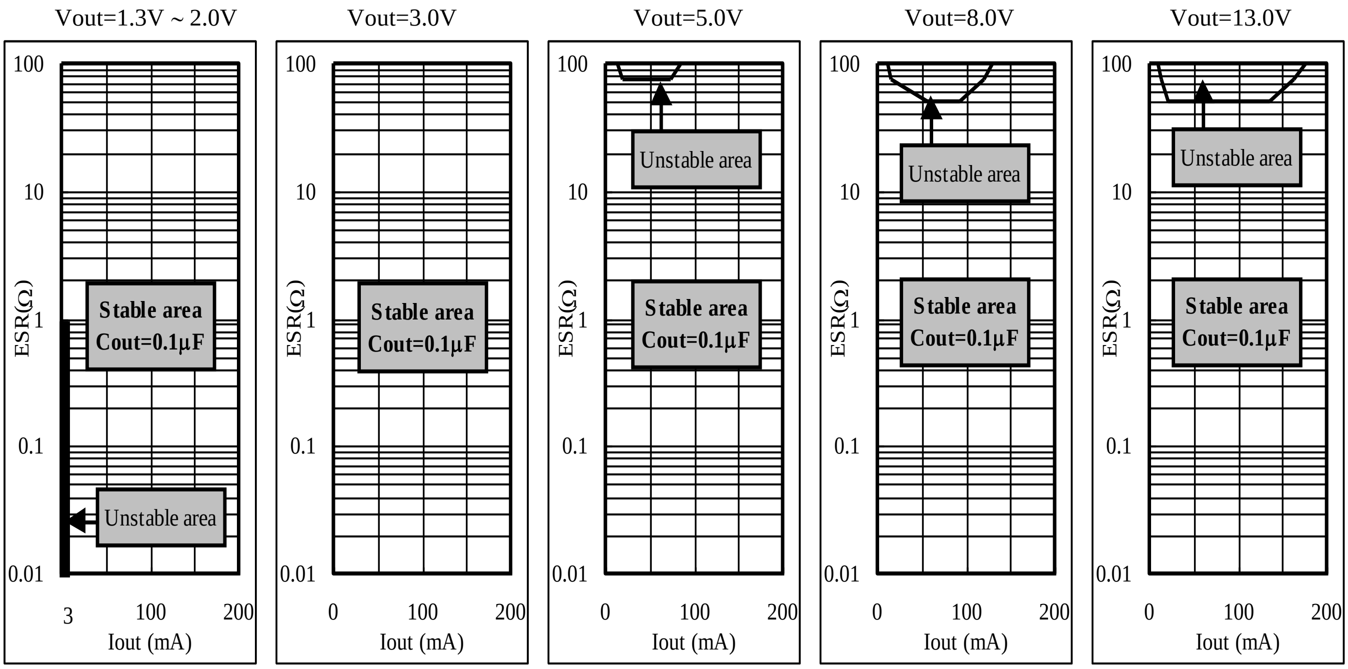


Figure 2. Recommended circuit

However, above recommended value does not satisfy some condition. Please refer to Figure 3. Select the Cout capacitance according to the condition. If the fast load transient response is necessary, increase the Cout capacitance as much as possible.



All stable: Cout≥0.22μF

Figure 3. Output Voltage, Output Current vs. Stable Operation Area

Figure 3 shows stable operation area with a ceramic capacitor of 0.1μF (excluding the low voltage and the low current region).If the capacitance is not increased in the low voltage, low current region, stable operation may not be achieved. Please select the best output capacitor according to the voltage and current used. The stability of the regulator improves if a large output side capacitor is used (the stable operation area extends.) Please use as large a capacitance as is practical.

For evaluation

Kyocera: CM05B104K10AB, CM05B224K10AB, CM105B104K16A, CM105B224K16A, CM21B225K10A

Murata: GRM36B104K10, GRM42B104K10, GRM39B104K25, GRM39B224K10, GRM39B105K6.3

Generally, a ceramic capacitor has both a temperature characteristic and a voltage characteristic. Please consider both characteristics when selecting the part. The B curves are the recommend characteristics.

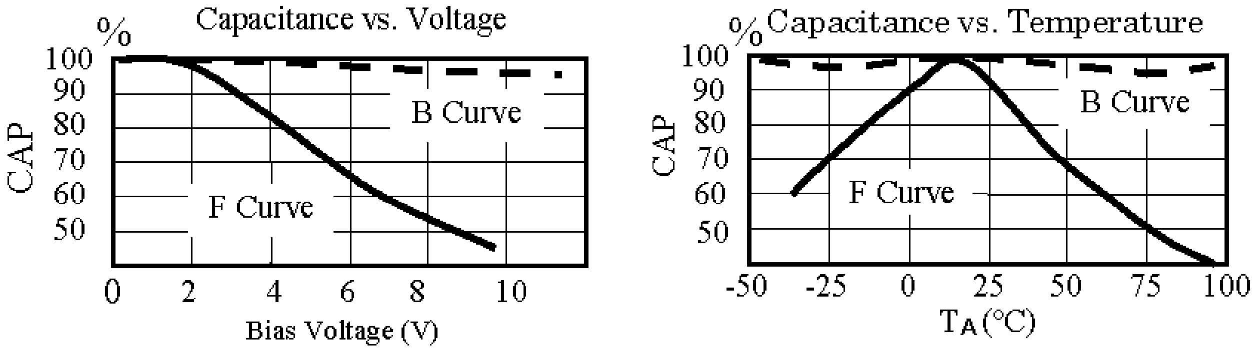


Figure 4. Ceramic Capacitance vs. Voltage, Temperature

11.9 Operating Region and Power Dissipation

The power dissipation of the device is dependent on the junction temperature. Therefore, the package dissipation is assumed to be an internal limitation. The package itself does not have enough heat radiation characteristic due to the small size. Heat runs away by mounting IC on PCB. This value changes by the material, copper pattern etc. of PCB. The overheating protection operates when there is a lot of loss inside the regulator (Ambient temperature high, heat radiation bad, etc.). The output current and the output voltage will drop when the protection circuit operates. When joint temperature (Tj) reaches the set temperature, IC stops the operation. However, operation begins at once when joint temperature (Tj) decreases.

・The thermal resistance when mounted on PCB

The chip joint temperature during operation is shown by Tj=θJA×Pd+Ta. Joint part temperature (Tj) of AP1151ADS is limited around 150°C with the overheating protection circuit. Pd is the value when the overheating protection circuit starts operation.

When you assume the ambient temperature to be 25°C,

150=θJA × Pd(W)+25

θJA × Pd=125

θJA=125/Pd (°C /W)

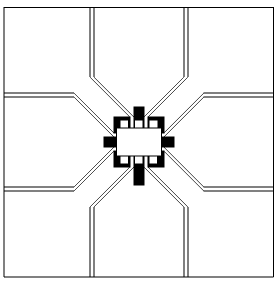


Figure 5. Example of mounting substrate

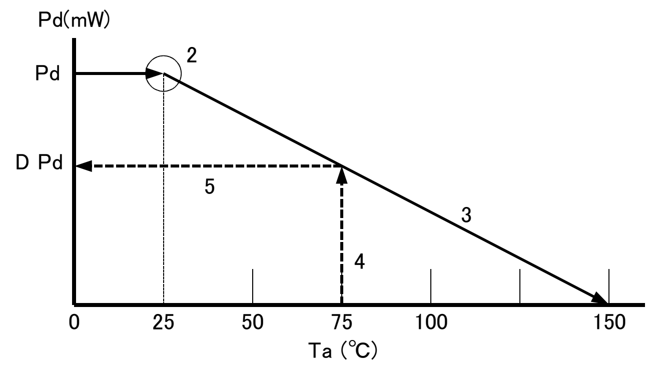
PCB Material: Two-layer glass epoxy substrate (x=30mm,y=30mm,t=1.0mm,Copper pattern thickness 35um)

・**Method of obtaining Pd easily**

Connect output terminal to GND (short circuited), and measure the input current by increasing the input voltage gradually up to 10V. The input current will reach the maximum output current, but will decrease soon according to the chip temperature rising, and will finally enter the state of thermal equilibrium (natural air cooling).The input current and the input voltage of this state will be used to calculate the Pd. When the device is mounted, mostly achieve 500mW or more.

$$Pd(mW) \cong Vin\ (V) \times Iin\ (mA)$$

The maximum output current at the highest operating temperature will be Iout ≅ DPd ÷ (Vinmax-Vout). Please use the device at low temperature with better radiation. The lower temperature provides better quality.
In the case that the power, Vin × Ishort (Short Circuit Current), becomes more than the maximum rating of its power dissipation in a moment, there is a possibility that the IC is destroyed before internal thermal protection works.



Procedure (When mounted on PCB).

1.Find Pd (Vin×Iin when the output is short-circuited).
2. Plot Pd against 25°C.
3. Connect Pd to the point corresponding to the 150°C with a straight line.
4. Pull a vertical line from the maximum operating temperature in your design (e.g., 75°C).
5. Read the value of Pd against the point at which the vertical line intersects the derating curve(DPd).
6.DPd÷(Vinmax-Vout)=Iout (at 75°C)

Figure 6. Obtaining Pd

11.10 ON/OFF Control

It is recommended to turn the regulator off when the circuit following the regulator is not operating. A design with small electric power loss can be implemented. Because the control current is small, it is possible to control it directly by CMOS logic.

Table 1.

Control Terminal Voltage (Vcont)	ON/OFF State
Vcont > 1.8V	ON
Vcont < 0.35V	OFF

11.11 Noise Bypass

The noise characteristics depend on the capacitance on the Np terminal.A standard value is Cnp=0.001μF. Increase Cnp in a design with important output noise requirements. The IC will not be damaged even the capacitor value is increased. The on/off switching speed changes depending on the Np terminal capacitance. The switching speed slows when the capacitance is large.

11.12 The notes of the evaluation when output terminal is short-circuit to GND

By the resonance phenomenon by Cout (C ingredient) and the short circuit line (L ingredient), which are attached to an output terminal, an output terminal changes with minus potential. In order that Parasitism Tr arises within Bip IC, and a latch rise phenomenon may occur within IC when the worst if it goes into an output terminal's minus side, it results in damage by fire (white smoke) and breakage of a package. ($f_0 = 1 / 2\pi\sqrt{(L\ C)}$)

The above-mentioned resonance phenomenon appears notably in a ceramic capacitor with the small ESR value, etc. A resonance phenomenon can be reduced by connecting resistance (around 2ohms or more) in series with a short circuit line. Thereby, the latch rise phenomenon within IC can be prevented.

Generally, when using tantalum or large electrolysis capacitor, the influence of resonance phenomenon can be reduced due to the large ESR (2ohms or more)

12. Definition of term

■ Relating Characteristic

Each characteristic will be measured in a short period not to be influenced by joint temperature (Tj).

・**Output voltage (Vout)**

The output voltage is specified with Vin= $Vout_{TYP}$+1V and Iout=5mA

・**Output current (Iout)**

Output current, which can be used continuously (It is the range where overheating protection of the IC does not operate.)

・**Maximum output current ($Iout_{MAX}$)**

The rated output current is specified under the condition where the output voltage drops 90% by increasing the output current, compared to the value specified at Vin=$Vout_{TYP}$+1V.

・**Dropout voltage (Vdrop)**

It is an I/O voltage difference when the circuit stops the stable operation by decreasing the input voltage. It is measured when the output voltage drops 100mV from its nominal value by decreasing the input voltage gradually.

・**Line Regulation (LinReg)**

It is the fluctuations of the output voltage value when the input voltage is changed.

・**Load Regulation (LoaReg)**

It is the fluctuations of the output voltage value when the input voltage is assumed to be $Vout_{TYP}$ +1V, and the load current is changed.

・**Ripple Rejection (R.R)**

Ripple rejection is the ability of the regulator to attenuate the ripple content of the input voltage at the output. It is measured with the condition of Vin=Vout+1.5V. Ripple rejection is the ratio of the ripple content between the output vs. input and is expressed in dB.

・**Standby current (Istandby)**

It is an input current, which flows to the control terminal, when the IC is turned off.

■ Relating Protection Circuit

・**Over Current Protection**

It is a function to protect the IC by limiting the output current when excessive current flows to IC, such as the output is connected to GND, etc.

・**Thermal Protection**

It protects the IC not to exceed the permissible power consumption of the package in case of large power loss inside the regulator.

The output is turned off when the chip reaches around 150°C, but it turns on again when the temperature of the chip decreases.

・**Reverse Voltage Protection**

Reverse voltage protection prevents damage due to the output voltage being higher than the input voltage. This fault condition can occur when the output capacitor remains charged and the input is reduced to zero, or when an external voltage higher than the input voltage is applied to the output side. Generally, a LDO regulator has a diode in the input direction from an output. If an input falls from an output in an input-GND short circuit etc. and this diode turns on, current will flow for an input terminal from an output terminal. In the case of excessive current, IC may break. In order to prevent this, it is necessary to connect an Schottky Diode etc. outside. This product is equipped with reverse bias over-current prevention, and excessive current does not flow in to IC. Therefore, no need to connect diode outside.

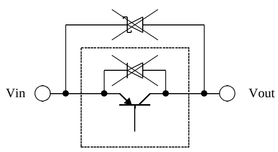
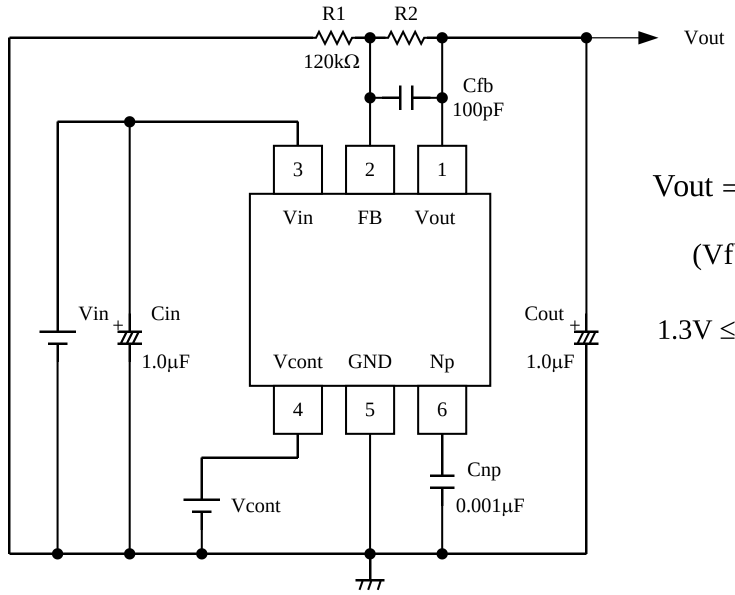


Figure 7.

13. Recommended External Circuits

■External Circuit



$$Vout = Vfb \times \frac{R1 + R2}{R1}$$

$$(Vfb_{TYP} = 1.27V)$$

$$1.3V \le Vout_{TYP} \le 13.0V$$

Figure 8. External Circuit

Note 6. In the actual application, either ceramic or tantalum capacitor can be used for Cin and Cout. Please set feedback resistor R1, R2 current larger than 10μA. The current is fixed withVfb/R1.Please fix R2 value smaller than 510kΩ. In case of high output voltage, please adjust R1 value in order to make R2 value smaller than 510kΩ.Recommended capacitor value for Cfb: Cfb=100pF

■Test Circuit

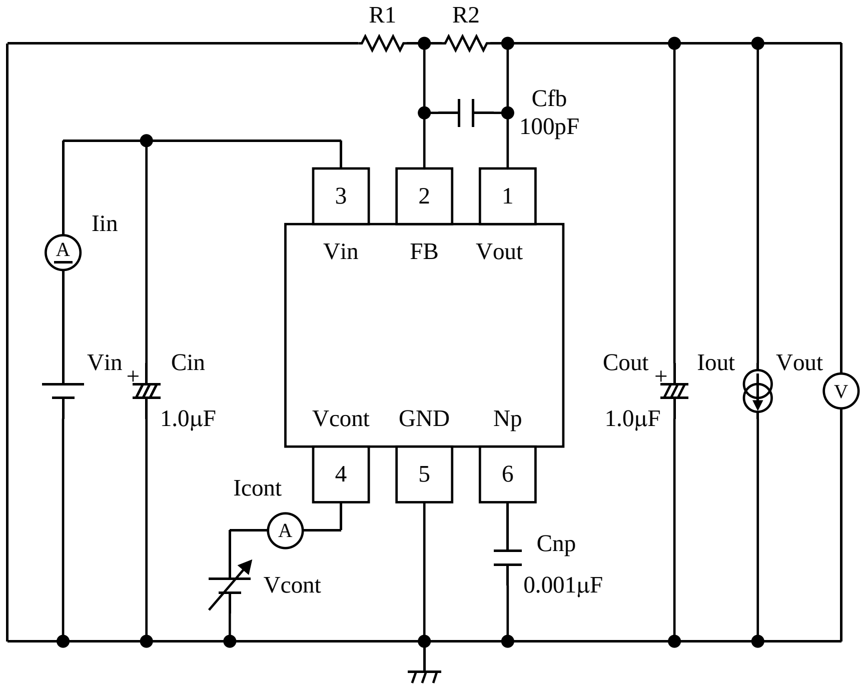
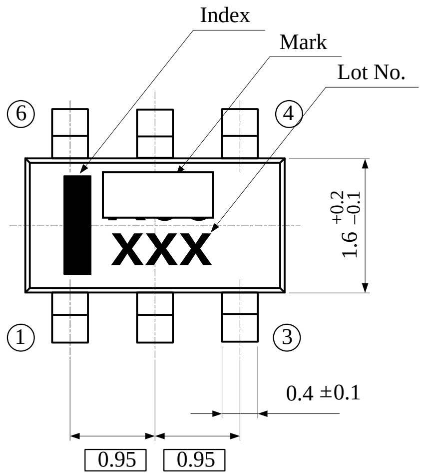
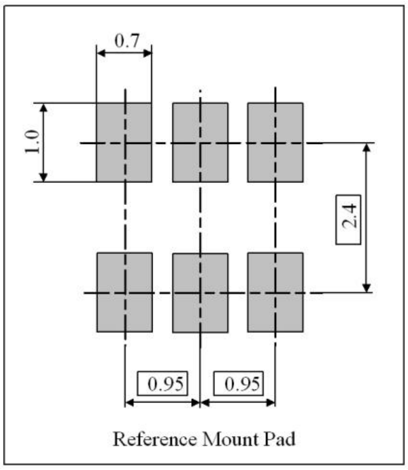


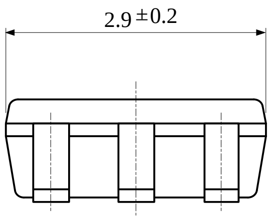
Figure 9. Test Circuit (R1=51kΩ, R2=68kΩ ($Vout_{TYP}$=3.0V))

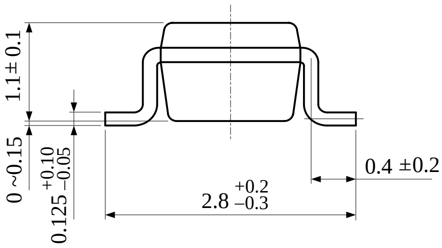
14. Package

■ Outline Dimensions









15. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/01/21	00	-	First edition

IMPORTANT NOTICE