# NMF3000, NMF3010

# Dual−Stage, Differential Lines Filter with ESD Protection

The NMF3000 and the NMF3010 are a dual−stage, differential line ESD and filtering protection scheme for input signals into portable devices. The NMF3000 is the first stage and is located at or very near to the interface to the outside world. It provides the high−level ESD protection as well as the initial filtering of incoming audio signals. The NMF3010 is the second stage and provides additional signal filtering. This second stage can be placed some distance away from the first stage to allow for effective filtering across extended distances.

### Features

- Dual Filtering Lines for 2−Channels or Differential Transmission
- Separate Power and Analog Grounds for ESD Protection and Filtering Circuitry
- $V_{CC}$ Input Pin on First Stage to Set Microphone DC Bias
- IEC 61000−4−2 Grade ±15 kV Contact ESD Protection on the Inputs, $V_{CC}$, and Between Power and Analog Grounds
- IEC 61000−4−2 Level 1 ESD protection on All Other Pin−to−Pin Combinations
- These are Pb−Free Devices*

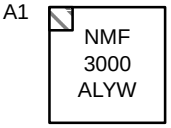
ON Semiconductor®

http://onsemi.com

**MARKING DIAGRAMS**

A1

**9 Bump Flip−Chip**
**CASE 499AE**




A1

**6 Bump Flip−Chip**
**CASE 499AF**


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

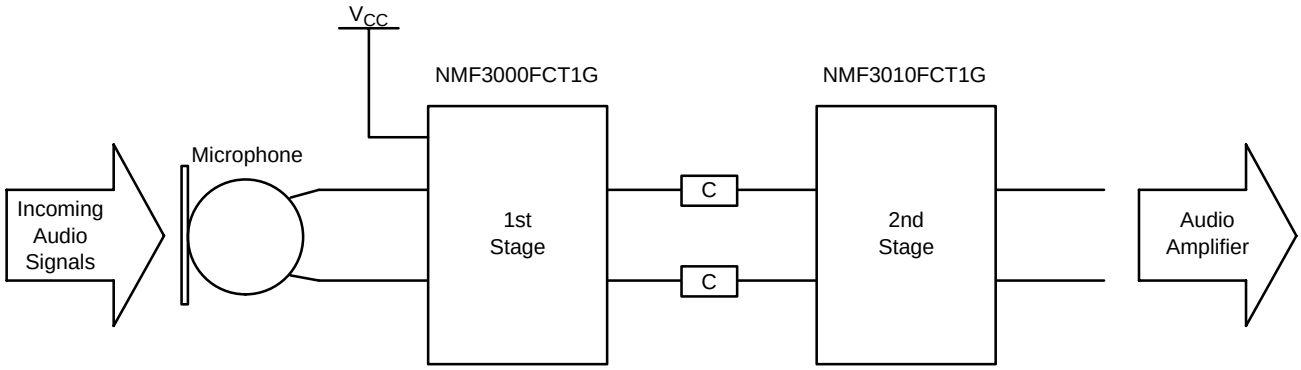



**Figure 1. System Diagram**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## FUNCTIONAL BLOCK DIAGRAMS

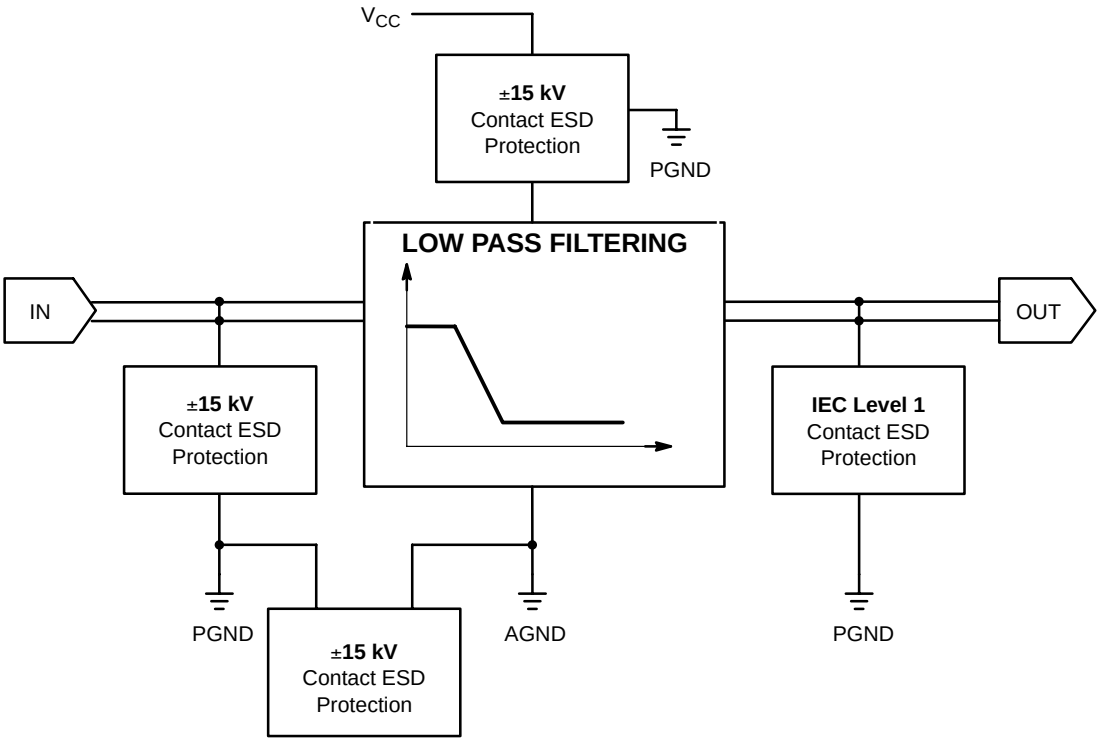



**Figure 2. First Stage: NMF3000FCT1G**

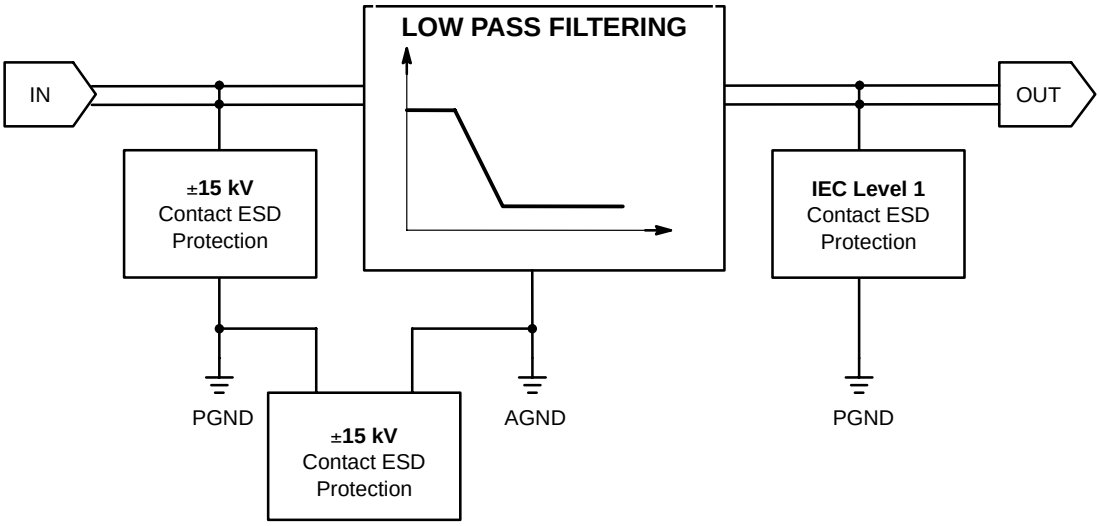



**Figure 3. Second Stage: NMF3010FCT1G**

## PINOUTS AND PIN DESCRIPTIONS

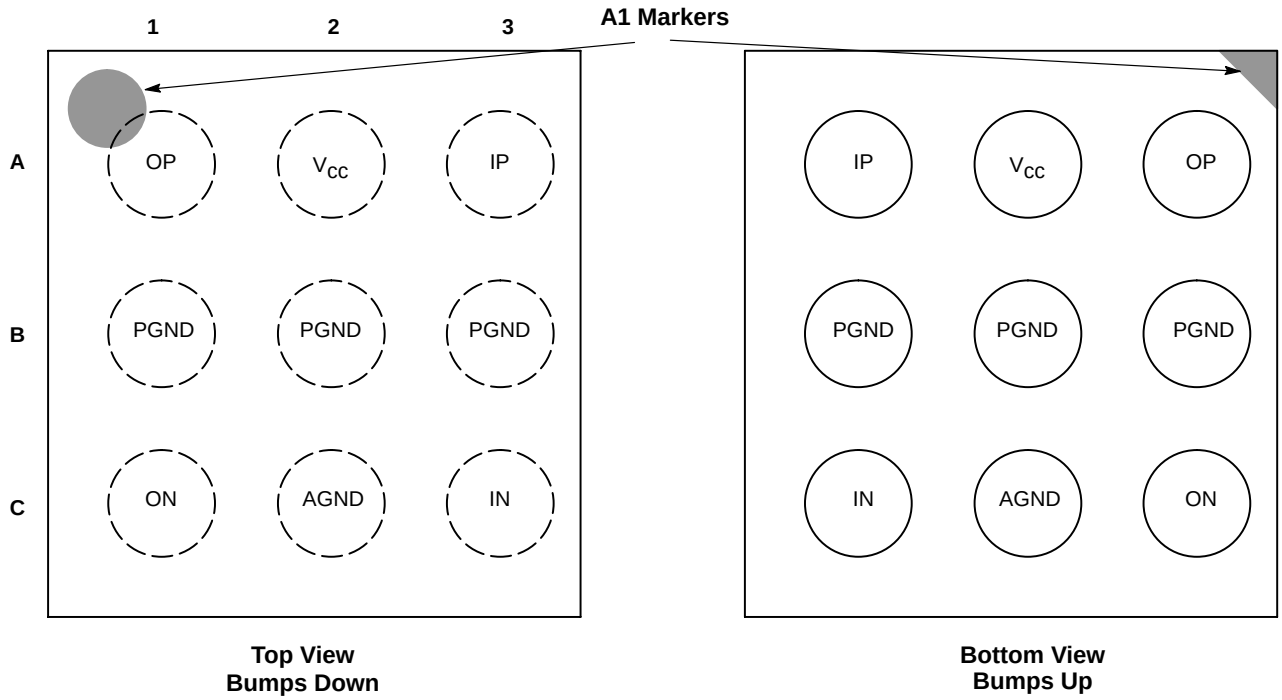



**Figure 4. Pinout Diagrams for First Stage: NMF3000FCT1G**

### PINOUT FUNCTIONS FOR FIRST STAGE

| Pin | Type | Description |
|---|---|---|
| A1 | Output P | Positive Side Signal Output |
| A2 | VCC | DC Power Connection |
| A3 | Input P | Positive Side Signal Input |
| B1, B2, B3 | PGND | Power Ground |
| C1 | Output N | Negative Side Signal Output |
| C2 | AGND | Analog Ground |
| C3 | Input N | Negative Side Signal Input |

## PINOUTS AND PIN DESCRIPTIONS

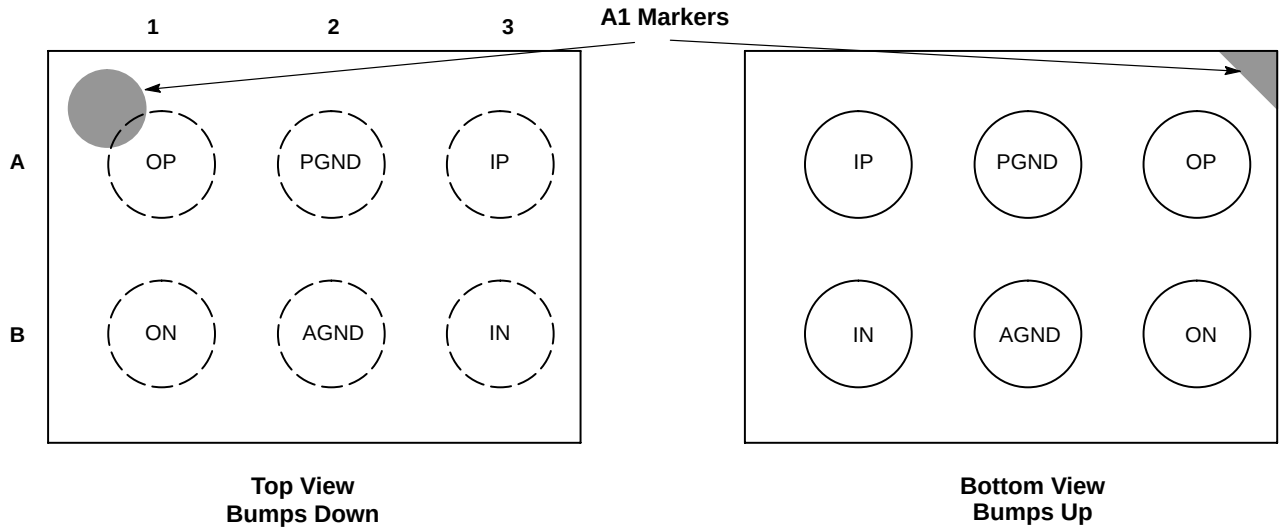



**Figure 5. Pinout Diagrams for Second Stage: NMF3010FCT1G**

### PINOUT FUNCTIONS FOR SECOND STAGE

| Pin | Type | Description |
|---|---|---|
| A1 | Output P | Positive Side Signal Output |
| A2 | PGND | Power Ground |
| A3 | Input P | Positive Side Signal Input |
| B1 | Output N | Negative Side Signal Output |
| B2 | AGND | Analog Ground |
| B3 | Input N | Negative Side Signal Input |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Units |
|---|---|---|---|
| Operating Ambient Temperature Range | $T_A$ | −40 to 85 | °C |
| Moisture Sensitivity | MSL | Level 1 | |
| Storage Temperature Range | $T_{stg}$ | −55 to 150 | °C |
| Supply Voltage | $V_{CC}$ | 0 to 11 | V |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 0 V to 10 V, $T_A$ = −40°C to 85°C, All Typical Values Measured at 25°C)

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | First stage only | $V_{CC}$ | 0 | | 10 | V |
| Attenuation | @ 800 MHz, 50 Ω Environment | | 52 | 95 | | dB |
| Attenuation | @ 1.9 GHz, 50 Ω Environment | | 52 | 70 | | dB |
| B2B Diode Breakdown Voltage | IR = 1.0 mA, Pin to PGND, AGND to PGND | B2B BV | ± 12 | | | V |
| Standoff Voltage | | VRM | | 10 | | V |
| Leakage Current | V = VRM, for each stage | IRM | | | 500 | nA |
| Power Dissipation | | | | | 100 | mW |
| NMF3000FCT1G DC Series Resistance | Input to output on first stage | RI/O | 997 | 1050 | 1103 | Ω |
| NMF3010FCT1G DC Series Resistance | Input to output on second stage | RI/O | 950 | 1000 | 1050 | Ω |
| Input Capacitance per Line | f = 1.0 MHz, for each stage when capacitor has 2.0 V across its terminals. | $C_{LINE}$ | 900 | 1000 | 1100 | pF |
| Bias Resistance per Line | First Stage Only | $R_{BIAS1}$ | 950 | 1000 | 1050 | Ω |
| Crosstalk | 50 Ω Source and Load | CT | −25 | | | dB |
| Noise | Idle−channel or Self−noise of the Network | | | | 6.0 | nV/√Hz |
| Distortion | Anywhere in the Bandwidth 20 Hz to 20 kHz | | | | 0.01 | % |

1. Specifications apply to devices as a pair, as shown in the system diagram, unless otherwise noted as ‘for each stage’.

## ESD CHARACTERISTICS

| Pin | Level | Type | Min | Units |
|---|---|---|---|---|
| NMF3000FCT1G: A2, C2, A3, C3 to PGND<br>NMF3010FCT1G: B2, B3, A3 to PGND | 4+<br>IEC 61000−4−2 | Contact | 15 | kV |
| NMF3000FCT1G: A2, C2, A3, C3 to PGND<br>NMF3010FCT1G: B2, B3, A3 to PGND | 4<br>IEC 61000−4−2 | Air | 15 | kV |
| NMF3000FCT1G: All Pins Pairwise<br>NMF3010FCT1G: All Pins Pairwise | 1<br>IEC 61000−4−2 | Contact | 2.0 | kV |
| NMF3000FCT1G: All Pins Pairwise<br>NMF3010FCT1G: All Pins Pairwise | 1<br>IEC 61000−4−2 | Air | 2.0 | kV |

## COMPONENT MATCHING

| Component | Description | Max | Unit |
|---|---|---|---|
| Resistors | Amount of Relative Variation between Symmetrical Resistors / Capacitors on the same Device | 2.0 | % |
| Capacitors | | 2.0 | % |

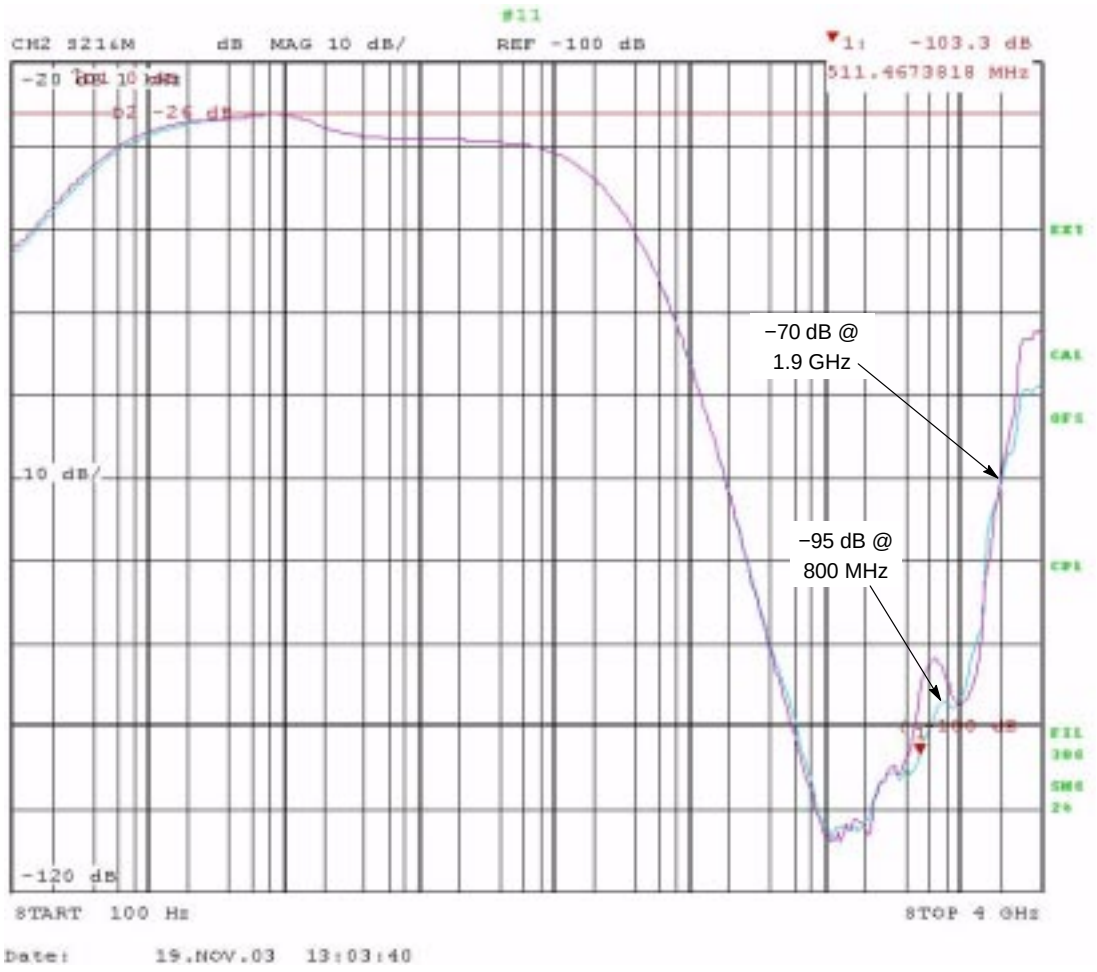
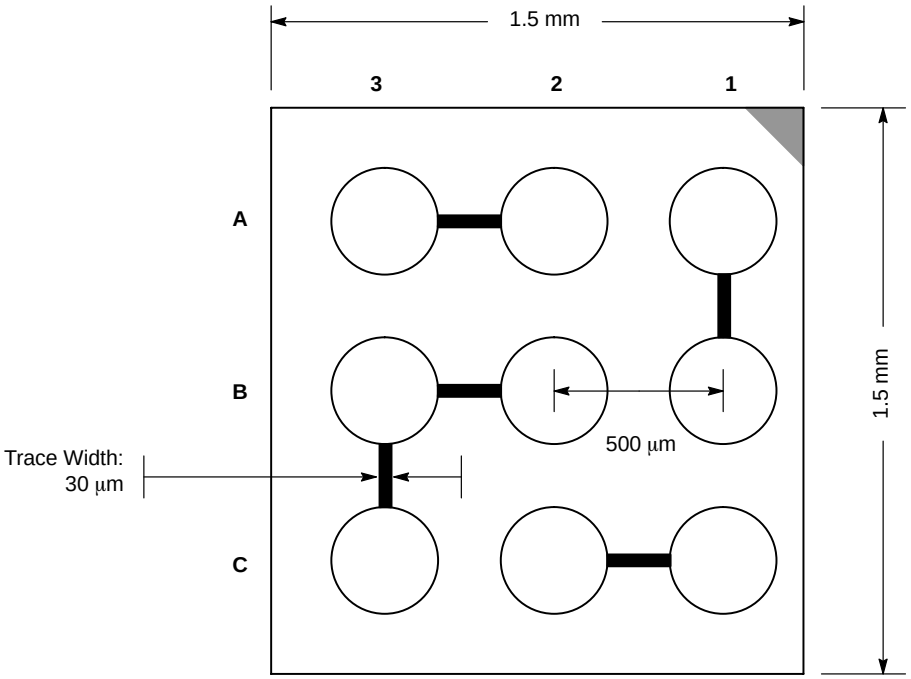


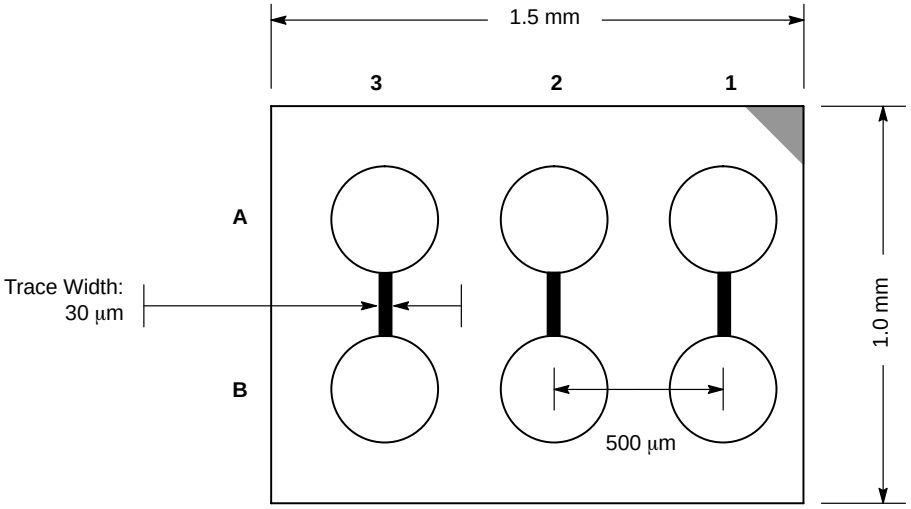

**Figure 6. Typical S21 of NMF3000FCT1G & NMF3010FCT1G in a 50 Ω Environment**
**2 Lines = Positive and Negative Sides**

## DAISY CHAIN SPECIFICATIONS




**Bottom View**
**Bumps Up**

**Figure 7. First Stage: NMF3000FCT1G**




**Bottom View**
**Bumps Up**

**Figure 8. Second Stage: NMF3010FCT1G**

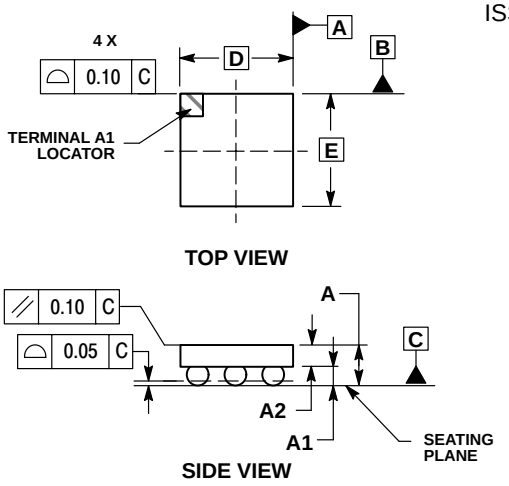
## DEVICE ORDERING INFORMATION

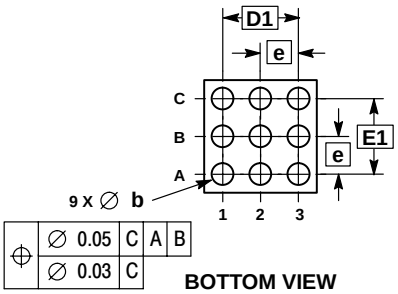
| Device Order Number | Package Type | Shipping† |
|---|---|---|
| NMF3000FCT1G | 9−Bump Flip−Chip | 3000 / Tape and Reel |
| NMF3010FCT1G | 6−Bump Flip−Chip | 3000 / Tape and Reel |
| ENGTDDSY3x3FCT1G | 9−Bump Flip−Chip | 500 / Tape and Reel |
| ENGTDDSY2x3FCT1G | 6−Bump Flip−Chip | 500 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**FLIP−CHIP−9**
CASE 499AE
ISSUE A

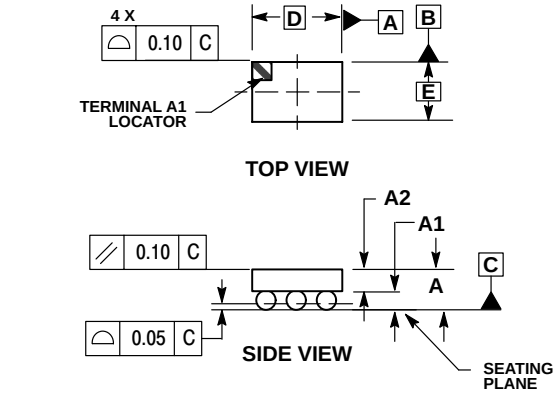


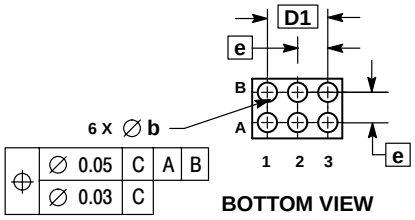




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | − − − | 0.700 |
| A1 | 0.210 | 0.270 |
| A2 | 0.380 | 0.430 |
| D | 1.489 BSC | |
| E | 1.489 BSC | |
| b | 0.290 | 0.340 |
| e | 0.500 BSC | |
| D1 | 1.000 BSC | |
| E1 | 1.000 BSC | |

**FLIP−CHIP−6**
CASE 499AF
ISSUE A

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| E | 0.989 BSC | |
| b | 0.290 | 0.340 |
| e | 0.500 BSC | |
| D1 | 1.000 BSC | |

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PUBLICATION ORDERING INFORMATION

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**NMF3000/D**