PIC14C000

Errata Sheet for PIC14C000 Revision A

The PIC14C000 parts you have received conform functionally to the PIC14C000 data sheet (DS40122**B**), except for the anomalies described below.

USING AN1 AND AN5 AS ANALOG INPUTS

1. Analog inputs AN1 and AN5 can not be used if their level-shift network is disabled. According to Section 9.2 of the PIC14C000 data sheet, (DS40122B), the level-shift network feature can be turned off by setting the LSOFF bit (SLPCON<4>). However, doing so will cause the AN1 and AN5 inputs to go to V_{DD}, rendering them unusable as analog input channels. Therefore, the LSOFF bit must remain cleared. The other functions associated with these pins, such as the current zeroing and filtering switches, operate as specified. The AN1 and AN5 pins can still be used for ADC operations, but a small firmware routine is required to ensure accurate results. This routine can be implemented by following the steps below:
   - Ensure the LSOFF bit (SLPCON<4>) is cleared.
   - Ensure a good zero-level on AN1 and/or AN5 by setting the ADZERO bit (ADCON0<0>).
   - Perform an A/D conversion as normal and keep the count from ADCAPH and ADCAPL in user-defined RAM. This is the representative digital count for the exact level-shift value.
   - Enable the signal of interest onto AN1 and/or AN5.
   - Perform another A/D conversion and keep the count in ADCAPH and ADCAPL. This is the representative digital count for the sum of the signal of interest and the exact level-shift value.
   - Subtract the level-shift count from the representative count for the sum.
   - This result will be the representative count for the signal of interest alone.

USING THE I^2C™ MODULE IN SMBus MODE

2. The I^2C Module in the PIC14C000 can be used with either PORTC<7:6> or PORTD<1:0> to provide the clock and data signal connections. According to Figure 7-16 of the PIC14C000 data sheet (DS40122B), the MISC<bit 3>, SMBus bit, allows user to select the input thresholds of PORTC<7:6> and PORTD<1:0> to either be SMBus-compatible or Schmitt Trigger-compatible.

   Although the data sheet says that PORTC<7:6> operates the same way as PORTD<1:0>, in the actual implementation, PORTC<7:6> always uses the Schmitt Trigger input thresholds when the I^2C module reads through PORTC<7:6>, even if the SMBus mode is selected.

   If PORTC<7:6> are read as port inputs, while the SMBus mode is selected, the SMBus voltage levels are used.

   Interfacing to an SMBus port can still be implemented using either of the following methods:

   - Use the I^2C module together with PORTD<1:0>, and set the MISC<3> bit high.
   - Use PORTC<7:6> or PORTD<1:0> with the MISC<3> bit set high, and perform the I^2C function in firmware.

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Clarifications/Corrections to the Data Sheet:

In the PIC14C000 Device Data Sheet (document DS40122B), the following clarifications and corrections should be noted:

1. Module: A/D
   The operating current specifications during SLEEP have been modified to the values shown in Table 1.

TABLE 1: A/D CONVERTER OPERATING CURRENT DURING SLEEP MODE

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
$I_{PD}1$	During A/D conversion:	—	500	900	—	TBD	900	µA	V_{DD} = 3.0V
$I_{PD}1$	All analog on and	—	650	1250	—	TBD	1250	µA	V_{DD} = 4.0V
	internal oscillator active								

2. Module: I/O Port
   The Input High Voltage specification for the RC7, RC6, RD1, and RD0 in the SMBus mode has been modified to the values shown in Table 2.

TABLE 2: RC7, RC6, RD1, RD0 INPUT HIGH VOLTAGE

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{IH}	SMBus mode (RC7, RC6, RD0, RD1)	1.4	—	6.0	1.4V	—	V_{DD}	V	SMBus bit, MISC<3> = 1

3. $\overline{MCLR}$ Reset
   The $\overline{MCLR}$ reset specification has been modified to the values shown in Table 3.

TABLE 3: $\overline{MCLR}$ RESET TIMING

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
TmcL	$\overline{MCLR}$ Pulse Width (low)	2.0	—	—	0.1	—	—	µS	V_{DD} = 5V, -40°C to +85°C
T_{IOZ}	I/O High Impedance from $\overline{MCLR}$ Low	—	—	2.1	—	—	0.1	µS	

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4. Module: Bandgap Voltage Reference
   The condition for the Output Voltage specification has been added as shown in Table 4.

TABLE 4: BANDGAP OUTPUT VOLTAGE SPECIFICATION

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
VO(VREF)	Output Voltage	1.14	1.19	1.24	1.14	1.19	1.24	V	TA = 25°C

5. Module: Temperature Sensor
   The Output linearity specification has been modified to the values shown in Table 5.

TABLE 5: TEMPERATURE SENSOR SPECIFICATION

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
LIN (temp)	Output Linearity (Note 1, 2)	—	0.5	—	—	TBD	—	°C	

Note 1: This parameter is characterized but not tested.
2: Linearity is defined as the maximum deviation over temperature from a best fit straight line.

6. Module: Internal Oscillator
   The Frequency Range specification has been modified to the values shown in Table 6.

TABLE 6: INTERNAL OSCILLATOR

Symbol	Characteristics	New Specification			Data Sheet Specification			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
FOSC (in)	Frequency Range	3.0	4.0	5.5	3.0	4.0	5.0	MHz	

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