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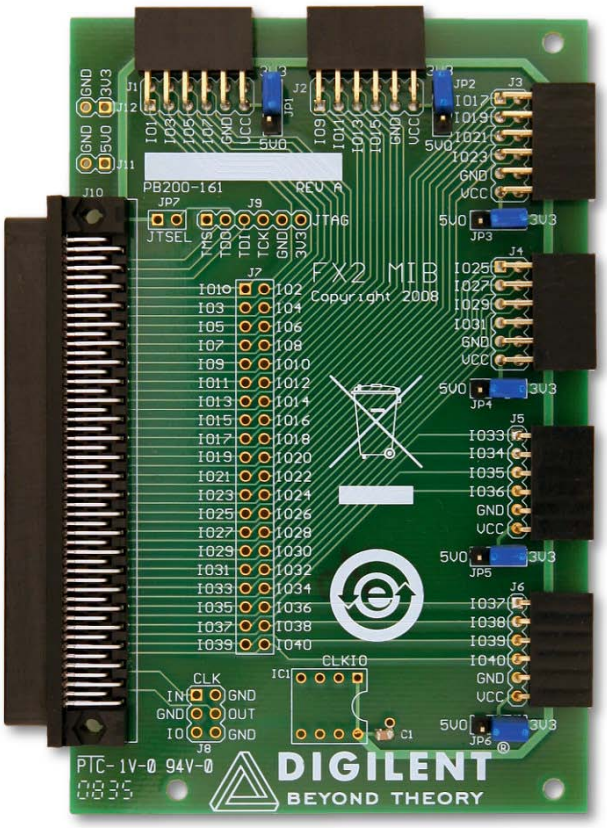
FX2 MIB™ Reference Manual

Revised January 14, 2009
This manual applies to the FX2 MIB rev. A

Overview

The Digilent FX2 Module Interface Board (MIB) offers a ready-made solution for interfacing peripheral modules to Digilent system boards.



The FX2 MIB.

Features include:

- FX2 peripheral board connector
- four 12-pin and two 6-pin Pmod connectors
- access to JTAG scan chain
- access to signals for test points
- provision for oscillator for clock input to system board

1 Functional Description

1.1 Power Connections

The FX2 MIB provides two power busses and a ground bus. The two power busses are labeled VCC and VCCFX2. These two busses are made available at each connector position on the board. There is also a ground plane that connects the ground pins from all connectors.

The usual Digilent convention is to power the VCC bus at 3.3V and the VCCFX2 bus at 5.0V. However, depending on the system board connected and the power supply used, other voltages may be present. Use caution when using any voltage other than 3.3V on the VCC bus. Most Digilent system boards will be damaged if the voltage on the VCC bus is greater than 3.3V.

FX2 connector J10 is provided on one side of the board for connection to Digilent system boards, like the Nexys2, that contain an FX2-style connector. The Digilent FX2 connector signal convention provides for forty general-purpose I/O signals, three clock signals, JTAG signals, and power busses.

The forty general-purpose I/O signals from the FX2 connector are brought out to connector J7. These signals are labeled IO1-IO40. See Table 1 for a description of the relationship between FX2 connector pins and signal names on J7. The remaining signals from the FX2 connector are brought out to connectors J8, J9, J11, and J12. See Table 1 for a description of the relationship between FX2 connector pins and connectors J8 and J9 signal names. In addition to the FX2 connector signals, connector J11 and J12 also provide access to the power and ground busses.

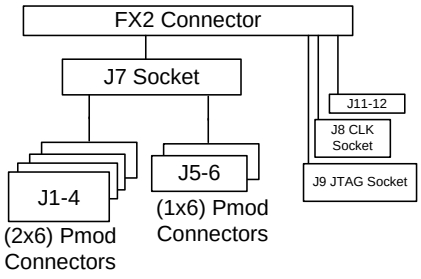


Figure 1. MIB block diagram.

1.2 Pmod Connectors

Digilent Pmods provide various peripheral functions. These can be as simple as buttons or switches for inputs and LEDs for outputs, or as complex as graphical LCD display panels, accelerometers, and keypads.

All Digilent Pmods use either a six-wire interface or a twelve-wire interface. The six-wire interface provides four I/O signals, power, and ground. The twelve-wire interface provides eight I/O signals, two powers, and two grounds. The signal definitions for the I/O signals as well as the voltage requirements for the power supply depend on the specific module.

The FX2 MIB provides four twelve-pin and two six-pin Pmod connectors.

The twelve-pin connector provides access such that the top set of four pins are the odd labeled signals while the bottom set are even labeled signals. See Table 2.

The signals for Pmod connectors J1-J6 are brought out to connector J7. These signals are labeled IO1-IO40.

Each Pmod connector has an associated power select jumper. The power select jumper for J1 is JP1, and so on. These jumpers are used to select one of the two power busses on the FX2 MIB to provide power to the power supply pin on a Pmod plugged into that connector position. Placing a shorting block in the 3V3 position provides VCC power to the Pmod. Placing a shorting block in the 5V0 position provides VCCFX2 power to the Pmod. Place a shorting block so that it hangs off of the center pin only to disconnect power to the Pmod.

1.3 FPGA Configuration

The FX2 MIB provides JTAG access via unloaded jumper J9. Given that the jumper JP7 labeled JTSEL is shorted, this jumper allows a connected board to be programmed via a JTAG cable.

See Table 1 for a description of the relationship between the FX2 connector pins and the connections on the JTAG jumper J9.

1.4 Clocks

The FX2 MIB provides an oscillator clock input to a system board via socket connector IC1. This socket can be used to input a clock signal to a system board when an external oscillator is placed on it. It will then output a clock signal on the CLKIO pin of the FX2 connector.

The unloaded jumper J8 provides access to all possible clock signals into and out of the FX2 MIB. This includes the signal CLKIO from the external oscillator socket connector as well as CLKIO and CLKOUT signals directly from the FX2 connector.

See Table 1 for more details.

A	Pinout	B	Pinout
1	VCC	1	SHLD
2	VCC	2	GND
3	TMS	3	TDI
4	JTSEL	4	TCK
5	TDO	5	GND
6	IO1	6	GND
7	IO2	7	GND
8	IO3	8	GND
9	IO4	9	GND
10	IO5	10	GND
11	IO6	11	GND
12	IO7	12	GND
13	IO8	13	GND
14	IO9	14	GND
15	IO10	15	GND
16	IO11	16	GND
17	IO12	17	GND
18	IO13	18	GND
19	IO14	19	GND
20	IO15	20	GND
21	IO16	21	GND

22	IO17	22	GND
23	IO18	23	GND
24	IO19	24	GND
25	IO20	25	GND
26	IO21	26	GND
27	IO22	27	GND
28	IO23	28	GND
29	IO24	29	GND
30	IO25	30	GND
31	IO26	31	GND
32	IO27	32	GND
33	IO28	33	GND
34	IO29	34	GND
35	IO30	35	GND
36	IO31	36	GND
37	IO32	37	GND
38	IO33	38	GND
39	IO34	39	GND
40	IO35	40	GND
41	IO36	41	GND
42	IO37	42	GND
43	IO38	43	GND
44	IO39	44	GND
45	IO40	45	GND
46	GND	46	CLKIN
47	CLKOUT	47	GND
48	GND	48	CLKIO
49	VU	49	VU
50	VU	50	SHLD

Table 1. FX2 signals and connector pinout.

2 Pmod Connector Pin Layouts

Pin	Pinout
1	IO1
2	IO3
3	IO5
4	IO7
5	GND
6	VDD

Table 2-1. J1 top set of pins.

Pin	Pinout
7	IO2
8	IO4
9	IO6
10	IO8
11	GND
12	VDD

Table 2-2. J1 bottom set of pins.

Pin	Pinout
1	IO9
2	IO11
3	IO13
4	IO15
5	GND
6	VDD

Table 2-3. J2 top set of pins.

Pin	Pinout
7	IO10
8	IO12
9	IO14
10	IO16
11	GND
12	VDD

Table 2-4. J2 bottom set of pins.

Pin	Pinout
1	IO17
2	IO19
3	IO21
4	IO23
5	GND
6	VDD

Table 2-5. J3 top set of pins.

Pin	Pinout
7	IO18
8	IO20
9	IO22
10	IO24
11	GND
12	VDD

Table 2-6. J3 bottom set of pins.

Pin	Pinout
1	IO25
2	IO27
3	IO29
4	IO31
5	GND
6	VDD

Table 2-7. J4 top set of pins.

Pin	Pinout
7	IO26
8	IO28
9	IO30
10	IO32
11	GND
12	VDD

Table 2-8. J4 bottom set of pins.

Pin	Pinout
1	IO33
2	IO34
3	IO35
4	IO36
5	GND
6	VDD

Table 2-9. J5 pins.

Pin	Pinout
1	IO37
2	IO38
3	IO39
4	IO40
5	GND
6	VDD

Table 2-10. J6 pins.