



# Si3406x Family Data Sheet

## Fully-Integrated IEEE 802.3-Compliant POE+ PD Interface and High-Efficiency Switching Regulators with Transistor Bypass, Sleep, Wake, and LED Drive

The Si3406x family integrates all power management and control functions required in a Power-over-Ethernet Plus (PoE+) powered device (PD) application. These devices convert the high voltage supplied over the 10/100/1000BASE-T Ethernet connection to a regulated, low-voltage output supply. The optimized architecture of this device family minimizes the solution footprint and external BOM cost and enables the use of low-cost external components while maintaining high performance. The Si3406x family integrates the required diode bridges and transient surge suppressor, thus enabling direct connection of the IC to the Ethernet RJ-45 connector. The switching power FET and all associated functions are also integrated. The integrated, current mode controlled switching regulator supports isolated or non-isolated flyback and buck converter topologies. The switching frequency for the regulator is tunable with a simple external resistor value to help avoid unwanted harmonics for better emissions control. A synchronous driver is provided to optionally drive a secondary side FET to improve efficiency of power conversion. Connection to the PSE switch is maintained during sleep by an optional automated maintain-power-signature (MPS) signal.

These devices fully support the IEEE 802.3at specification for the cases of single or two event classification. Standard external resistors provide the proper IEEE 802.3 signatures for the detection function and programming of the classification mode, and internal startup circuits ensure well-controlled soft-start initial operation of both the hotswap switch and the voltage regulator.

The Si34061 and Si34062 add main transformer bias winding support for ultra-high-efficiency operation.

The Si34061 includes support for external augmentation or full bypass of the internal hotswap and/or switching FET for best power handling and thermal management at the high end of Class 4, plus offers a further boost in power conversion efficiency when needed.

The Si34062 includes support for sleep modes with wake function, as well as LED drive capability. These features can be utilized to minimize standby current, control sleep and wake states, and provide application status information using a solid or blinking LED.

The Si3406 is available in a low-profile, 20-pin, 5 x 5 mm QFN package, and the Si34061 and Si34062 are available in low-profile, 24-pin, 5 x 5 mm QFN packages.

### KEY FEATURES

- Type 1 (PoE) or Type 2 (PoE+) power
- Full IEEE 802.3at compliance
- Synchronous secondary FET driver
- Current mode dc-dc converter
- Tunable switching frequency
- Auxiliary transformer winding support
- Auxiliary adapter support
- Internal hotswap and switching FET bypass support
- Automated maintain-power-signature (MPS) support
- Sleep mode augmented with wake pin, mode control, and LED driver
- 120 V Absolute Max voltage performance
- Extended -40 to +85 °C temperature
- Compact ROHS-compliant 5 mm x 5 mm QFN Package

### APPLICATIONS

- Voice over IP telephones
- Wireless access points
- Security and surveillance IP cameras
- Lighting luminaires
- Point-of-sale terminals
- Internet appliances
- Network devices

## 1. Ordering Guide

**Table 1.1. Si3406x Ordering Guide**

Ordering Part Number	Package	Temperature Range (Ambient)	Applications
Si3406-A-GM	5 x 5 mm 20-QFN Pb-free, RoHS-compliant	–40 to 85 °C Extended	All Purposes
Si34061-A-GM	5 x 5 mm 24-QFN Pb-free, RoHS-compliant	–40 to 85 °C Extended	Any high-power, high-efficiency uses, such as Wireless Access Points and IP Cameras
Si34062-A-GM	5 x 5 mm 24-QFN Pb-free, RoHS-compliant	–40 to 85 °C Extended	IP Phones or other uses with Sleep/Green mode

# Table of Contents

<b>1. Ordering Guide</b>	<b>2</b>
<b>2. System Overview</b>	<b>4</b>
2.1 Block Diagrams	4
2.2 Power over Ethernet (PoE) Line-Side Interface	5
2.2.1 Surge Protection	5
2.2.2 Telephony Protection	5
2.2.3 Detection and Classification	6
2.3 Hotswap Switch	6
2.4 HSSW State Machine	7
2.4.1 External HSSW FET Driver	7
2.5 DC to DC Converter	8
2.5.1 Average Current Sensing, Overcurrent, and Low-Current Detection	9
2.5.2 Sync FET Driver	9
2.6 External HSSW FET Driver	9
2.7 Tunable Oscillator	9
2.8 Regulators	10
2.9 Sleep Mode	10
2.10 Extended Sleep Mode	10
2.11 External Wall Support	11
<b>3. Application Examples</b>	<b>12</b>
<b>4. Electrical Specifications</b>	<b>14</b>
<b>5. Pin Descriptions</b>	<b>19</b>
5.1 Detailed Pin Descriptions	21
<b>6. Packaging</b>	<b>26</b>
6.1 Package Outline: Si3406	26
6.2 Land Pattern: Si3406	28
6.3 Package Outline: Si34061/62	29
6.4 Land Pattern: Si34061/62	31
<b>7. Top Markings</b>	<b>32</b>
7.1 Si3406 Top Marking	32
7.2 Si34061 Top Marking	33
7.3 Si34062 Top Marking	34
<b>8. Revision History</b>	<b>35</b>

## 2. System Overview

The following Block Diagrams will give the designer a sense for the internal arrangement of functional blocks, plus their relationships to external pins. The Block Diagrams are followed by a description of the features of these integrated circuits.

### 2.1 Block Diagrams

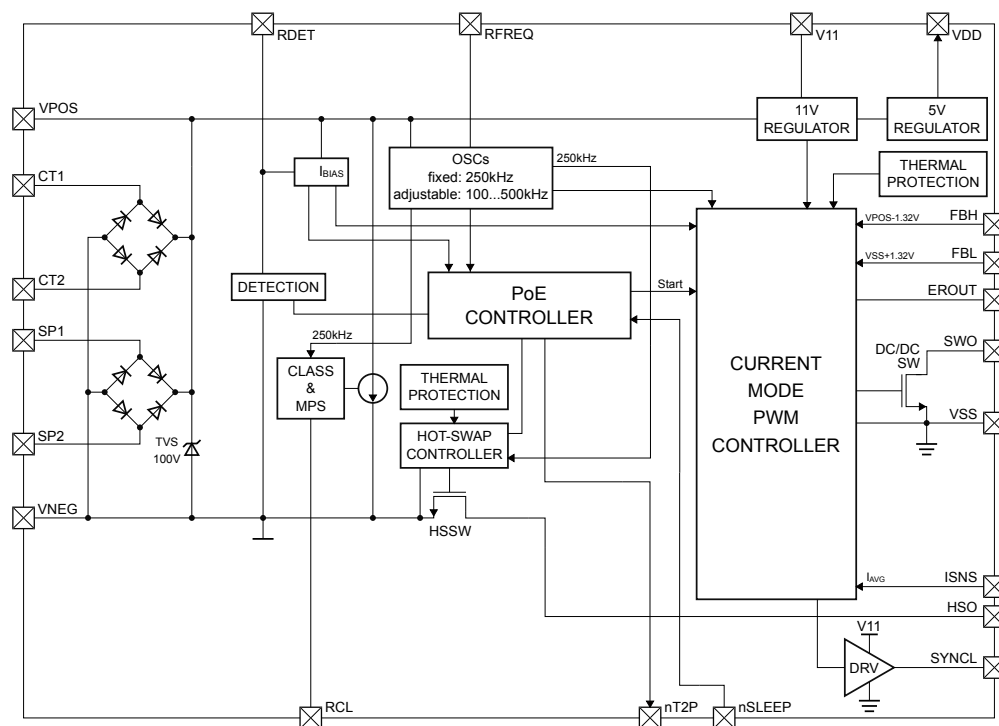


Figure 2.1. Si3406 Block Diagram

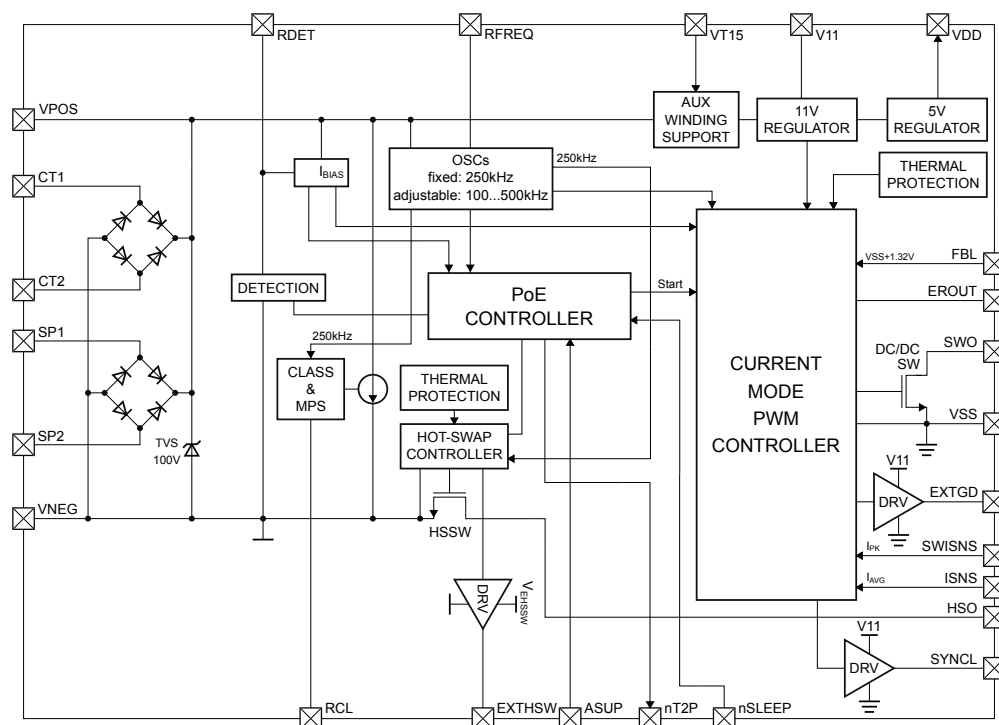


Figure 2.2. Si34061 Block Diagram

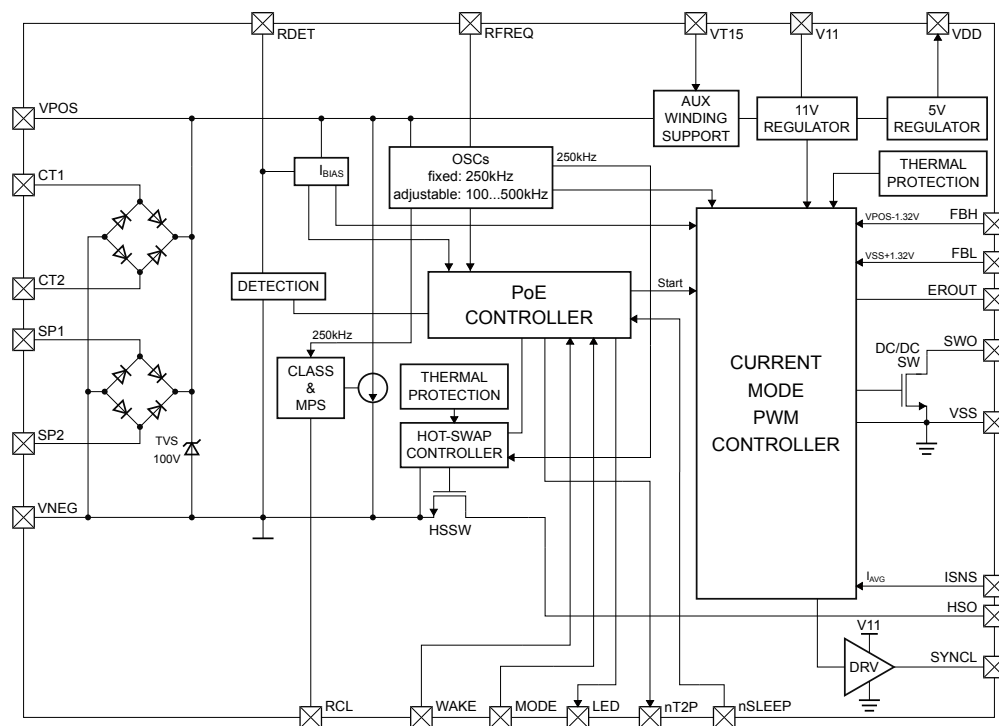


Figure 2.3. Si34062 Block Diagram

## 2.2 Power over Ethernet (PoE) Line-Side Interface

The PoE line interface consists of diode bridges, internal surge protection, and the protocol interface support for detection and classification.

Internal diode bridge maximum current is given by the specification,  $I_{RECT}$ . If the application needs to consume more current from the power interface, an external diode bridge has to be used. The external bridge should be connected in parallel to the internal bridge and the designer must ensure that the internal bridge will not conduct significant current by using low-voltage-drop external diodes.

The chip features active protection against surge transients and accidentally applied telephony voltages.

### 2.2.1 Surge Protection

The surge protection circuit is activated if the VPOS-VNEG voltage exceeds  $T_{PROT}$  and the hotswap switch is off (dc-dc is not powered). If the hotswap switch is on, the surge power is sunk in the dc-dc's capacitance.

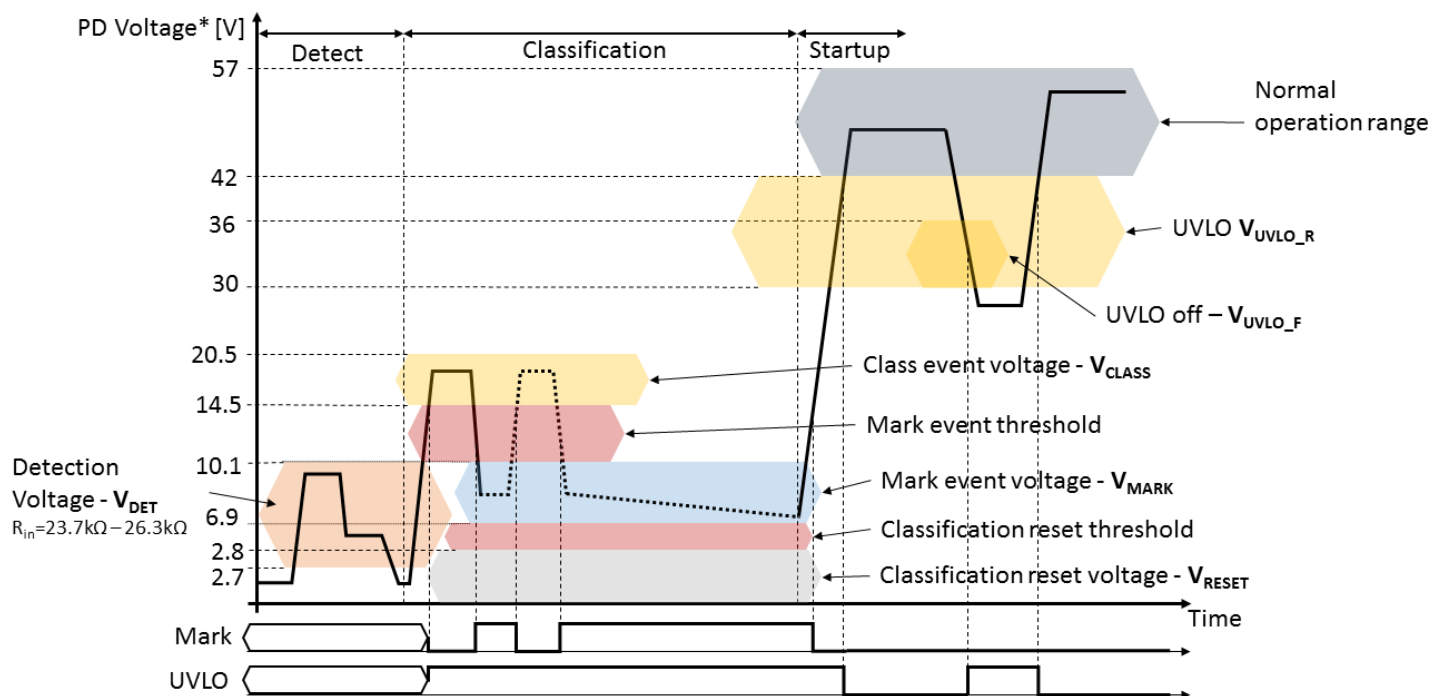
The internal surge protection can be overridden with an external TVS if higher than specified surge conditions need to be tolerated. The external surge device must be connected in parallel to the internal one; therefore, the designer must ensure that the external surge protection will activate prior to the internal surge protection.

### 2.2.2 Telephony Protection

The Si3406x provides protection against telephony ringing voltage. The telephony ringing is much longer than the surge pulse but it has less energy, therefore, the Si3406x has a switch parallel with the supply (VPOS and VNEG). When the protection circuit is activated, it turns ON the telephony switch; the ringing energy then dissipates on this switch and ringing generator resistance ( $> 400 \Omega$ ).

### 2.2.3 Detection and Classification

When si3406x is connected to the Ethernet cable it has to provide a characteristic resistance (~25 kΩ) to the PSE in a given voltage range (2.7–10.1 V). This is called detection. After the PSE detects the PD, the PSE increases the voltage above the classification threshold 14.5 V. Then, the PD provides the classification current to inform the PSE about its required power class (Class 1, 2, 3, or 4). Type 1 PSEs cannot provide enough power for a Class4 PD. Type 2 PSEs have additional voltage steps before switching on the PD. After an initial classification voltage pulse, the Type 2 PSE reduces the voltage below the mark threshold level (10 V) then raises it up again to the Class event range. Last, before switching ON the DCDC it reduces the voltage again. This sequence is recognized by the si3406x and its pull down its nT2P pin to inform the application about the higher available power; otherwise, the application will need to operate in a reduced power consumption state (Type 1) if the PSE is incapable of delivering Class 4 power.



\*Voltages shown are representative. Refer to Electrical Characteristics table.

Figure 2.4. Powered Device Voltages

### 2.3 Hotswap Switch

The internal hotswap switch (HSSW) is turned on (conducting) when the PoE interface voltage goes above  $V_{UVLO\_R}$ . It provides limited inrush current until the dcdc side capacitor is charged. The hotswap switch turns off (open) if voltage on the HSSW switch (HSO-VNEG) is greater than  $V_{HSSW\_OFF}$ .

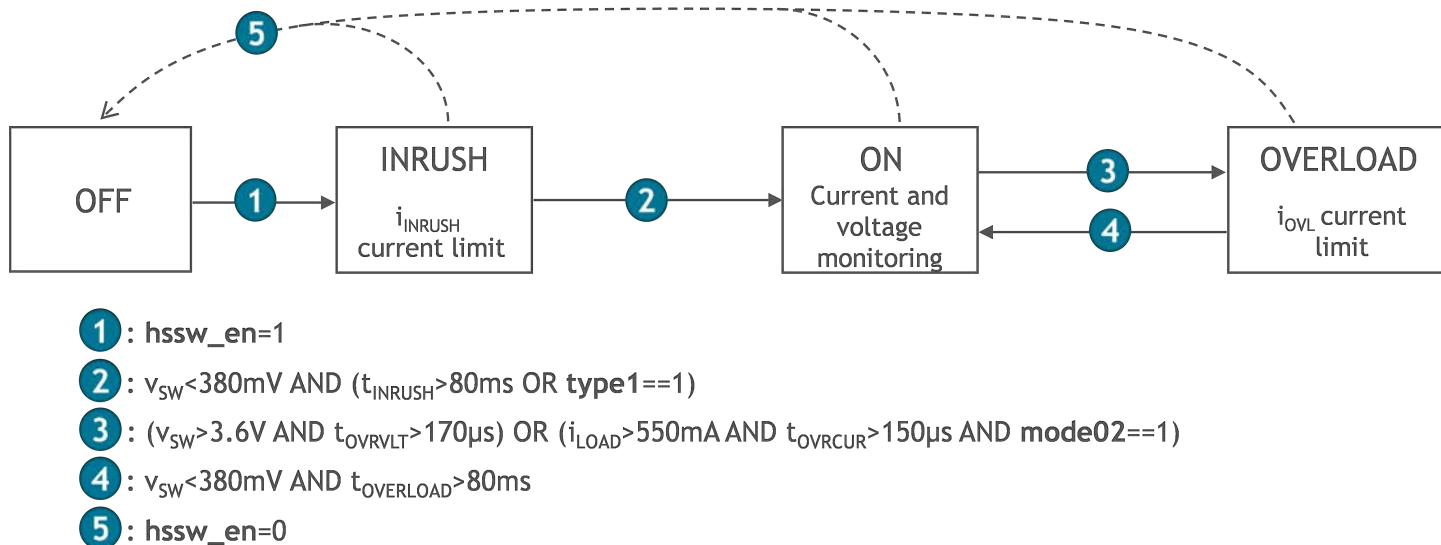
In overload, the hotswap switch goes into current-limiting mode with a current limit of  $I_{OVL}$ . It will turn back ON after  $T_{WAITHSSW}$  elapses and the dc-dc input capacitor is recharged, meaning the HSO-VNEG voltage is less than  $V_{HSSW\_ON}$ .

The hotswap switch (if it is in the on state and conducting) can detect if the current is lower than  $I_{MPSth}$ . In this case, the chip turns on MPS pulse generation, which ensures that the PSE will not disconnect.

With the Si34061, an external hotswap switch can be used to improve efficiency and reduce thermal stress in high current applications. For Class 3 applications, using an external hotswap switch is recommended; for Class 4, it is mandatory because the internal hotswap switch otherwise generates significant heat. When an external hotswap switch is used, intelligent switch control ensures that inrush current limiting and automatic MPS request of the internal switch are still supported.

## 2.4 HSSW State Machine

The HSSW operates as simple 4-state state machine:



**Figure 2.5. Hotswap Switch 4-State Machine**

**Note:** Internal signal names are shown in this Figure, not to be confused with external pin names. For the below discussion,  $I_{LOAD}$  is the switch current, and  $V_{HSSW}$  is the voltage drop of the switch. In other words,  $V_{HSSW} = HSO - VNEG$ . All the voltage, current and time limits of the above diagram are typical values.

### OFF State

HSSW turn-on is controlled by UVLO, the undervoltage lockout feature. When UVLO is engaged, the HSSW is OFF. In this state, the HSSW is in idle mode, VNEG and HSO pins are disconnected. In normal operation, a complete detect/classification procedure precedes the HSSW turn-on, and the control of this sequence is implemented in the state machine logic of the chip.

### INRUSH State

After the controller enables the HSSW, the block starts operation in the INRUSH state. In this state the switch itself is not directly turned on, but operating in a closed-loop current limit mode to avoid high current peaks during the charging of the primary bypass cap of the dc to dc converter.

If the  $V_{HSSW}$  voltage drops below 380 mV (meaning the bypass cap is 99% charged), the HSSW will change state to ON either in Type1 classification immediately, or in Type2 classification if the HSSW has been in the INRUSH state for at least 80 ms.

### ON State

In ON state, the HSSW switch is directly turned on. The HSSW circuit continuously monitors  $V_{HSSW}$ . HSSW will change to OVERLOAD state if  $V_{HSSW}$  voltage increases over 3.6 V for at least 140  $\mu s$ .

### OVERLOAD State

In OVERLOAD state the HSSW operates in closed-loop low current limit mode. If the  $V_{HSSW}$  voltage drops below 360 mV again, and the HSSW has been in the OVERLOAD state for at least 80 ms, the HSSW will change back to the ON state.

#### 2.4.1 External HSSW FET Driver

An external HSSW FET may be used to improve thermal operation of an Si34061 at very high power loading levels (the top end of Class 4).

With the Si34061, the chip automatically detects if the EXT\_HSW pin is connected to VNEG or to a FET gate at startup. If the external hotswap FET driver will not be used, the EXT\_HSW pin must be tied to VNEG.

For further information on using an external HSSW FET, please refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

## 2.5 DC to DC Converter

The dc-to-dc converter is current-controlled for easier compensation and more robust protection of circuit magnetics. The controller has the following features:

- High- and low-side feedback (supports buck and flyback topologies).
- $<1\ \Omega$  internal switching FET
- Driver for optional synchronous rectification
- Overcurrent detection
- Low current detection
- Cycle skipping at low current and short circuit conditions
- Optional external switching FET driver (Si34061)
- Automatic non-overlap control

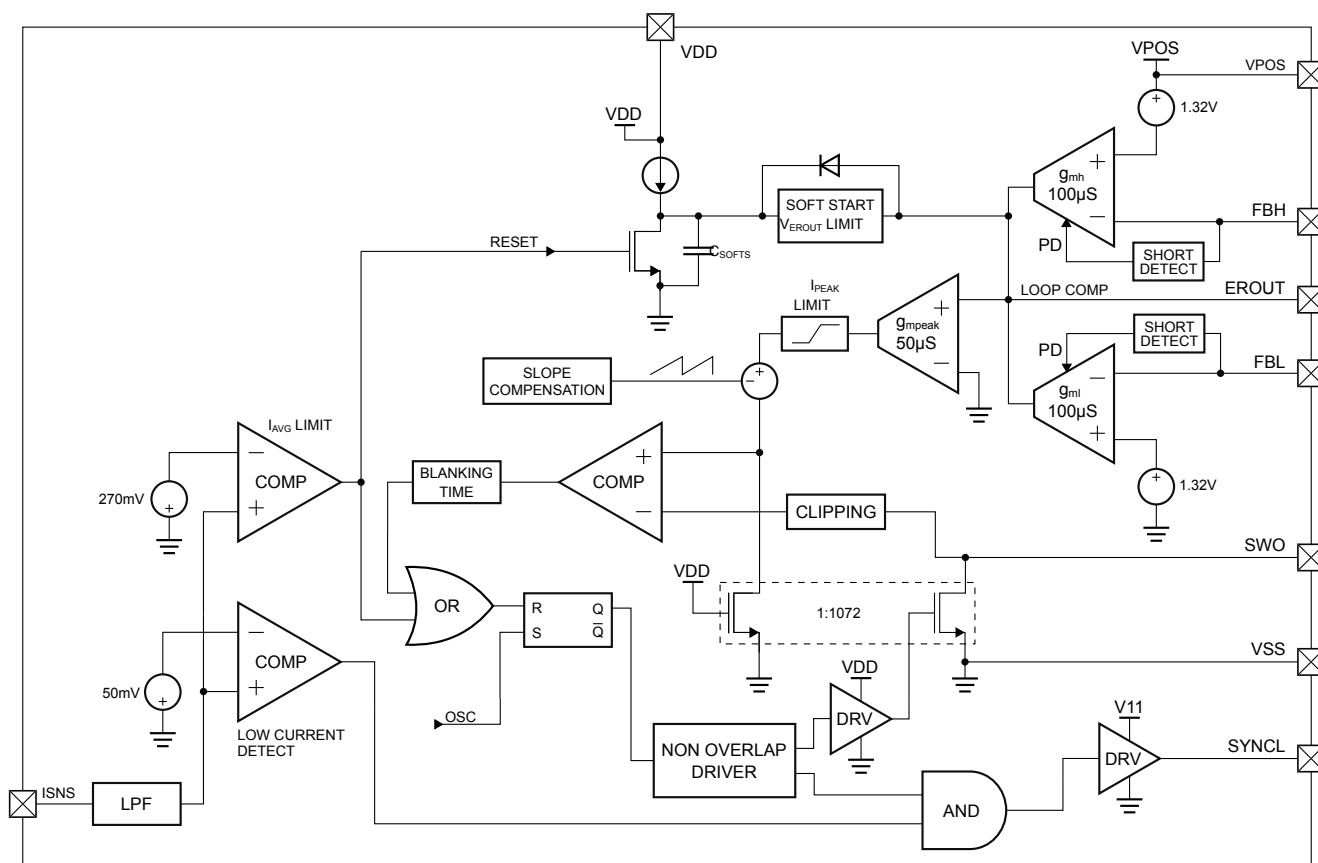


Figure 2.6. Si3406x DC-DC Converter

When the internal switching FET is used with the converter, internal peak current detection is employed. When the EXTGD pin and an external FET are used with Si34061, an external current sense resistor is used to measure the peak current connected to the SWISNS pin. Changing that resistor allows the application to set the converter maximum peak current to protect the magnetic components (like the transformer) from saturation.

Feedback to the dcdc converter can be provided in three ways:

- High side, referenced to VPOS, connected to FBH pin (buck converter)
- Low side, referenced to VSS, connected to FBL pin (nonisolated flyback)
- Directly to EROUT pin by a voltage to current converter (isolated flyback)

The EROUT pin provides current output (if FBL or FBH is used) and voltage input. Also, the loop compensation impedance is connected to EROUT. The active voltage range is  $V_{EROUT}$ , which is proportional to the converter peak current.

The converter startup is not configurable; soft start is accomplished by internal circuitry. Soft start time is  $T_{SOFTSTART}$ . The intelligent soft start circuit dynamically adjusts the soft start time depending on the connected load.



### 2.5.1 Average Current Sensing, Overcurrent, and Low-Current Detection

The application average current is sensed by an external resistor ( $R_{SENSE}$ ) connected between VSS and ISNS. Overcurrent is detected and triggered when the voltage on the sense resistor exceeds  $V_{ISNS\_OVC}$ . Sizing the resistor allows the designer to set the overcurrent limit according to application needs. When overcurrent is triggered, the dc/dc controller goes into reset until the overcurrent resolves. When the overcurrent is no longer present, the controller starts up again with softstart.

This external sense resistor is also used to detect a low current situation. When the voltage on the sense resistor goes below  $V_{ISNS\_LC}$ , the dc/dc controller disables the sync FET and the external hotswap switch, allowing very low current consumption—the internal hotswap switch then measures the chip current internally. If the average current is lower than the PoE maintain power signature (MPS) limit, and if automatic sleep mode is enabled, the chip turns on the MPS generation. See the sleep mode section for further detail.

### 2.5.2 Sync FET Driver

With the Si3406x family, an optional synchronous rectifying FET may be used in place of an output rectifier diode for improved power conversion efficiency.

A gate driver is provided for this purpose. The synchronous rectifying FET driver is enabled by default in Si3406x configurations, but, if a synchronous FET is not used in the design, the SYNCL pin must not be connected (do not connect SYNCL to any power or ground rail). The synchronous rectifying FET driver is disabled only when the dc/dc converter measures low average current (meaning lower than  $V_{ISNS\_LC}$  on ISNS). This ensures low sleep mode current consumption.

### 2.6 External HSSW FET Driver

An external HSSW FET may be used to improve thermal operation of an Si34061 at very high power loading levels (the top end of Class 4).

With the Si34061, the chip automatically detects if the EXTSHW pin is connected to VNEG or to a FET gate at startup. If the external hotswap FET driver will not be used, the EXTSHW pin must be tied to VNEG.

For further information on using an external HSSW FET, please refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

### 2.7 Tunable Oscillator

The dc/dc frequency can be fixed to 250 kHz or tunable by an external resistor.

The tuning resistor must be connected between the  $R_{FREQ}$  pin and VPOS. If  $R_{FREQ}$  is shorted to VPOS, the fixed frequency oscillator will provide the clock,  $F_{OSCINT}$ , to the dc/dc converter; otherwise, the resistor will determine the frequency as shown in the curve below.

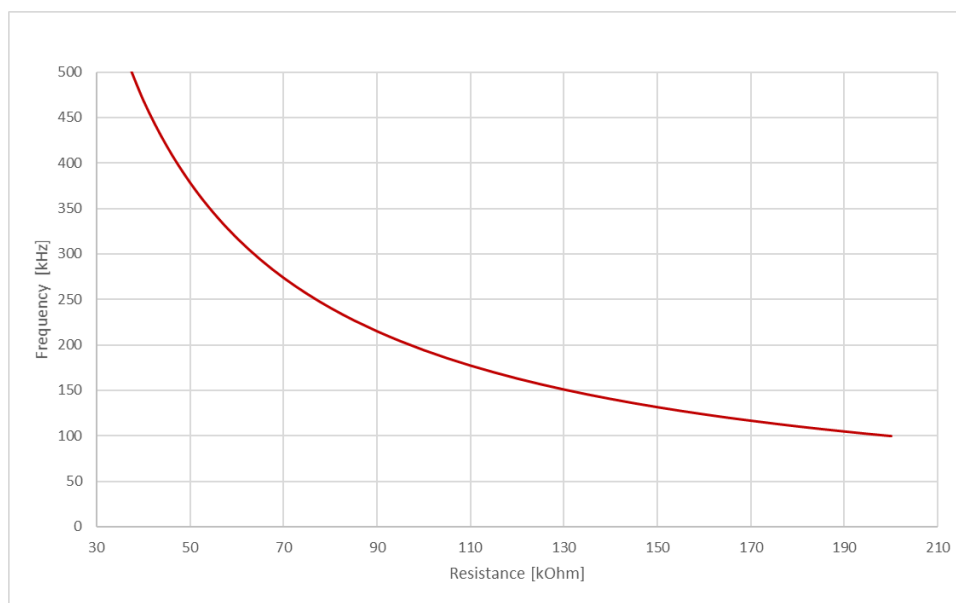


Figure 2.7.  $R_{FREQ}$  Frequency Selector Diagram

## 2.8 Regulators

The chip provides a 5 V output to power LEDs or optocouplers. This is a closed-loop regulator, which ensures accurate output voltage. The 5 V regulator is supplied by an internal 11 V open loop regulator, which also provides power for the external FET gate drivers. The 11 V regulator is supplied by a coarse regulator, which is also open-loop. With the Si34061 and Si34062, the VT15 pin can be used to supply this regulator from an optional auxiliary transformer winding. The advantage of doing so is additional power saving since the external FET drivers' current is not generated from the PoE 50 V but, rather, from a transformer-provided 12–16 V. The application must be designed to ensure that the absolute maximum rating voltage for the VT15 pin is not exceeded.

## 2.9 Sleep Mode

The Si3406, Si34061, and Si34062 have automatic (consumption-based) and non-automatic sleep modes. When SLEEPb is tied to ground, the automatic sleep mode is enabled, meaning that if the current consumption is lower than IMPSt<sub>h</sub>, the chip will automatically generate MPS pulses to the PSE. If SLEEPb is tied to VDD, then it will not generate MPS pulses, and the PSE will disconnect if total application current consumption drops below 5–10 mA.

For non-automatic sleep mode, tie SLEEPb high at initial startup (right after the hotswap switch turns on). The chip turns OFF automatic mode, but pulling SLEEPb low will force MPS generation as long as the pin is held low. Using this mode, the designer can control MPS generation.

## 2.10 Extended Sleep Mode

In the Si34062, an extended sleep mode is available which includes LED, WAKE, and MODE pin support. The LED pin drives a light emitting diode to (for example) illuminate a button on the primary side of the application. The WAKE pin triggers wakeup, and the MODE button controls if MPS generation is enabled in sleep. In the Si34062 case, nSLEEP is used to initiate sleep.

The sleep mode is initiated by a negative transition on nSLEEP. It is latched at that negative transition event together with MODE, so their status is kept until wakeup even if the input changes on these pins due to the secondary side losing power. MPS generation is enabled if MODE = 0 at the nSLEEP transition. The following figure shows the Si34062 sleep mode behavior.

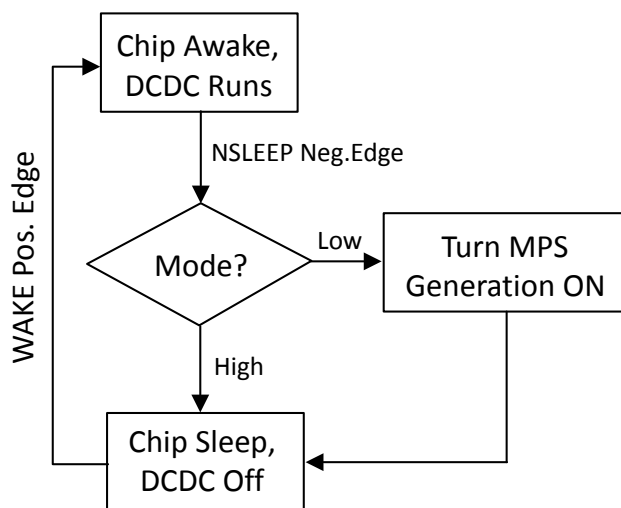


Figure 2.8. Si34062 Extended Sleep Mode Behavior

Refer to [Figure 3.3 Si34062 ISO Flyback Application Diagram on page 13](#), which shows shows the connectivity for the Si34062 with the extended sleep mode.

## 2.11 External Wall Support

The Si3406x supports using a wide voltage range of external wall adapters as a primary or secondary supply. For details on options and supported modes of adapter connection, please refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

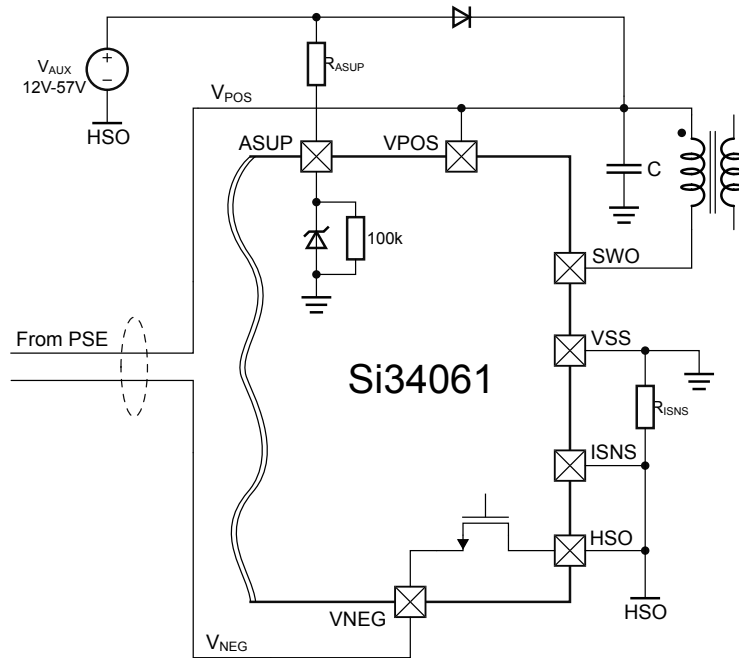


Figure 2.9. Example Auxiliary Wall Adapter Connection

### 3. Application Examples

The following diagrams demonstrate the ease of use and straightforward BOM of the Si3406x Powered Device ICs. Detailed reference designs are available in Evaluation KIT User Guides. Also refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

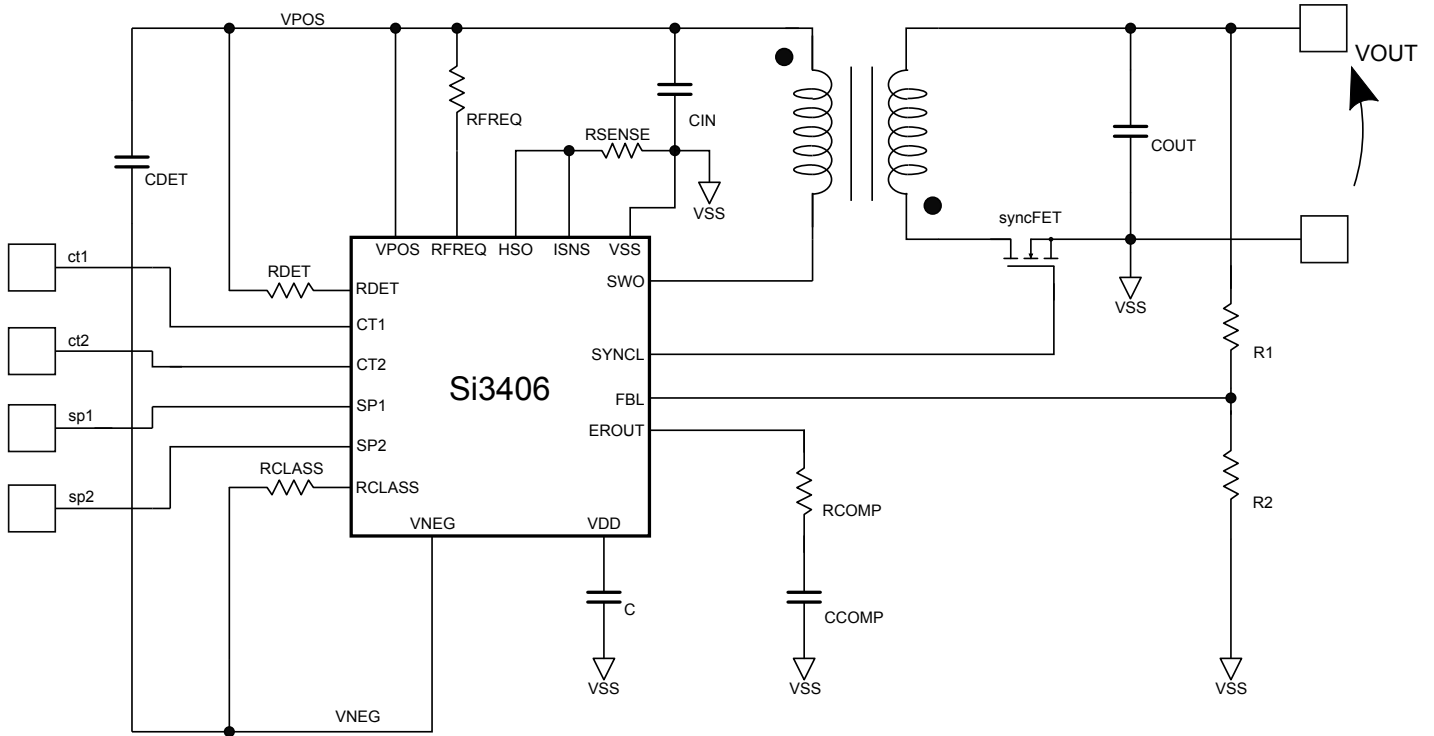


Figure 3.1. Si3406 Non-ISO Flyback Application Diagram

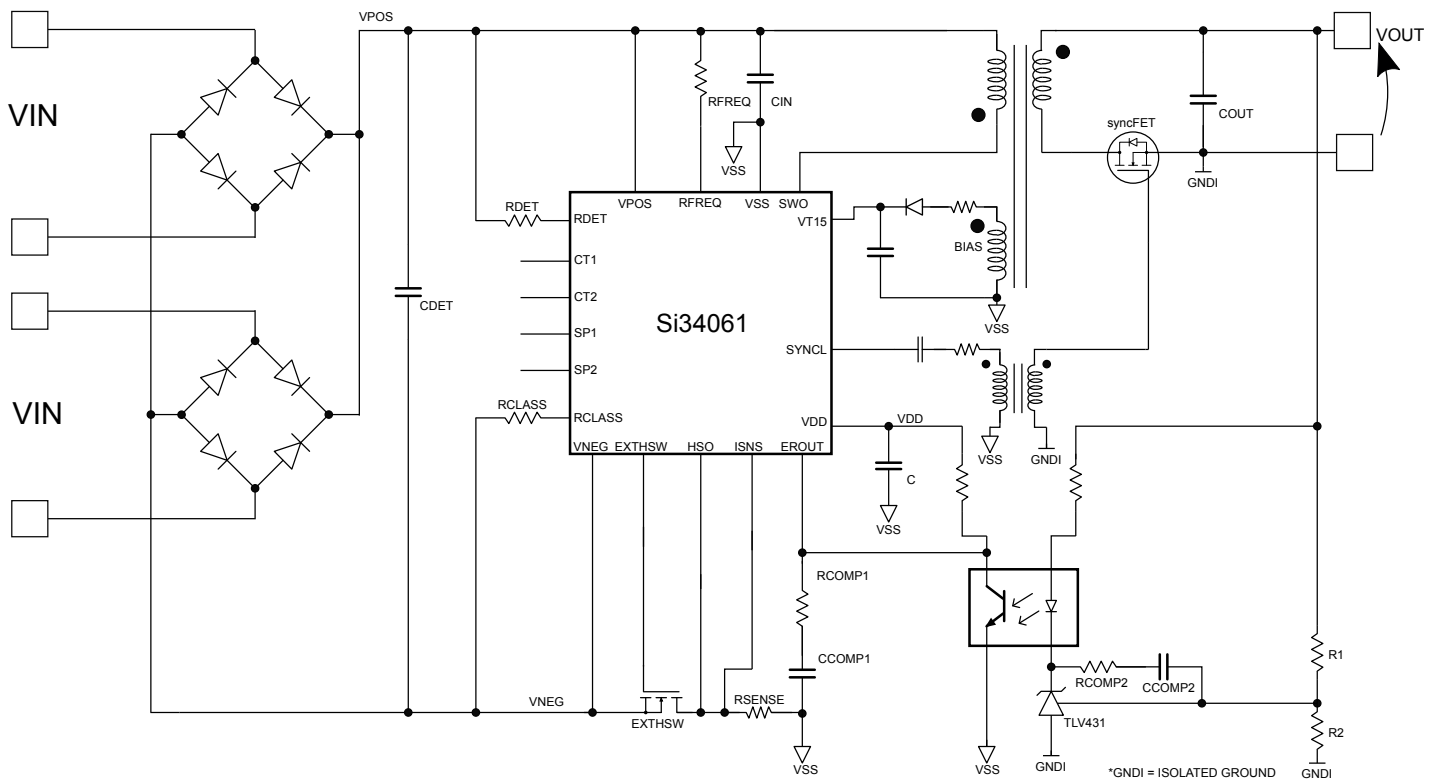


Figure 3.2. Si34061 ISO Flyback Application Diagram



## 4. Electrical Specifications

Table 4.1. Absolute Maximum Ratings<sup>1</sup>

Type	Description	Min	Max	Units
Voltage	CT1–CT2 or SP1–SP2	–100	100	V
	VNEG-VSS, VPOS- VNEG, HSO <sup>2</sup> , RDET <sup>3</sup>	–0.7	100	V
	SWO-VSS	–0.7	120	V
	ISNS, SWISNS	–1	1	V
	Low Voltage pins: FBH <sup>3</sup> , EROUT, FBL, NSLEEP, RCL <sup>2</sup> , RFREQ <sup>3</sup> , ASUP <sup>3</sup> , WAKE, MODE, LED	–0.7	6	V
	Mid Voltage pins: SYNCL, VT15, EXTGD, EXTHSW	–0.7	18	V
	Other Mid Voltage pin: V11	–0.7	12	V
Peak Current	CT1, CT2, SP1, SP2, VPOS	–TBD	TBD	A
DC Current <sup>4</sup>	CT1, CT2, SP1, SP2	–0.2	0.2	A
Temperature	Storage Temperature	–65	150	°C
	Ambient Operating Temperature	–40	85	

**Note:**

1. Unless otherwise noted, all voltages referenced to VSS. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Voltage referenced to VNEG.
3. Voltage referenced to VPOS.
4. Higher dc current is possible in the application, but only utilizing external bridge diodes. Refer to reference design documentation and AN1130 for further details.

Table 4.2. Recommended Operating Conditions

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
V <sub>PORT</sub>	CT1 – CT2  or  SP1 – SP2	2.7	—	57	V
V <sub>HV_OP</sub>	VNEG-VSS, VNEG-HSO, VPOS-VSS	2.7	—	57	V
V <sub>LV_OP</sub>	VPOS referred low voltage pins: RFREQ, RDET, FBH	–5.5	—	0	V
V <sub>LV_OP</sub>	VSS referred low voltage pins: VDD, FBL, EROUT, ASUP, nSLEEP, nT2P, ASUP, WAKE, MODE, LED	0	—	5.5	V
V <sub>OH_DIG</sub>	V <sub>OH</sub> of ASUP and nT2P relative to VSS.	3	—	—	V
V <sub>ISNS_OP</sub>	VSS referred current sensing pins: ISNS, SWISNS	–0.5	—	0.5	V
V <sub>LV_OP</sub>	VNEG referred low voltage pins: RCL	0	—	5.5	V
V <sub>MV_OP</sub>	VSS referred medium voltage pins SYNCL, EXTGD, EXTHSW	0	—	13	V
V <sub>MV_VT15</sub>	VSS referred medium voltage pin VT15 <sup>1</sup>	12	14.5	16.5	V
I <sub>RECT</sub>	On chip rectifier current on CT1, CT2, SP1, SP2—steady state <sup>2</sup>	—	—	176	mA
V <sub>RECT</sub>	On chip rectifier voltage @ 200 mA, 2 diodes	—	1.8	—	V
I <sub>RECT_PK</sub>	Peak rectifier current Max 75 ms 5% Duty Cycle <sup>3</sup>	—	—	231	mA
I <sub>AVG</sub>	Allowable continuous current on SWO, VSS, HSO, VNEG	—	—	600	mA
I <sub>PEAK</sub>	Peak current on SWO, VSS, HSO, VNEG Max 75 ms 5% Duty Cycle	—	—	683	mA

**Note:**

1. V<sub>MV\_VT15</sub> is relevant for Si34061 and Si34062 only when an external auxiliary winding from the primary side of the transformer is being used to improve power conversion efficiency. This can be left undriven, in which case an internal regulator will be used.
2. For Class 3 and above operation, use external diode bridge rectifiers to bypass the internal input diode bridge rectifiers.
3. The IEEE 802.3at specification allows for higher peak current for transients.

Table 4.3. Electrical Characteristics

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
<b>PoE PROTOCOL</b>					
<b>Detection</b>					
V <sub>DET</sub>	Detection Voltage (at V <sub>PORT</sub> )	2.7	—	10.1	V
<b>Classification</b>					
V <sub>RESET</sub>	Classification Reset (at V <sub>PORT</sub> )	0	—	2.81	V
V <sub>CLASS</sub>	Classification Voltage (at V <sub>PORT</sub> )	14.5	—	20.5	V
I <sub>PortCLASS</sub>	Class 0 (R <sub>CLASS</sub> > 681 Ω)	0	—	4	mA
	Class 1 (R <sub>CLASS</sub> = 140 Ω @ 1%)	9	—	12	mA
	Class 2 (R <sub>CLASS</sub> = 75 Ω @ 1%)	17	—	20	mA
	Class 3 (R <sub>CLASS</sub> = 48.7 Ω @ 1%)	26	—	30	mA
	Class 4 (R <sub>CLASS</sub> = 33.2 Ω @ 1%)	36	—	44	mA
<b>Type 2 Classification</b>					
V <sub>MARK</sub>	Mark event voltage (at V <sub>PORT</sub> )	6.9	—	10.1	V
I <sub>MARK</sub>	Mark event current	0.25	TBD	4	mA
<b>Power On and UVLO</b>					
V <sub>UVLO_R</sub>	Hotswap closed and converter on	—	37	—	V
V <sub>UVLO_F</sub>	Hotswap open and converter off	—	32	—	V
<b>Thermal Characteristics</b>					
T <sub>shd</sub>	Thermal shutdown	—	160	—	°C
T <sub>HYST</sub>	Thermal shutdown hysteresis	—	20	—	°C
<b>On-Chip Transient Voltage Suppression/Protection</b>					
T <sub>PROT</sub>	TVS protection activation voltage (VPOS-VNEG)	100	—	—	V
<b>Hotswap Switch</b>					
I <sub>inrush</sub>	Inrush current	100	170	200	mA
I <sub>MAXHSSW</sub>	Maximum continuous operating current	—	—	600	mA
V <sub>HSSW_ON</sub>	Switch ON voltage	—	380	—	mV
V <sub>HSSW_OFF</sub>	Switch OFF voltage, HSSW goes to overload cycle	—	3.5	—	V
I <sub>OVL</sub>	Switch current limit in OVERLOAD State	8.7	10.5	12.4	mA
I <sub>MPSth</sub>	MPS signal request current level threshold	14	20	26	mA
I <sub>EXT_DRV</sub>	External hotswap driver peak current on EXTHSW pin	—	—	10	mA



Symbol	Parameter (Condition)	Min	Typ	Max	Unit
V <sub>EXT_DRV</sub>	External hotswap driver voltage on EXTHSW pin	9	11	—	V
T <sub>WAITHSSW</sub>	Wait time in OVERLOAD and type 2 inrush	80	96	116	ms
R <sub>ONHSSW</sub>	Internal hotswap drain-source resistance while ON	0.65	1.5	2.9	Ω
<b>DC-DC</b>					
I <sub>SWOPEAK</sub>	Peak current limit of internal FET (SWO pin)	2.1	—	2.7	A
V <sub>EXTGD</sub>	External FET driver voltage (EXTGD pin)	9	11	13	V
I <sub>EXTGD</sub>	External FET driver peak current (EXTGD pin)	—	—	500	mA
F <sub>OSCINT</sub>	Using internal Oscillator	—	250	—	kHz
F <sub>OSCEXT</sub>	Using external Oscillator, tunable on pin RFREQ	100	—	500	kHz
DUC	Output duty cycle of PWM	—	TBD	75	%
V <sub>DCDCUVLO</sub>	DCDC UVLO level (Minimum adapter voltage)	10.2	10.7	11.3	V
V <sub>FBREF</sub>	FBH (referenced to VPOS) and FBL (referenced to VSS) reference voltage	—	1.32	—	V
V <sub>EROUT</sub>	Operating voltage range of error input	1	—	4	V
V <sub>ISNS_OVC</sub>	Overcurrent limit voltage on ISNS (ref. to VSS)	—	-270	—	mV
V <sub>ISNS_LC</sub>	Low current limit voltage on ISNS (ref. to VSS)	—	-30	—	mV
V <sub>SWISNSMAX</sub>	External FET current sense	—	240	—	mV
T <sub>SOFTSTART</sub>	Startup time	—	4	—	ms
R <sub>ONDCDC</sub>	Internal DCDC switching FET drain-source resistance while ON	—	0.9	1.2	Ω
<b>Regulators</b>					
VT15	Override internal regulator with transformer winding	13	—	16.5	V
VDD	High accuracy 5 V	4.85	5.1	5.46	V
VDD <sub>ILIM</sub>	DC current limit of VDD	9.7	11.2	12.9	mA
C <sub>REG</sub>	Filter capacitor on VDD and V11	—	100	—	nF
I <sub>MAXLED</sub>	LED pin max current, reduces VDD <sub>ILIM</sub>	—	5	—	mA
I <sub>MAXDO</sub>	Digital output max current (NT2P), reduces VDD <sub>ILIM</sub>	2	2.5	—	mA
<b>Power Dissipation</b>					

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
$P_{INTMAX}$	DC-DC max power internal FET	—	1.2	1.5	W
$P_{MAX}$	Total chip power	—	TBD	TBD	W
$I_{PortOP}$	Operating current ( $V_{PORT}$ 57 V; 250 kHz)	—	3	4	mA
<b>Package Thermal Characteristics</b>					
$\theta_{JA-EFF}$	QFN20	—	44	—	C°/W
$\theta_{JA-EFF}$	QFN24	—	TBD	—	C°/W

## 5. Pin Descriptions

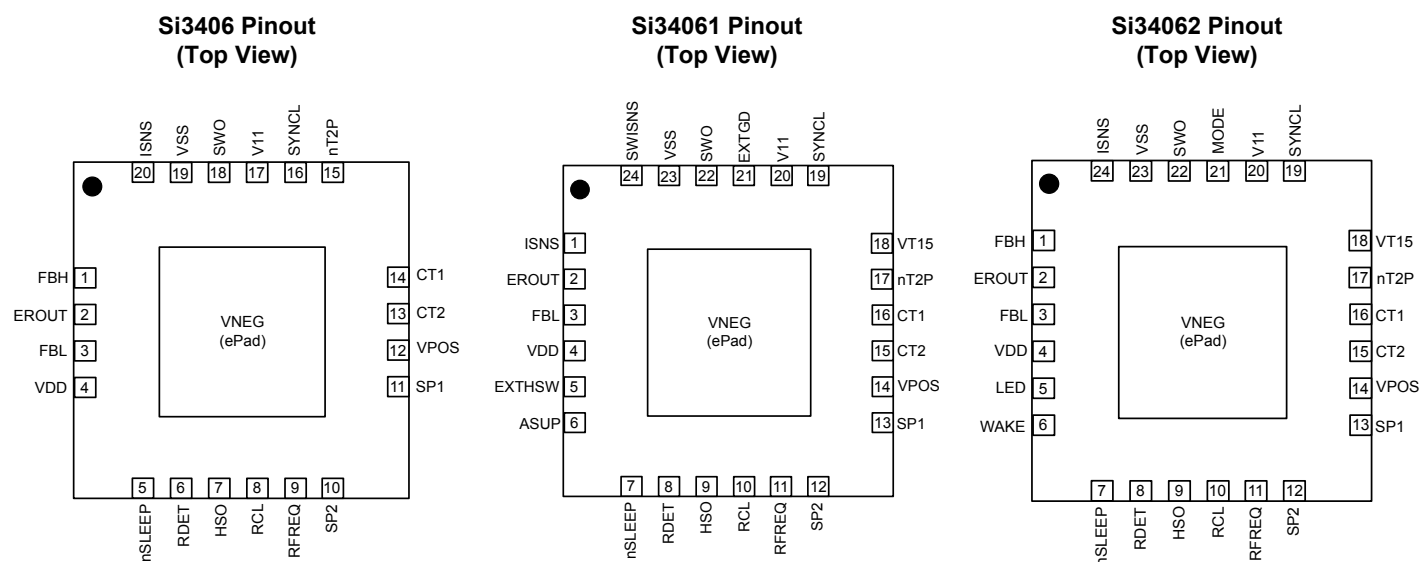


Table 5.1. Pin Descriptions

'06 Pins	'061 Pins	'062 Pins	Name	Ref	Dir.	Vrange	Description
	24	24	SWISNS	VSS	I	0–0.5	External FET peak current sense resistor voltage input
20	1		ISNS	VSS	I	-0.5–0	Chip average current sense resistor input
1		1	FBH	VPOS	I	0–5	High side (VPOS referred) dcdc feedback (buck converter)
2	2	2	EROUT	VSS	IO	0–5	Error amplifier current output, compensation impedance input
3	3	3	FBL	VSS	I	0–5	Low side (ground referenced) dcdc feedback (flyback converter)
4	4	4	VDD	VSS	O	0–5	5V regulator output
		5	LED	VSS	O	0–5	Output to drive sleep LED
	5		EXTHSW	VNEG	O	0–11	External hotswap switch drive
		6	WAKE	VSS	I	0–5	Wakeup from sleep mode
	6		ASUP	VSS	I	0–5	AUX auxiliary adapter present
5	7	7	nSLEEP	VSS	I	0–5	Sleep, with pull-up, driven by open drain
6	8	8	RDET	VPOS	IO	0–100	Detection resistor
7	9	9	HSO	VNEG	IO	0–100	Hotswap switch output
8	10	10	RCL	VNEG	IO	0–5	Classification resistor
9	11	11	RFREQ	VPOS	IO	0–5	Oscillator frequency tuning resistor, tie to VPOS to select default freq
10	12	12	SP2	SP1	I	0 - 100	High-voltage supply input from spare pair; polarity-insensitive
11	13	13	SP1	SP2	I	0–100	High-voltage supply input from spare pair; polarity-insensitive
12	14	14	VPOS	—	IO	0–100	Rectified high-voltage supply positive rail
13	15	15	CT2	CT1	I	0–100	High-voltage supply input from main pair; polarity-insensitive
14	16	16	CT1	CT2	I	0 - 100	High-voltage supply input from main pair; polarity-insensitive

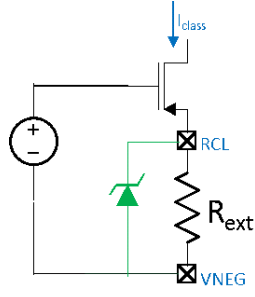
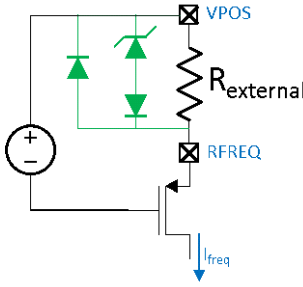
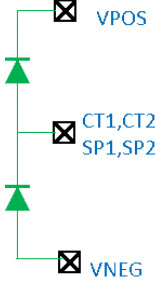
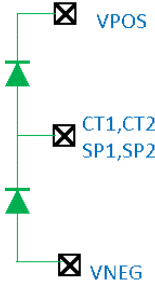
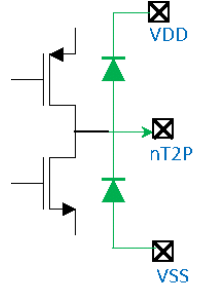
'06 Pins	'061 Pins	'062 Pins	Name	Ref	Dir.	Vrange	Description
15	17	17	nT2P	VSS	O	0–5	Type II classification was successful
	18	18	VT15	VSS	I	0–16.5	Dcdc transformer bias winding input
16	19	19	SYNCL	VSS	O	0–11	Gate driver for synchronous rectification FET
17	20	20	V11	VSS	IO	0–11	11 V regulator output for filter cap.
	21		EXTGD	VSS	O	0–11	External FET gate drive. When internal switching FET is in use, tie to VSS.
		21	MODE	VSS	I	0–5	Controls MPS and LED switch behavior
18	22	22	SWO	VSS	O	0–120	Internal dcdc switch output (NMOS drain)
19	23	23	VSS	—	IO	0	Dcdc converter primary ground
ePad	ePad	ePad	VNEG	—	IO	0	Rectified high voltage supply ground

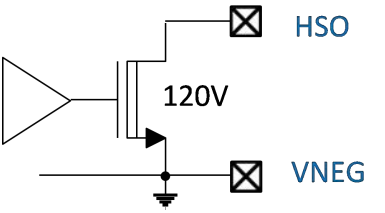
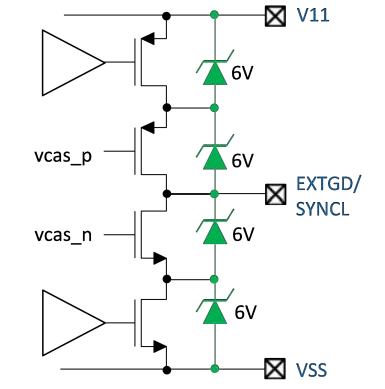
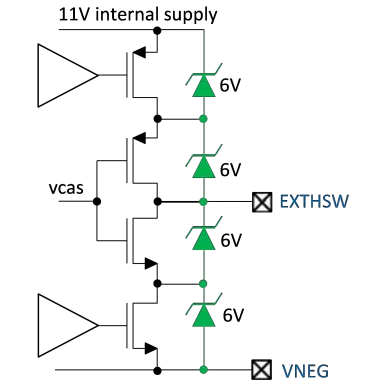
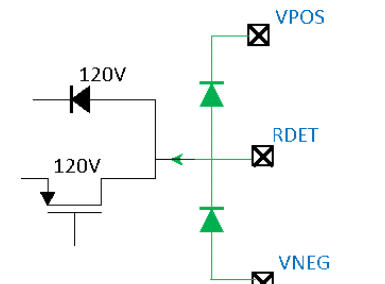
5.1 Detailed Pin Descriptions

Table 5.2. Circuit Equivalent and Description of Die Pads

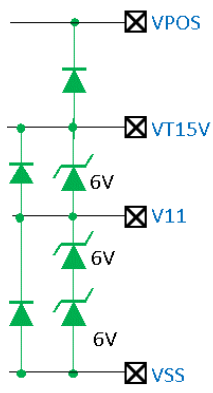
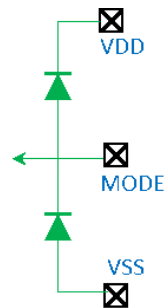
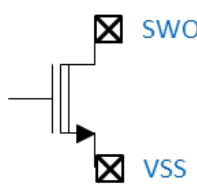
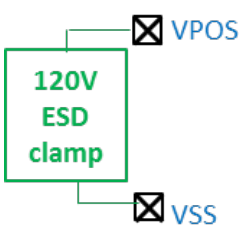
Pin Name	Detailed Description	Circuit Detail
SWISNS	External dcdc switching FET peak current sense resistor input. The maximum current of the switching FET should correspond to voltage $V_{SWISNS-SMAX}$ .	
ISNS	Average current sense resistor input. The resistor value will set the maximum allowed average current for the application. The overcurrent threshold voltage $V_{ISNS\_OVC}$ . Note that this pin voltage goes below VSS.	
FBH	High side dcdc feedback input. Need to be tied to VPOS when not used. See VFBREF.	
EROUT	dcdc converter error output; current out, voltage sense. Loop compensating impedance should be connected here. $I_{EROUT} = (V_{FBH} - V_{FBREF}) \times 50 \mu A$ or $I_{EROUT} = (V_{FBL} - V_{FBREF}) \times 50 \mu A$	
FBL	Low side dcdc feedback input. Need to be tied to VSS when not used. See VFBREF	

Pin Name	Detailed Description	Circuit Detail
VDD	<p>Regulated 5 V relative to VSS. There is no foldback characteristic, reaching <math>VDD_{ILIM}</math> the output voltage decreases.</p> <p>The regulator needs <math>C_{REG}</math> external capacitance.</p>	
LED	<p>LED driver output Max current is <math>I_{MAXLED}</math></p>	
WAKE	<p>Wake-up input pin for sleep mode, used only in Si34062.</p>	
ASUP	<p>Auxiliary supply adapter is present. Enables the operation of the dc/dc controller without PoE supply being present.</p>	
nSLEEP	<p>Sleep function input, see description in Sleep mode section.</p>	

Pin Name	Detailed Description	Circuit Detail
RCL	Classification resistor input. For class 0 this pin can be left floating. Pin is active only at time of classification.	
RFREQ	Used for adjusting the oscillator frequency. The frequency is inversely proportional to the value of the connected resistor.	
SP1, SP2 CT1, CT2	Main power inputs, goes to diode bridge producing VPOS and VNEG.	
VPOS, VNEG	Main chip power output generated by the diode bridge. Note that VNEG (the ePad on the bottom of the chip) also provides thermal relief.	
nT2P	Pin main function is digital output; it is low if Type 2 classification was successful and the application is allowed to draw class 4 current. Output current is $I_{MAXDO}$ , but the load (e.g. an LED) should be connected to VDD not VSS; otherwise, it can cause false operation.	

Pin Name	Detailed Description	Circuit Detail
HSO	Hotswap Switch Output. The switch shorts the VNEG and HSO pins, and includes several other functions. See hotswap switch section for details.	 <p>The diagram shows a 120V switch controlled by a logic input. One terminal of the switch is connected to the HSO pin, and the other terminal is connected to the VNEG pin. The VNEG pin is also connected to ground.</p>
EXTGD, SYNCL	<p>EXTGD: Optional external switch driver of the dc/dc converter. When the internal switch is used this pin should be tied to VSS. This driver controls the external switch with 10 V logic level, relative to VSS.</p> <p>SYNCL: Optional synchronous rectifier switch driver of the dc/dc converter. When not used the pin must be left floating. This driver controls the external synchronous switch with 10 V logic level, relative to VSS.</p>	 <p>The diagram shows a driver circuit for the EXTGD/SYNCL pins. It consists of two NMOS transistors. The gates are driven by logic inputs. The drains are connected to V11 and VSS. The sources are connected to the EXTGD/SYNCL pins. There are 6V diodes in series with the gates and sources.</p>
EXTHSW	Optional external hotswap switch output. The maximum current of the internal hotswap switch is $I_{MAXHSSW}$ , for higher currents an external NMOS FET should be used parallel to the internal HSSW (VNEG-HSO). When EXTGD is not used the pin should be tied to VNEG. This driver controls the external switch with 10 V logic level, relative to VNEG.	 <p>The diagram shows a driver circuit for the EXTHSW pin. It consists of two NMOS transistors. The gates are driven by logic inputs. The drains are connected to an 11V internal supply and VNEG. The sources are connected to the EXTHSW pin and VNEG. There are 6V diodes in series with the gates and sources.</p>
RDET	The user has to tie the RDET resistor between this pin and VPOS. During detection, a high voltage switch pulls down RDET to VNEG. After detection, the reference block uses RDET as absolute chip current reference, forcing -750 mV relative to VPOS, creating 30 $\mu$ A for the internal blocks.	 <p>The diagram shows a circuit for the RDET pin. A 120V switch is connected to the RDET pin and VNEG. A resistor is connected between the RDET pin and VPOS. The VNEG pin is also connected to ground.</p>



Pin Name	Detailed Description	Circuit Detail
<p>VT15, V11</p>	<p>VT15 is input for an optional 15 V supply generated by an auxiliary transformer bias winding. If the bias winding voltage is lower than VT15, the internal 15 V coarse regulator will provide the current for the 11 V regulator.</p> <p>The V11 pin is for filtering capacitor for the 11 V regulator. A capacitor of value <math>C_{REG}</math> is required.</p>	
<p>MODE</p>	<p>MPS mode control, used in Si34062.</p>	
<p>SWO</p>	<p>Dcdc converter switching transistor drain output, <math>V_{max} = 120 V</math>.</p>	
<p>VSS</p>	<p>DC-DC converter ground.</p>	

## 6. Packaging

### 6.1 Package Outline: Si3406

The figure below illustrates the package details for the Si3406. The table lists the values for the dimensions shown in the illustration.

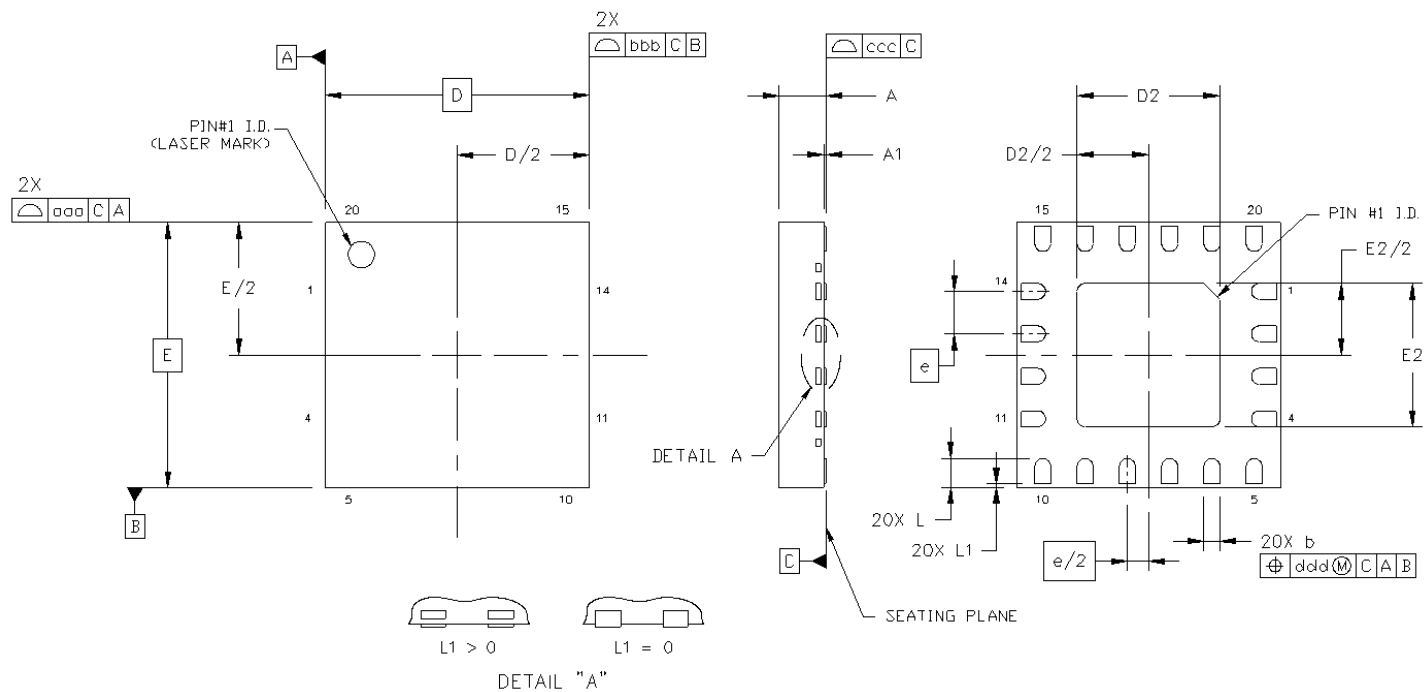


Figure 6.1. 20-Pin, QFN Package

Table 6.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D	5.00 BSC.		
D2	2.60	2.70	2.80
e	0.80 BSC.		
E	5.00 BSC.		
E2	2.60	2.70	2.80
L	0.50	0.55	0.60
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Dimension	Min	Nom	Max
-----------	-----	-----	-----

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHB-1.

## 6.2 Land Pattern: Si3406

The figure below illustrates the land pattern details for the Si3406. The table lists the values for the dimensions shown in the illustration.

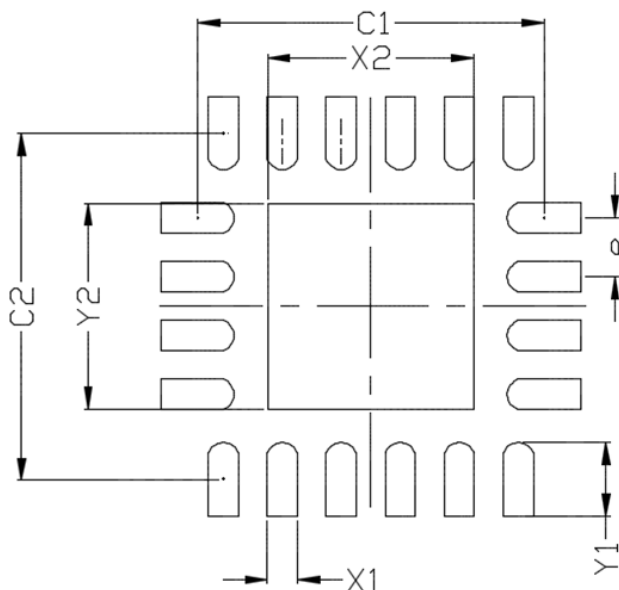


Figure 6.2. 20-Pin, QFN Land Pattern

Table 6.2. Land Pattern Dimensions

Dimension	Max
C1	4.70
C2	4.70
X1	0.35
X2	2.80
Y1	1.00
Y2	2.80
e	0.80

### Note:

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

#### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.3 Package Outline: Si34061/62

The figure below illustrates the package details for the Si34061/62. The table lists the values for the dimensions shown in the illustration.

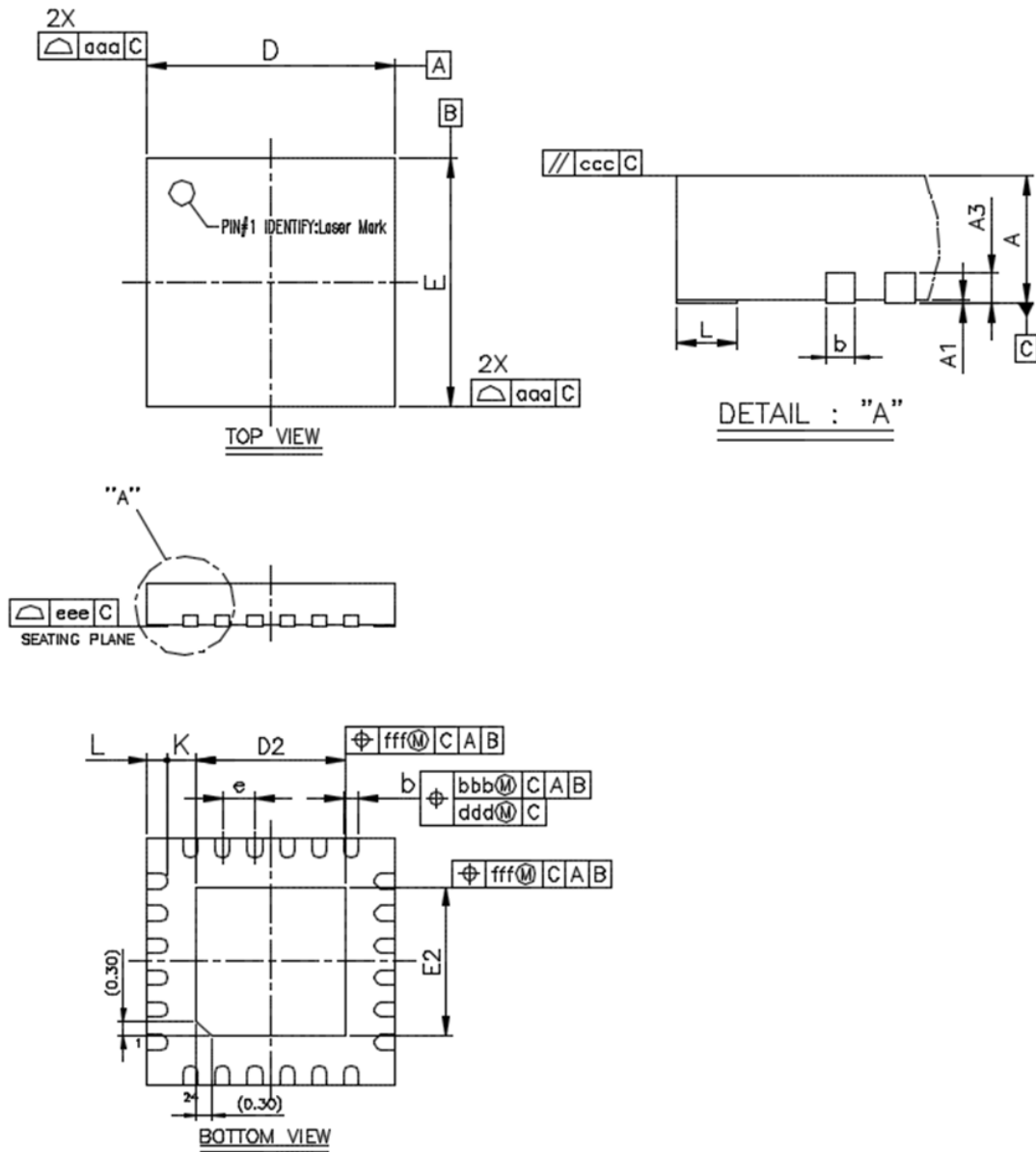


Figure 6.3. 24-Pin, QFN Package

Table 6.3. Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
A3		0.20 REF	
D		5.00 BSC.	
e		0.65 BSC.	
E		5.00 BSC.	

Symbol	Min	Nom	Max
D2	2.90	3.00	3.10
E2	2.90	3.00	3.10
L	0.35	0.40	0.45
K	0.20	—	—
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6.4 Land Pattern: Si34061/62

The figure below illustrates the land pattern details for the Si34061/62. The table lists the values for the dimensions shown in the illustration.

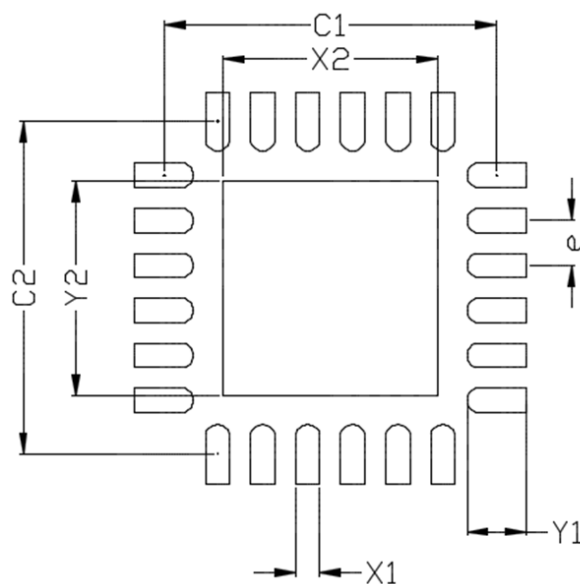


Figure 6.4. 24-Pin, QFN Land Pattern

Table 6.4. Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
X1	0.35
X2	3.10
Y1	0.85
Y2	3.10
e	0.65

### Note:

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted
2. This land pattern design is based on the IPC-7351 guidelines

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

#### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release
2. The stencil thickness should be 0.125 mm (5 mils)
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Top Markings

### 7.1 Si3406 Top Marking



Figure 7.1. Si3406 Top Marking

Table 7.1. Si3406 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Pin 1 Mark:</b>	Circle = 0.50 mm Diameter (Lower-Left Corner)	
<b>Font Size:</b>	2.0 Point (28 mils)	
<b>Line 1 Mark Format:</b>	Device Part Number	Si3406
<b>Line 2 Mark Format:</b>	Device Type	A = Device Revision A G = Extended temperature range M = QFN package
<b>Line 3 Mark Format:</b>	TTTTTT	Manufacturing Trace Code (assigned at assembly)
<b>Line 4 Mark Format:</b>	YY = Year WW = Work Week	Assembly Year Assembly Week



## 7.2 Si34061 Top Marking

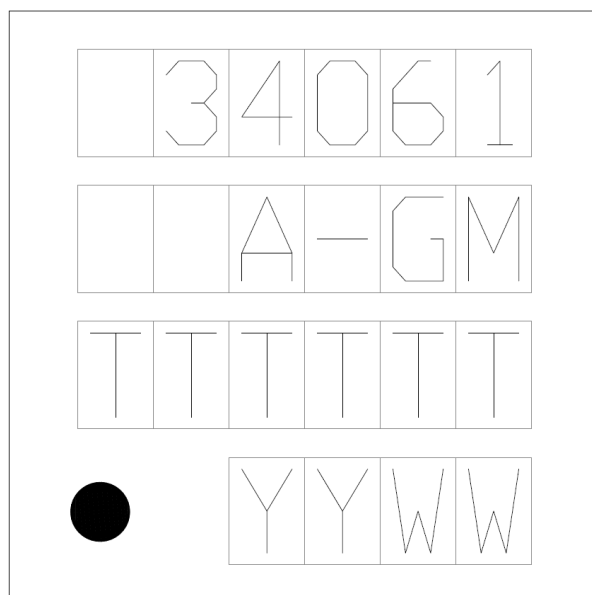


Figure 7.2. Si34061 Top Marking

Table 7.2. Si34061 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Pin 1 Mark:</b>	Circle = 0.50 mm Diameter (Lower-Left Corner)	
<b>Font Size:</b>	2.0 Point (28 mils)	
<b>Line 1 Mark Format:</b>	Device Part Number	Si34061
<b>Line 2 Mark Format:</b>	Device Type	A = Device Revision A G = Extended temperature range M = QFN package
<b>Line 3 Mark Format:</b>	TTTTTT	Manufacturing Trace Code (assigned at assembly)
<b>Line 4 Mark Format:</b>	YY = Year WW = Work Week	Assembly Year Assembly Week

## 7.3 Si34062 Top Marking

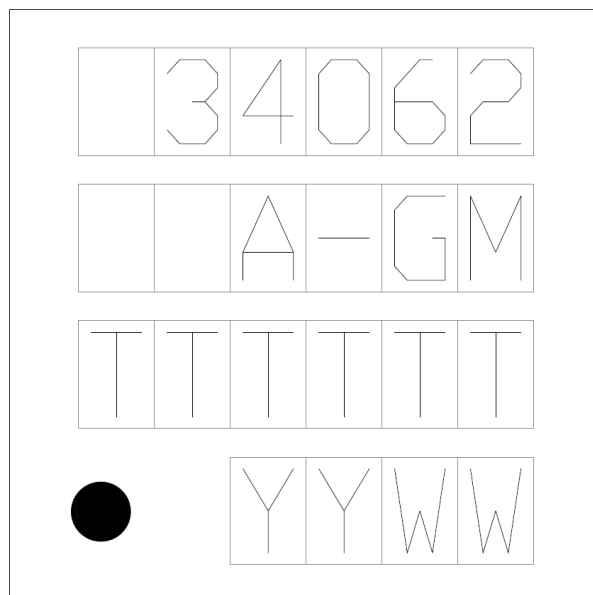


Figure 7.3. Si34062 Top Marking

Table 7.3. Si34062 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Pin 1 Mark:</b>	Circle = 0.50 mm Diameter (Lower-Left Corner)	
<b>Font Size:</b>	2.0 Point (28 mils)	
<b>Line 1 Mark Format:</b>	Device Part Number	Si34062
<b>Line 2 Mark Format:</b>	Device Type	A = Device Revision A G = Extended temperature range M = QFN package
<b>Line 3 Mark Format:</b>	TTTTTT	Manufacturing Trace Code (assigned at assembly)
<b>Line 4 Mark Format:</b>	YY = Year WW = Work Week	Assembly Year Assembly Week

## 8. Revision History

### Revision 0.5

February, 2018

- Updated [2. System Overview](#) and [3. Application Examples](#).
  - Added theory of operation and application content.
- Updated [Table 4.1 Absolute Maximum Ratings<sup>1</sup> on page 14](#), [Table 4.2 Recommended Operating Conditions on page 15](#), and [Table 4.3 Electrical Characteristics on page 16](#).
  - Clarified multiple parameters.
- Added [5.1 Detailed Pin Descriptions](#).
- Added [6. Packaging](#) including outline and land pattern.

### Revision 0.1

August, 2016

- Initial release.



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