

The T9S0 SCR employs a Center-Fired amplifying gate structure which allows the SCR to be reliably operated at high di/dt and high dv/dt conditions in phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Plating Supplies
- Welding Supplies

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
EXAMPLE: **T9S0082803DH** is an 800V-2850A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{tavg}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
T9S0	800V	08	2850A	28	0	3	DH
	600V	06					
	400V	04			400us typ.	200ma	12"

Revised: 9/22/2009

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	400 - 800	Volts
Average On-State Current, $T_C=70^{\circ}C$	$I_{T(Avg.)}$	2850	A
RMS On-State Current, $T_C=72^{\circ}C$	$I_{T(RMS)}$	4477	A
Average On-State Current, $T_C=55^{\circ}C$	$I_{T(Avg.)}$	3300	A
RMS On-State Current, $T_C=55^{\circ}C$	$I_{T(RMS)}$	5184	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	37,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	34,884	A
Fuse Coordination I^2t , 60Hz	I^2t	5.70E+06	A ² s
Fuse Coordination I^2t , 50Hz	I^2t	6.08E+06	A ² s
Critical Rate-of-Rise of On-State Current Repetitive	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive	di/dt	200	A/us
Critical Rate-of-Rise of Off-State Voltage Linear to $\frac{2}{3}V_{DRM}$	dv/dt	1000	V/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-20 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		0.65	lb
		0.29	Kg
Mounting Force		5500-6000	lbs
		24.5 - 26.7	Knewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

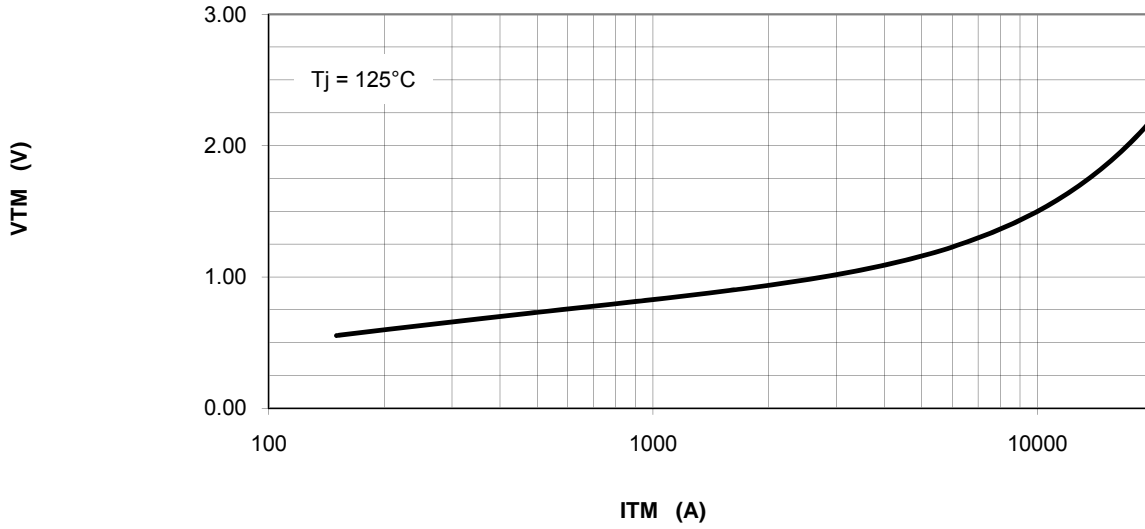
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Leakage Current	I_{DRM}/I_{RRM}	Tj=125°C, V _{DRM} =Rated			150	ma
Peak On-State Voltage	V _{TM}	Tj=25°C, I _{TM} =1500A			1.15	V
V _{TM} Model, Low Level	V ₀	Tj=125°C			0.722	V
V _{TM} = V ₀ + r•I _{TM}	r	15% I _{TM} - π•I _{TM}			8.83E-02	mΩ
V _{TM} Model, High Level	V ₀	Tj=125°C			0.784	V
V _{TM} = V ₀ + r•I _{TM}	r	π•I _{TM} - I _{TSM}			7.11E-02	mΩ
V _{TM} Model, Hiç 4-Term	A	Tj=125°C			-0.342	
V _{TM} = A + B•Ln(I _{TM}) +	B	15%I _{TM} - I _{TSM}			0.199	
C•(I _{TM}) + D•(I _{TM}) ^{1/2}	C				9.66E-05	
	D				-0.00962	
Turn-On Delay Time	t _d	V _D = 0.5•V _{DRM} Gate Drive: 40V - 20Ω		1.5		us
Turn-Off Time	t _q	Tj=125°C dv/dt = 20V/us to 80% V _{DRM}		400		us
Gate Trigger Current	I _{GT}	Tj=25°C V _D = 12V	30	90	200	ma
Gate Trigger Voltage	V _{GT}		0.6	1.6	3.0	V
Peak Reverse Gate Voltage	V _{GRM}				5	V

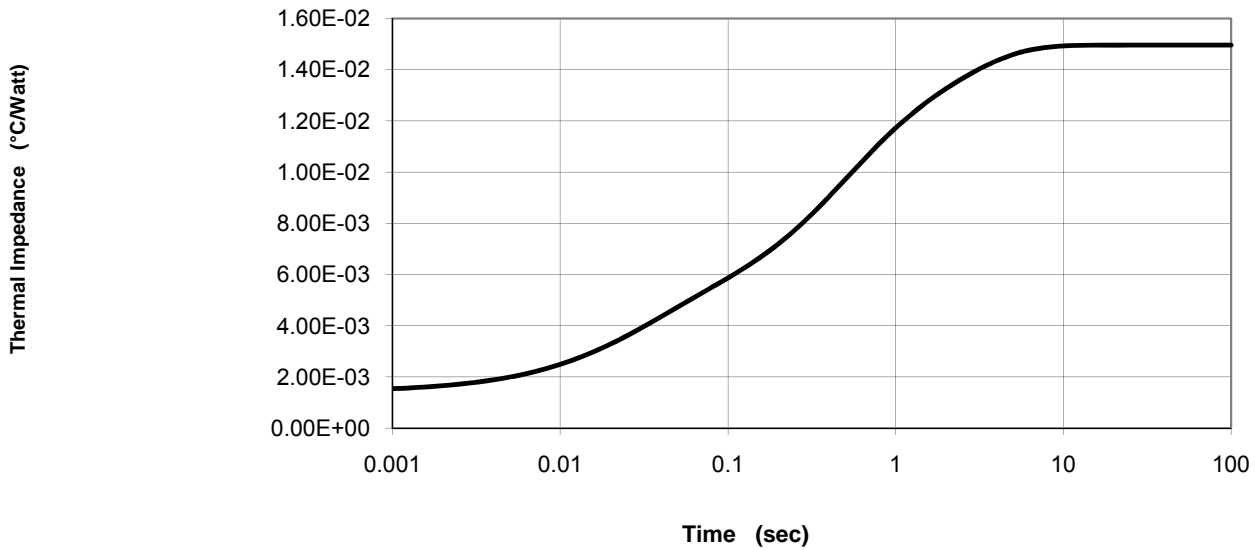
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating				
			max			Units	
Thermal Resistance							
Junction to Case	Rθ _{jc}	Double side cooled			0.015	°C/Watt	
Case to Sink	Rθ _{cs}	Double side cooled			0.0025	°C/Watt	
Thermal Impedance Model							
Zθ _{jc} (t) = Σ(A(N)•(1-exp(-t/Tau(N))))	Zθ _{jc}	Double side cooled					
		where:	N =	1	2	3	4
			A(N) =	1.42E-03	2.97E-03	6.07E-03	4.50E-03
			Tau(N) =	5.95E-05	2.76E-02	4.01E-01	2.00E+00

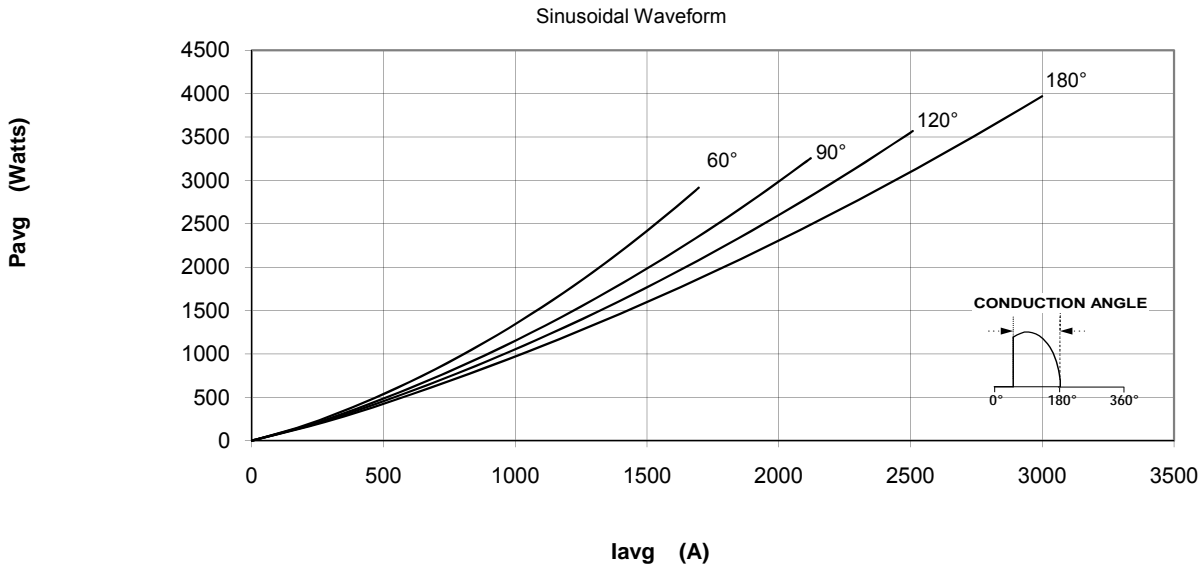
Maximum On-State Voltage Drop



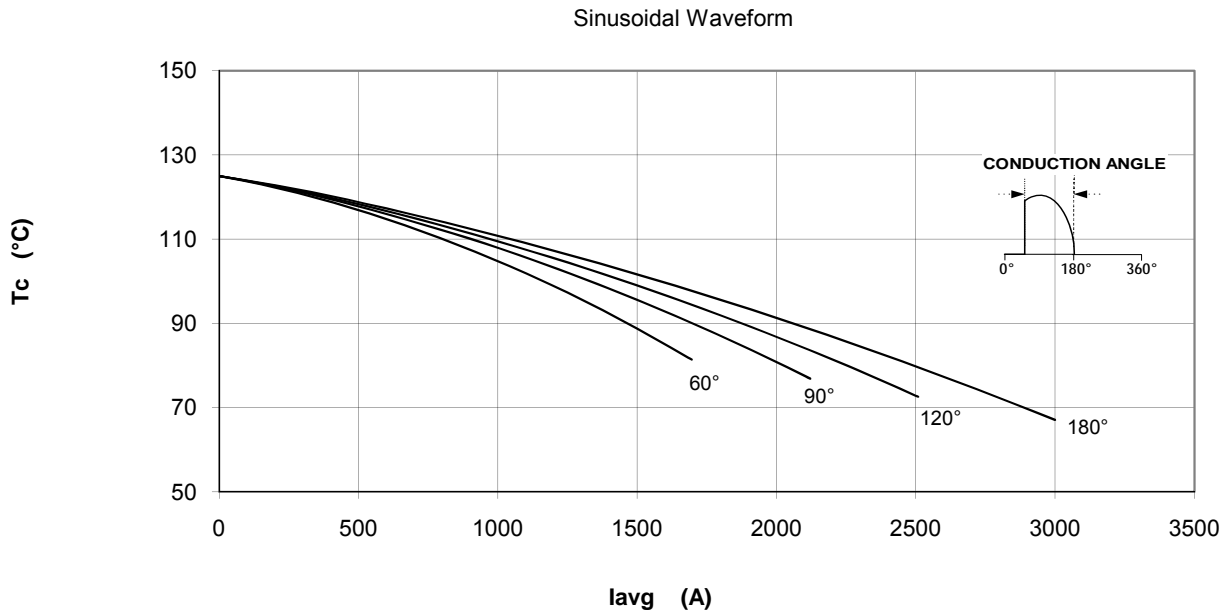
MAXIMUM TRANSIENT THERMAL IMPEDANCE



Maximum On-State Power Dissipation

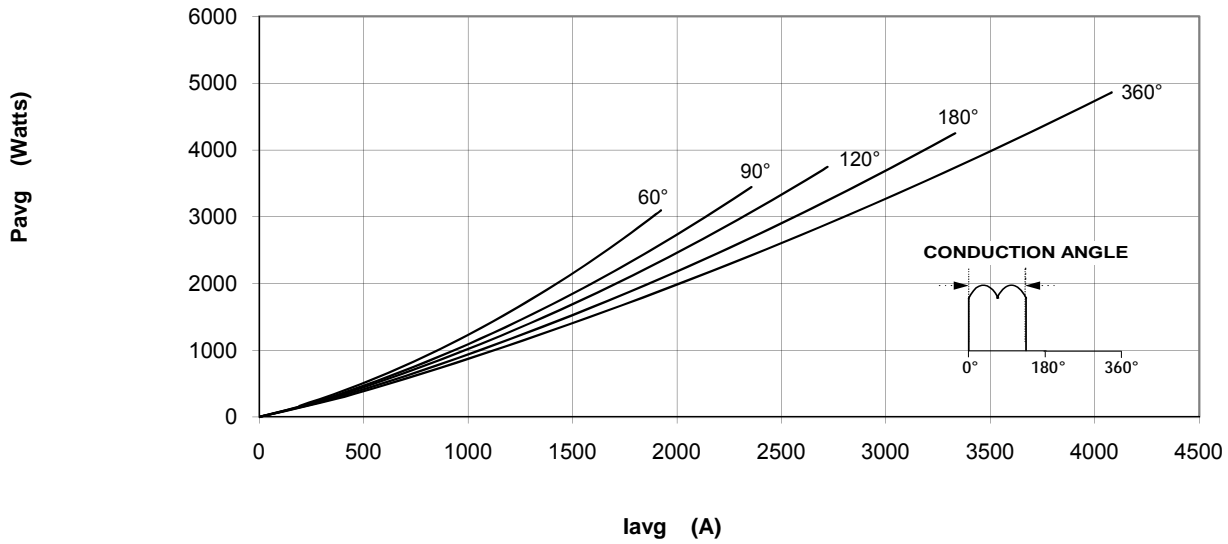


Maximum Allowable Case Temperature



Maximum On-State Power Dissipation

Square Waveform



Maximum Allowable Case Temperature

Square Waveform

