DATA SHEET

TZA1038HW
High speed advanced analog DVD signal processor and laser supply

Product specification

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Philips
Semiconductors

PHILIPS

CONTENTS

High speed advanced analog DVD signal processor and laser supply

TZA1038HW

1 FEATURES

- Operates with DVD-ROM, DVD+RW, DVD-RW, CD-ROM and CD-RW
- Operates up to 64 × CD-ROM and 12 × DVD-ROM
- RF data amplifier with wide, fine pitch programmable noise filter and equalizer equivalent to 64 × CD or 12 × DVD
- Programmable RF gain for DVD-ROM, CD-RW and CD-ROM applications (approximately 50 dB range to cover a large range of disc-reflectivity and OPUs)
- Additional RF sum input
- Balanced RF data signal transfer
- Universal photodiode IC interface using internal conversion resistors and offset cancellation
- Input buffers and amplifiers with low-pass filtering
- Three different tracking servo strategies:
  - Conventional three-beam tracking for CD
  - Differential Phase Detection (DPD) for DVD-ROM, including option to emulate traditional drop-out detection: Drop-Out Concealment (DOC)
  - Advanced push-pull with dynamic offset compensation.
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions
- Radial error signal for Fast Track Counting (FTC)
- RF only mode: servo outputs can be set to 3-state, while RF data path remains active
- Radial servo polarity switch
- Flexible adaption to different light pen configurations
- Two fully automatic laser controls for red and infrared lasers, including stabilization and an on/off switch
- Automatic selection of monitor diode polarity
- Digital interface with 3 and 5 V compatibility.

2 GENERAL DESCRIPTION

The TZA1038HW is an analog preprocessor and laser supply circuit for DVD and CD read-only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between single light path voltage output CD or DVD mechanisms to Philips digital signal processor family for CD and DVD (for example, Gecko, HDR65 or Iguana). A separate high-speed RFSUM input is available.

The device contains several options for radial tracking:

- Conventional three-beam tracking for CD
- Differential phase detector for DVD
- Push-pull with flexible left and right weighting to compensate dynamic offsets e.g. beam landing offset
- A radial error signal to allow Fast Track Count (FTC) during track jumps.

The dynamic range of this preamplifier and processor combination can be optimized for LF servo and RF data paths. The gain in both channels can be programmed separately and so guarantees optimal playability for all disc types.

The RF path is fully DC coupled. The DC content compensation techniques provide fast settling after disc errors.

The device can accommodate astigmatic, single foucault and double foucault detectors and can be used with P-type lasers with N-sub or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant stabilized output power is ensured and is independent of ageing.

An internal Power-on reset circuit ensures a safe start-up condition.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1038HW	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-2

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	ambient temperature		–40	–	+85	°C
Supplies						
V_{DDA1}, V_{DDA2}, V_{DDA3}, V_{DDA4}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD3}	3 V digital supply voltage		2.7	3.3	5.5	V
V_{DDD5}	5 V digital supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	without laser supply	–	98	120	mA
		STANDBY mode	–	–	1	mA
$V_{I(logic)}$	logic input compatibility	note 1	2.7	3.3	5.5	V
Servo signal processing						
$B_{LF(-3dB)}$	–3 dB bandwidth of LF path		60	75	100	kHz
$I_{O(LF)}$	output current	focus servo output	0	–	12	μA
		radial servo output	0	–	12	μA
$V_{O(FTC)(p-p)}$	FTC output voltage (peak-to-peak value)		2.0	–	–	V
B_{FTC}	FTC bandwidth	FTCHBW = 0	–	600	–	kHz
		FTCHBW = 1; note 2	–	1200	–	kHz
$V_{I(FTCREF)}$	FTC reference input voltage		1.25	–	2.75	V
RF data processing						
A_{RF}	linear current gain	programmable gain				
		RF channels	6	–	49	dB
		RFSUM channels	–6	–	+31	dB
$B_{RF(-3dB)}$	–3 dB bandwidth of RFP and RFN signal path	RFEQEN = 0; RFNFEN = 0	200	300	–	MHz
$f_{0(RF)}$	noise filter and equalizer corner frequency	BWRF = 0	8	12.0	14.5	MHz
		BWRF = 127	100	145	182	MHz
$t_{d(RF)}$	flatness delay in RF data path	equalizer on; flat from 0 to 100 MHz; BWRF = 127	–	–	0.5	ns
Z_i	input impedance of pins A to D		100	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(RF)(FS)}$	input voltage on pins A to D for full-scale at output	at the appropriate signal path gain setting				
		RF signal path	–	–	600	mV
		LF signal path	–	–	700	mV
$V_{i(SUM)(dif)}$	differential input voltage on pins RFSUMP and RFSUMN	G_{RFSUM} = −6 dB	–	–	1800	mV
$V_{I(DC)}$	DC input voltage range on pins RFSUMP and RFSUMN	with respect to V_{SS}	1.3	–	V_{DDA} − 1.0	V
$V_{o(RF)(dif)(p-p)}$	differential output voltage on pins RFP and RFN (peak-to-peak value)		–	–	1.4	V
$V_{O(RF)(DC)}$	DC output voltage on pins RFP and RFN		0.35	–	V_{DDA} − 1.9	V
$V_{i(RFREF)(CM)}$	input reference voltage on pin RFREF for common mode output		0.8	1.2	2.1	V
Laser supply						
$I_{o(laser)(max)}$	maximum current output to laser		−120	–	–	mA
$V_{i(mon)}$	input voltage from laser monitor diode	P-type monitor diode				
		LOW level voltage	–	V_{DDA4} − 0.155	–	V
		HIGH level voltage	–	V_{DDA4} − 0.190	–	V
		N-type monitor diode				
		LOW level voltage	–	0.155	–	V
		HIGH level voltage	–	0.185	–	V

Notes

1. Input logic voltage level follows the supply voltage applied at pin V_{DDD3}.
2. High FTC bandwidth is achieved when I_{S1} and I_{S2} > 1.5 μA.

5 BLOCK DIAGRAM

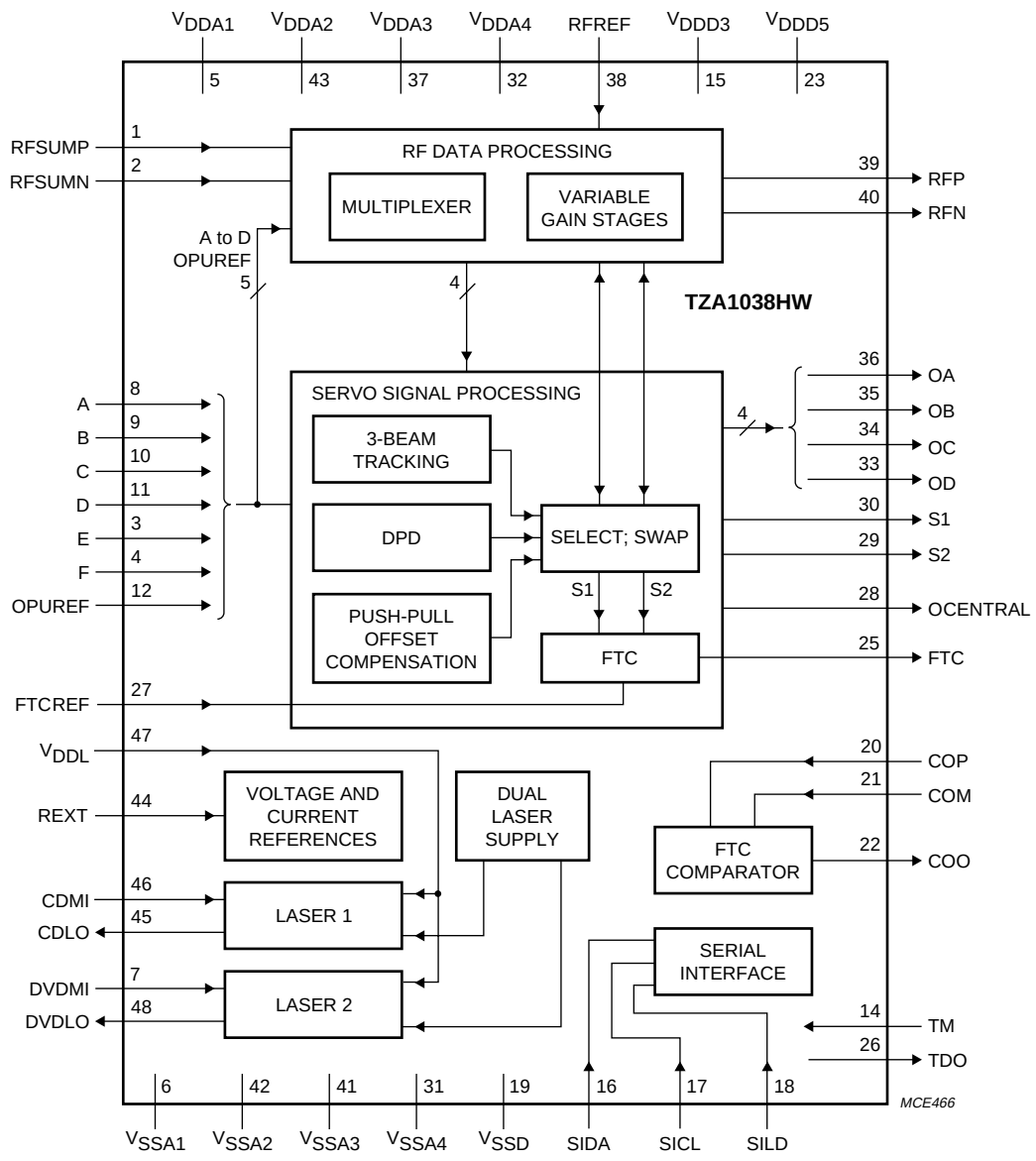


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
RFSUMP	1	positive RF sum input
RFSUMN	2	negative RF sum input
E	3	input E
F	4	input F
V_{DDA1}	5	analog supply voltage 1 (RF input stage)
V_{SSA1}	6	analog ground 1
DVDMI	7	input signal from DVD laser monitor diode
A	8	input A
B	9	input B
C	10	input C
D	11	input D
OPUREF	12	reference input from Optical Pick-Up (OPU)
n.c.	13	not connected
TM	14	test mode input (factory test only)
V_{DDD3}	15	digital supply voltage (serial interface 3 V I/O pads and FTC comparator)
SIDA	16	serial host interface data input
SICL	17	serial host interface clock input
SILD	18	serial host interface load
V_{SSD}	19	digital ground
COP	20	positive FTC comparator input
COM	21	inverting FTC comparator input
COO	22	FTC comparator output
V_{DDD5}	23	digital supply voltage (5 V digital core)
n.c.	24	not connected
FTC	25	fast track count output
TDO	26	test data output (factory test only)
FTCREF	27	FTC reference input
OCENTRAL	28	test pin for offset cancellation
S2	29	servo current output 2 for radial tracking
S1	30	servo current output 1 for radial tracking
V_{SSA4}	31	analog ground 4
V_{DDA4}	32	analog supply voltage 4 (servo signal processing)
OD	33	servo current output for focus D
OC	34	servo current output for focus C
OB	35	servo current output for focus B
OA	36	servo current output for focus A
V_{DDA3}	37	analog supply voltage 3 (RF output stage)
RFREF	38	DC reference input for RF channel common mode output voltage
RFP	39	positive RF output
RFN	40	negative RF output

SYMBOL	PIN	DESCRIPTION
V_{SSA3}	41	analog ground 3
V_{SSA2}	42	analog ground 2
V_{DDA2}	43	analog supply voltage 2 (internal RF data processing)
REXT	44	reference current input (connect via 12.1 kΩ to V_{SSA4})
CDLO	45	CD laser output
CDMI	46	input signal from CD laser monitor diode
V_{DDL}	47	laser supply voltage
DVDLO	48	DVD laser output

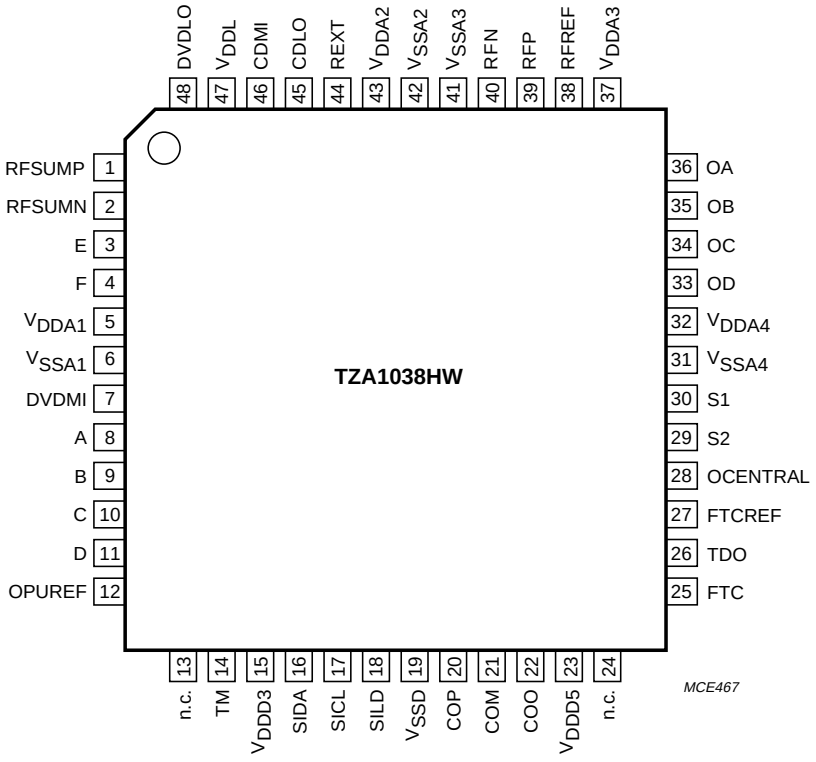


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 RF data processing

The RF data path is a fully DC-coupled, multi-stage amplifier (see Fig.3). The input signal for data can be selected from RF inputs A to D or from the summed RF inputs RFSUMP and RFSUMN. Switching between the two sets of signals is performed by an internal multiplexer. The signals are fully balanced internally to improve signal quality and reduce power supply interference.

RF outputs RFP and RFN can be DC coupled to the Analog-to-Digital Converter (ADC) of the decoder.

The RF input signals are from photodiodes and have a large DC content by nature. This DC component must be removed from the signals for good system performance. Built-in DACs, located after the input stages G_1 and RFSUM, have the ability to do this. The DAC range and resolution is scaled with the gain setting of the first amplifier stage. When the DC content is removed, the RF signal can be DC coupled to the decoder. The main advantage of DC coupling is fast recovery from signal swings due to disc defects since there is no AC coupling capacitance to slow the recovery. When using DC coupling, both AC and DC content in the data signal is known. The Philips Iguana decoders have on-chip control loops to support Automatic Gain Control (AGC) and DC cancellation.

Two separate DACs are available for cases where the left and right side DC conditions can be different.

When it is not possible to have a DC connection between the TZA1038HW and the decoder, the signals on servo outputs OA to OD can be used as they contain the same LP-filtered and DC coupled information.

Summing of the photodiode signals A to D is performed in the second amplifier stage G_2. Each individual diode channel can be switched on, off or inverted with switches SW-A to SW-D.

Switching between photodiode signals and RFSUM input is performed immediately before the third amplifier stage G_3. This stage has a variable gain with fine resolution to allow automatic gain adjustment to be controlled by the decoder.

The filter stage limits the bandwidth according to the maximum playback speed of the disc. This is to optimize the noise performance. The filter stage consists of an equalizer and a noise filter, both of which can be bypassed, also the boost factor of the equalizer can be set. The corner frequencies of the equalizer and noise filter are equal and can be programmed to a 7-bit resolution.

The RF output signals RFP and RFN can be DC coupled to a decoder with a differential input pair (as with Philips Iguana decoders). The common mode output voltage can be set externally at pin RFREF.

The signals for differential phase detection are tapped from the inputs A to D at the RF amplifier G_1 stages. DC cancellation for the A to D and RFSUM signal paths can be set independently or simultaneously.

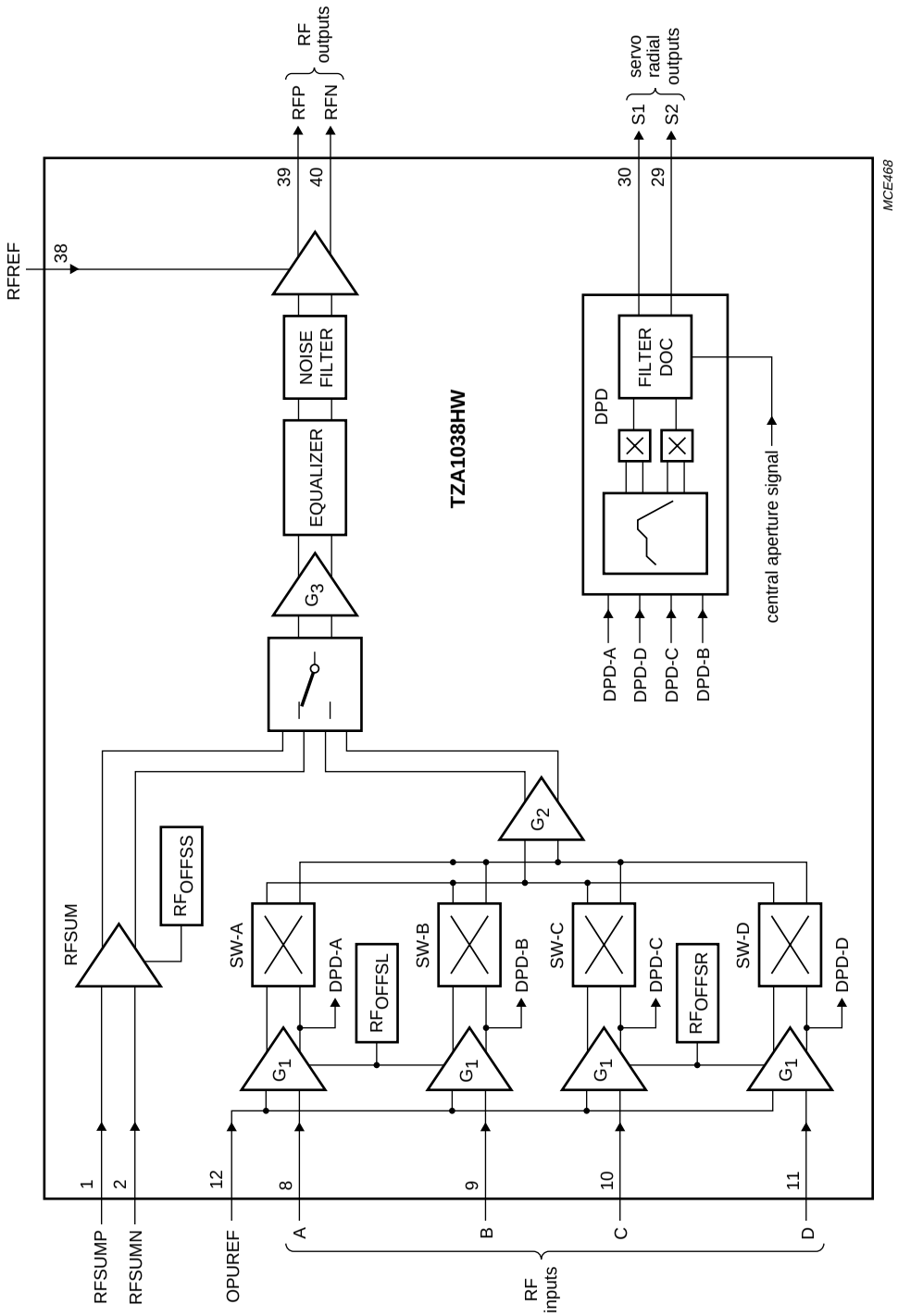


Fig.3 RF data and DPD processing.

7.2 Servo signal processing

The photodiode configurations and naming conventions are shown in Figs 4 and 5.

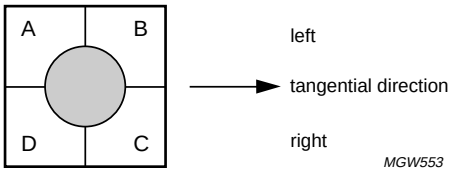
7.2.1 SERVO SIGNAL PATH SET-UP

A block diagram of the servo signal path is shown in Fig.6. In general, the servo signal path comprises:

- A voltage-to-current converter with programmable offset voltage source V_{LFOFFS} that is common to all inputs
- A 4-bit DAC for each of the six channels to compensate for offset per channel
- A variable gain stage to adapt the signal level to the specific pick-up and disc properties
- Low-pass filtering and output stage for the photodiode current signals
- Error output stage in the radial data path for fast track counting.

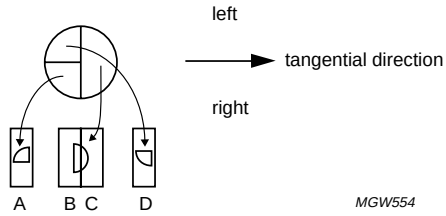
Servo output signals OA to OD, S1 and S2 are unipolar current signals which represent the low-pass filtered photodiode signals. In DPD radial tracking, the S1 and S2 signals are the equivalent of the satellite signals commonly found in traditional CD systems.

The servo output signals OA to OD, S1 and S2 are set to 3-state if bit RFonly = 1 (register 13, bit 11).



Data = A + B + C + D
Push-pull = (A + B) – (C + D)
Focus = (A + C) – (B + D)
DPD2 = phase (A + B, C + D)
DPD4 = phase (A,D) + phase (C,B)

Fig.4 Astigmatic diode configuration.



Data = A + B + C + D
Push-pull = A – D
Focus = C – B
DPD2 = phase (A, D)
DPD4 not applicable

Fig.5 Foucault diode configuration.

7.2.2 FOCUS SERVO

Focus information is reflected in the four outputs OA to OD. Gain and offset can be programmed.

For optical pick-ups where only channels B and C are used for focus, channels A and D can be switched off (bit Focus_mode = 0).

For initial alignment, a copy of the output currents can be made available on pin OCENTRAL.

7.2.3 RADIAL SERVO

Radial information can be obtained from the two output signals S1 and S2, and the gain and offset can be programmed. The TZA1038HW provides differential phase detection, push-pull and three-beam push-pull for radial tracking. The signal FTC is made available for fast track counting and is primarily the voltage error signal derived from signals S1 or S2.

The polarity of the radial loop can be reversed via the serial control bus (RAD_pol).

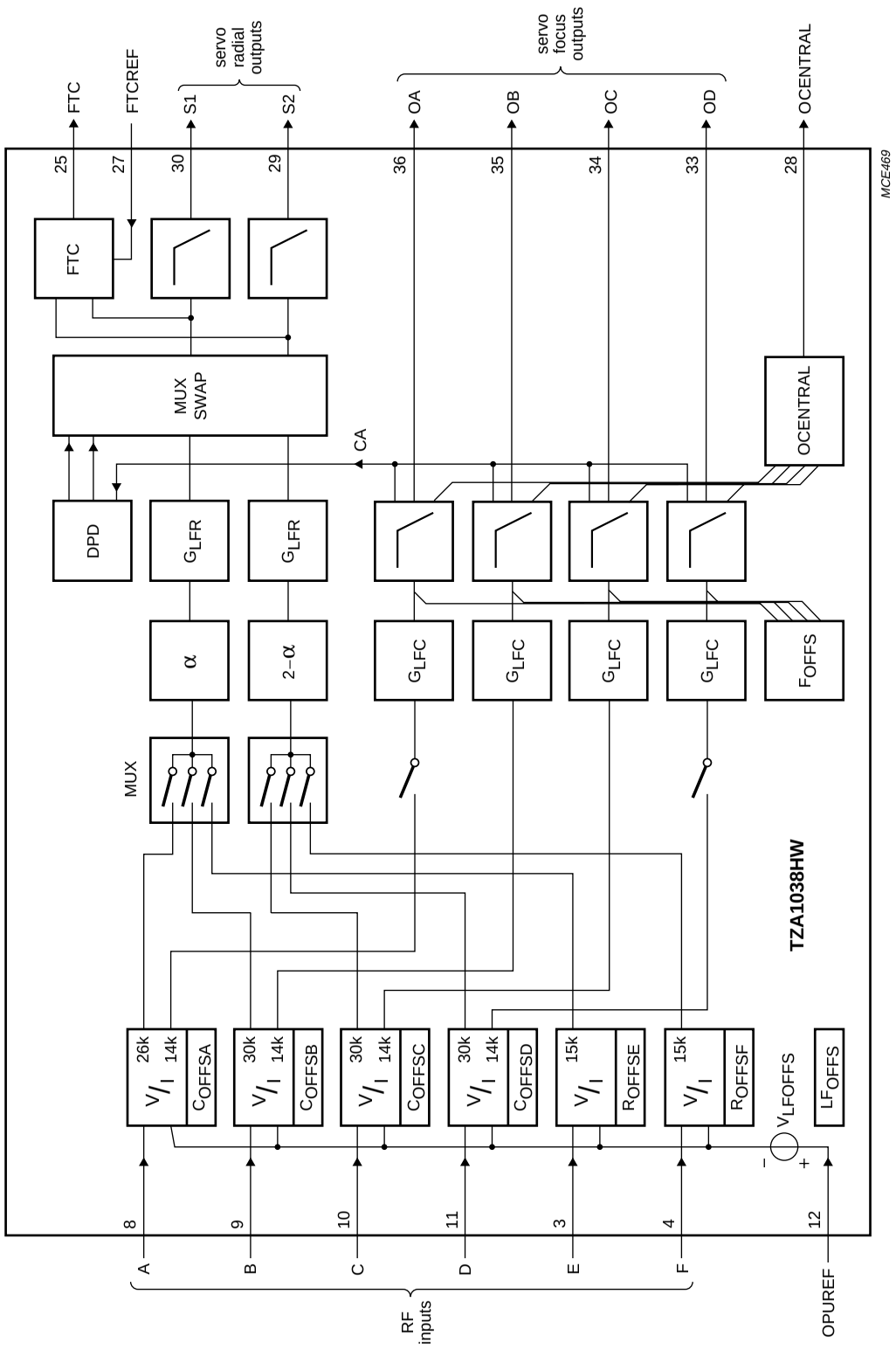


Fig.6 Servo signal path.

7.2.4 DIFFERENTIAL PHASE DETECTION

The TZA1038HW provides differential phase detection to support DVD in various ways:

- DPD2 with four channels programmed to be active gives DPD as required in the standard specification
- Two of the four channels can be excluded from the DPD for pick-ups with an alternative photodiode arrangement
- An increase in performance, dedicated for DVD+RW, can be obtained by using the DPD4 method. Then two truly separated phase detectors are active. After the phase detection of the two input pairs the result is summed.

Input signals for DPD are taken from input pins A to D after the first gain stage G_1 (see Fig.3). Pre-emphasis is applied by means of a programmable lead/lag filter. Additionally, a programmable low-pass filter is available to improve the signal quality under noisy signal conditions at lower speeds. For further signal improvements the DPD pulse stretcher can be programmed to higher values at lower speeds.

The DPD signal is low-pass filtered by two internal capacitors. The signal is then fed to pins S1 and S2, or directed via the drop-out concealment circuit to the outputs (see Section 7.5).

7.2.4.1 Drop-out concealment

A special function is built in for compatibility with drop-out detection strategies, based on level detection in the S1 and S2 signals. When using DPD in a fundamental way, there is no representation of mirror level information from the light pen.

When the drop-out concealment function is enabled (bit DOCEN = 1), a portion of the Central Aperture (CA) signal is added to S1 and S2. Also, when the CA signal drops below the DOC threshold, the DPD signal is gradually attenuated.

The DPD detection cannot work properly when the input signal becomes very small. The output of the DPD may then show a significant offset. The DOC may not conceal this offset completely because:

- DOC is gradually controlled from the CA signal
- The CA signal may not become 0 during disc-defect.

For details see Section 7.5.5.2

7.2.4.2 Push-pull and three-beam push-pull

The TZA1038HW can also provide radial information by means of push-pull signals (from the photodiode inputs) or in a three-spot optical system with Three-Beam Push-Pull (TBPP). The built-in multiplexer gives a flexible method of dealing with many detector arrangements. For push-pull, the input signals are taken from channels A to D. There is also a command that switches off channels B and C, leaving channels A and D for push-pull (bits RT_mode[2:0]).

For TBPP, the input signal is taken from channels E and F, irrespective of bit RFSUM setting.

7.2.4.3 Enhanced push-pull (dynamic offset compensation for beam landing)

This option cancels offsets due to beam landing. A factor α can be programmed to re-balance the signal gain between channels S1 and S2. In a simplified form this can be described as:

$S1 = A_{LFR} \times \alpha \times$ input left

$S2 = A_{LFR} \times (2 - \alpha) \times$ input right.

Factor α can be programmed in a range from 0.6 to 1.35, with 1.0 as the balanced condition (bits α[3:0]).

7.2.4.4 Offset compensation

A provision is made to compensate electrical offset from a light pen. The offset voltage from the light pen can be positive or negative. In general, the offset between any two channels is smaller than the absolute offsets. As negative input signals cannot be handled by the TZA1038HW internal servo channels, a two-step approach is adopted:

- A coarse DAC, common to all the input channels, adds an offset that shifts the input signals in positive direction until all inputs are ≥ 0. The DAC used (LF_{OFFS}) has a 2-bit resolution (bits LF_{OFF}[1:0]).
- A fine setting per channel is provided to cancel the remainder of the offset between the channels. This is achieved by DACs subtracting the DC component from the signals and bringing the inputs to approximately zero offset (within $\approx$ 1 mV). The DACs (registers 11 to 13) have a 4-bit resolution.

The range of both DACs can be increased by a factor of three to compensate for higher offset values by means of control parameter bit SERVOOS.

With a switched-off laser, the result of the offset cancellation can be observed at each corresponding output pin, OA to OD, S1 and S2, or via a built-in multiplexer to pin OCENTRAL (central channels only). See registers 11 to 13 for DAC and multiplexer control.

7.2.5 Automatic dual laser supply

The TZA1038HW can control the output power of two lasers; it has an Automatic Laser Power Control (ALPC) that stabilizes the laser output power and compensates the effects of temperature and ageing of the laser.

ALPC automatically detects if there is a P-type or N-type monitor diode in use in either of the laser circuits. The regulation loop formed by the ALPC, the laser, the monitor diode and the associated adjustment resistor will settle at the monitor input voltage. The monitor input voltage can be programmed to HIGH (≈ 180 mV) or LOW (≈ 150 mV), according to frequently-used pre-adjustments of the light pen. This set point can be set independently for both ALPCs. Bandwidth limitation and smooth switch-on behaviour is realized using an internal capacitor.

A protection circuit is included to prevent laser damage due to dips in laser supply voltage V_{DDL}. If a supply voltage dip occurs, the output can saturate and restrict the required laser current. Without the protection circuit, the ALPC would try to maximize the output power with destructive results for the laser when the supply voltage recovers. The protection circuit monitors the supply voltage and shuts off the laser when the voltage drops below a safe value. The ALPC recovers automatically after the dip has passed.

Only one laser can be activated at the same time. An internal break-before-make circuit ensures safe start-up for the laser when a toggle situation between the two lasers is detected. When both lasers are programmed on, neither laser will be activated.

7.2.6 Power-on reset and general power on

When the supply voltage is switched on, bit PWRON is reset by the Power-On Reset (POR) signal. This concludes in a STANDBY mode at power up. POR is intended to prevent the lasers being damaged due to random settings. All other functions may be switched when power is on. The TZA1038HW becomes active when bit PWRON = 1.

7.2.7 Compatibility with TZA1033HL/V1

7.2.7.1 Software compatibility

The TZA1038HW is highly software compatible with the TZA1033HL/V1. Provided that some conditions are met, the software of the TZA1038HW can be used as a successor with just minor modifications. This compatibility is achieved with the implementation of the TZA1038HW mode control bit (bit K2_Mode). When bit K2_Mode = 0, the TZA1038HW will act as a TZA1033HL/V1. When bit K2_Mode = 1, the TZA1038HW will act as a TZA1033HL/K2 and the new functions will be available (but require a software update).

Other conditions or restrictions are:

- Register bits of the TZA1038HW which were not defined are programmed to a logic 0. Registers 9, 10, 14 and 15 may be left undefined
- The G_4 stage high gain setting of the TZA1033HL/V1 is not available in the TZA1038HW; if this value was set to logic 0, there will be no difference
- When bit K2_Mode = 0 the RF bandwidth will be fixed to the minimum value of 10 MHz (typical); bit K2_Mode = 1 to select a higher bandwidth; the bandwidth is now lower than using a TZA1033HL/V1.

7.2.7.2 Hardware compatibility

The package is changed from LQFP64 for the TZA1033HL to LQFP48 for the TZA1038HW.

The hardware differences are:

- Input pins STB, HEADER and LAND of the TZA1033HL are not present
- Input pins CD of TZA1033HL/V1 are not used; TZA1038HW has RFSUM inputs instead; the RFSUM inputs of TZA1038HW may be connected to ground when not used.

7.2.8 INTERFACE TO THE SYSTEM CONTROLLER

Programming the registers of TZA1038HW is done via a serial bus (see Fig.7). The circuitry is formed by a serial input shift register and a number of registers that store the data. The registers can always be programmed, irrespective of STANDBY mode.

If required, the bus lines can be connected in parallel with an I^2C-bus. The protocol needs no switching of the data line during SICL = HIGH. This means that other I^2C-bus devices will not recognise any START or STOP commands. Control words addressed to TZA1038HW should go uniquely with the SILD signal. When SILD = HIGH, the TZA1038HW will not respond to any signal on SIDA or SICL.

During a transmission, the serial data is first stored in an input shift register. At the rising edge of SILD, the content of the input register is copied into the addressed register. This is also the moment the programmed information becomes effective.

The input pins have CMOS compatible threshold levels for both 3.3 and 5 V supplies.

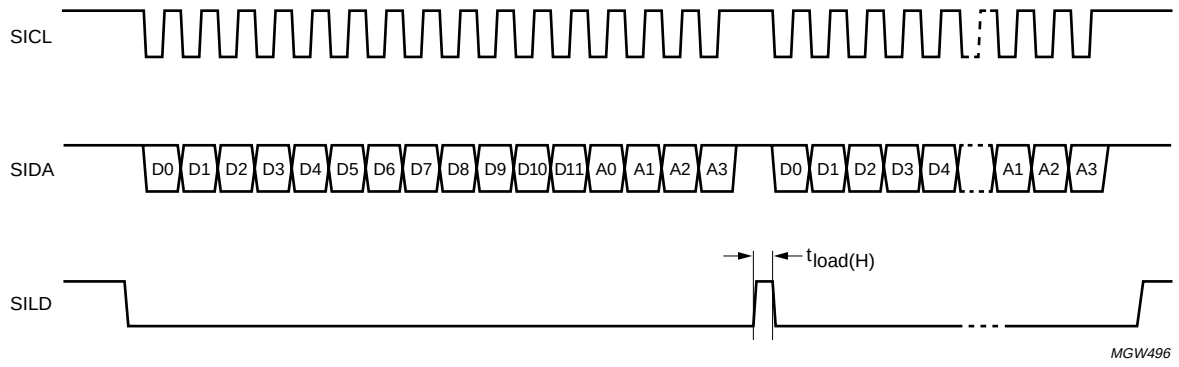


Fig.7 Two word transmission.

7.3 Control registers

The TZA1038HW is controlled by serial registers. To keep programming fast and efficient, the control bits are sent in 16-bit words. Four bits of the word are used for the address and for each address there are 12 data bits.

Table 1 Overview of control parameters

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
Data path				
G_1 (A_1)	gain of first RF amplifier stage (or linear amplification)	0, 6 and 12 dB (1×, 2× and 4×)	3	11 and 10
G_2 (A_2)	gain of second RF amplifier stage (or linear amplification)	6, 12, 18 and 24 dB (2×, 4×, 8× and 16×)	3	9 and 8
G_3 (A_3)	gain of third RF amplifier stage (or linear amplification)	0 to 13 dB in steps of 0.8 dB (1× to 4×)	3	7 to 4
GRFSUM (A_{RFSUM})	gain of RFSUM input stage (or linear amplification)	−6, 0, 6, 12 and 18 dB (0.5×, 1×, 2×, 4× and 8×)	0	7 to 5
BWRF	bandwidth limitation in RF path	$f_{0(RF)}$ = 12 to 145 MHz	14	6 to 0

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
RF_{OFFSL}	DC offset compensation in left RF input path	RFSUM = 0; full range depends on G_1 setting: G_1 = 0 dB: 0 to 450 mV in 7.1 mV steps G_1 = 6 dB: 0 to 225 mV in 3.6 mV steps G_1 = 12 dB: 0 to 120 mV in 1.9 mV steps	4	11 to 6
RF_{OFFSR}	DC offset compensation in right RF input path	RFSUM = 0; full range depends on G_1 setting: G_1 = 0 dB: 0 to 450 mV in 7.1 mV steps G_1 = 6 dB: 0 to 225 mV in 3.6 mV steps G_1 = 12 dB: 0 to 120 mV in 1.9 mV steps	4	5 to 0
RF_{OFFSS}	DC offset compensation in RFSUM path	RFSUM = 1; full range depends on GRFSUM setting: GRFSUM = −6 dB; 0 to 1700 mV GRFSUM = 0 dB; 0 to 850 mV GRFSUM = 6 dB; 0 to 425 mV GRFSUM = 12 dB; 0 to 210 mV GRFSUM = 18 dB; 0 to 105 mV	4 or 5	5 to 0
Servo radial path				
LF_{OFFS}	DC offset compensation for LF path (common for all servo inputs)	SERVOOS = 0: V_{LFOFFS} = 0, 5, 10 or 15 mV	11	11 and 10
		SERVOOS = 1: V_{LFOFFS} = 0, 15, 30 or 45 mV		
R_{LFR}	CD satellite path input transresistance	15 kΩ fixed	–	–
R_{LFPP}	DVD push-pull signal transresistance	30 kΩ fixed	–	–
R_{OFFSE}	DC offset compensation for radial servo path (input E)	SERVOOS = 0: V_{ROFFSE} = 0 to 20 mV SERVOOS = 1: V_{ROFFSE} = 0 to 60 mV	11	7 to 4
R_{OFFSF}	DC offset compensation for radial servo path (input F)	SERVOOS = 0: V_{ROFFSF} = 0 to 20 mV SERVOOS = 1: V_{ROFFSF} = 0 to 60 mV	11	3 to 0
α	dynamic radial offset compensation factor	α = 0.6 to 1.35 in 15 steps of 0.05	6	3 to 0
$I_{(FS)(DPD)}$, $I_{(FS)(DPD)(DOC)}$	full scale DPD current, fixed value based on bandgap voltage across external resistor	DOCEN = 0: fixed value = 20 μA DOCEN = 1: fixed value = 6.6 μA	1	5
$I_{REFRAD(CM)}$	internally generated common mode DC reference current in DPD mode	3.5 μA fixed	–	–
f_{start_DPD}	start frequency lead/lag filter of DPD block	f_{start_DPD} = 1, 5 or 10 MHz (TZA1033HL/V1 compatible)	7	1 and 0
		f_{start_DPD} = 1, 5, 10, 18 or 24 MHz	15	5 to 3

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
G_{LFR} (A_{LFR})	low frequency gain, radial path output stage (or linear amplification)	−15 to +9 dB in steps of 3 dB (0.18× to 2.8×)	6	11 to 8
R_{FTC}	gain of fast track count output	680 kΩ ±20% fixed for ±2 V (p-p)	–	–
Servo focus path				
R_{LFC}	LF path input transresistance	14 kΩ fixed	–	–
C_{OFFSA}	DC offset compensation for central servo path A	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	12	7 to 4
C_{OFFSB}	DC offset compensation for central servo path B	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	12	3 to 0
C_{OFFSC}	DC offset compensation for central servo path C	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	13	7 to 4
C_{OFFSD}	DC offset compensation for central servo path D	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	13	3 to 0
G_{LFC} (A_{LFC})	low frequency gain, central path output stage (or linear amplification)	−15 to +9 dB in steps of 3 dB (0.18× to 2.8×)	6	7 to 4
β	focus offset compensation	β = 0 to $^{31}/_{32}$	2	4 to 0
F_{OFFSEN}	full range offset compensation for focus	DAC enabled: I_{FOFFS} = 400 nA (fixed) DAC disabled: I_{FOFFS} = 0 nA	2	10

7.3.1 REGISTER 0: POWER CONTROL

Table 2 Register address 0H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	GRF SUM2	GRF SUM1	GRF SUM0	DVD_ MILVL	CD_MILVL	DVD_ LDON	CD_LDON	PWRON

Table 3 Description of register bits (address 0H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0000 = address 0H
11 to 8	–	not used
7 to 5	GRFSUM[2:0]	**Gain of RFSUM input stage.** 000 = −6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB
4	DVD_MILVL	**DVD monitor input level.** 0 = 150 mV; 1 = 180 mV.

BIT	SYMBOL	FUNCTION
3	CD_MILVL	**CD monitor input level.** 0 = 150 mV; 1 = 180 mV.
2	DVD_LDON	**DVD laser on.** 0 = laser off; 1 = laser on.
1	CD_LDON	**CD laser on.** 0 = laser off; 1 = laser on.
0	PWRON	**Power on.** 0 = STANDBY mode; 1 = power on.

7.3.2 Register 1: servo and RF modes

Table 4 Register address 1H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	DPD_DCC	–	–	RAD_pol

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	DOCEN	Focus_ mode	RT_mode2	RT_mode1	RT_mode0	RFSUM

Table 5 Description of register bits (address 1H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0001 = address 1H
11	DPD_DCC	**RF offset DAC for DPD signal control.** 0 = DAC controlled by register 4, bits RF_{OFFSL}[5:0]; 1 = DAC controlled by register 5, bits RF_{OFFSS}[5:0].
10 and 9	–	not used
8	RAD_pol	**Radial polarity switch.** 0 = inverse; 1 = normal (default).
7 and 6	–	not used
5	DOCEN	**Drop-out concealment enable.** 0 = disable; 1 = enable.
4	Focus_mode	**Focus mode.** 0 = two-channel focus (channels B and C only); 1 = four-channel focus.
3 to 1	RT_mode[2:0]	**Radial tracking mode.** 000 = DPD2; DPD = phase (A,D) 001 = push-pull; channels A,D only 100 = DPD2; DPD = phase (A + C, B + D) 101 = push-pull; four channels 110 = DPD4; DPD = phase (A,D) + phase (C,B) X11 = TBPP channels E and F
0	RFSUM	**RF channel selection.** 0 = diode inputs selected; 1 = RFSUM input selected.

7.3.3 REGISTER 2: FOCUS OFFSET DAC

Table 6 Register address 2H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	K2_Mode	F_{OFFSEN}	β4	β3

BIT	7	6	5	4	3	2	1	0
SYMBOL	β2	β1	β0	–	–	–	–	–

Table 7 Description of register bits (address 2H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0010 = address 2H
11	K2_Mode	**K2 mode.** 0 = disable; 1 = enable.
10	F_{OFFSEN}	**Focus offset enable.** 0 = enable; 1 = disable.
9 to 5	β[4:0]	**Focus offset compensation.** 00000 to 11111: β = 0 to β = $^{31}/_{32}$.
4 to 0	–	not used

7.3.4 REGISTER 3: RF PATH GAIN

Table 8 Register address 3H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$G_1$1	$G_1$0	$G_2$1	$G_2$0

BIT	7	6	5	4	3	2	1	0
SYMBOL	$G_3$3	$G_3$2	$G_3$1	$G_3$0	–	–	–	–

Table 9 Description of register bits (address 3H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0011 = address 3H
11 and 10	G_1[1:0]	**First RF amplifier stage gain.** 00 = 0 dB 01 = 6 dB 10 = 12 dB 11 = not used
9 and 8	G_2[1:0]	**Second RF amplifier stage gain.** 00 = 6 dB 01 = 12 dB 10 = 18 dB 11 = 24 dB
7 to 4	G_3[3:0]	**Third RF amplifier stage gain.** 0000 to 1111: 0 to 13 dB in 0.8 dB steps.
3 to 0	–	not used

7.3.5 Register 4: RF left and right, or sum offset compensation

Table 10 Register address 4H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$RF_{OFFSL}5$	$RF_{OFFSL}4$	$RF_{OFFSL}3$	$RF_{OFFSL}2$

BIT	7	6	5	4	3	2	1	0
SYMBOL	$RF_{OFFSL}1$	$RF_{OFFSL}0$	$RF_{OFFSR}5$/ $RF_{OFFSS}5$	$RF_{OFFSR}4$/ $RF_{OFFSS}4$	$RF_{OFFSR}3$/ $RF_{OFFSS}3$	$RF_{OFFSR}2$/ $RF_{OFFSS}2$	$RF_{OFFSR}1$/ $RF_{OFFSS}1$	$RF_{OFFSR}0$/ $RF_{OFFSS}0$

Table 11 Description of register bits (address 4H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0100 = address 4H
11 to 6	RF_{OFFSL}[5:0]	**Left channel RF offset compensation definition.** bit RFSUM = 0: left RF channel offset compensation value bit RFSUM = 1: not used
5 to 0	RF_{OFFSR}[5:0]	**Right channel RF offset compensation definition.** bit RFSUM = 0: right RF channel offset compensation value (symbol is RF_{OFFSR}) bit RFSUM = 1 and bit DPD_DCC = 1: not used bit RFSUM = 1 and bit DPD_DCC = 0: the decoder controls DPD and RFSUM channels automatically, in parallel and with same values (symbol is RF_{OFFSS}).

7.3.6 Register 5: RF sum offset compensation

Table 12 Register address 5H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	$RF_{OFFSS}5$	$RF_{OFFSS}4$	$RF_{OFFSS}3$	$RF_{OFFSS}2$	$RF_{OFFSS}1$	$RF_{OFFSS}0$

Table 13 Description of register bits (address 5H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0101 = address 5H
11 to 6	–	not used
5 to 0	RF_{OFFSS}[5:0]	**RF offset compensation definition.** bit RFSUM = 0: not used bit RFSUM = 1 and bit DPD_DCC = 0: not used bit RFSUM = 1 and bit DPD_DCC = 1: the decoder controls RFSUM channels; the DPD channels can be set independently from the microprocessor.

7.3.7 Register 6: servo gain and dynamic radial offset compensation factor

Table 14 Register address 6H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$G_{LFR}3$	$G_{LFR}2$	$G_{LFR}1$	$G_{LFR}0$

BIT	7	6	5	4	3	2	1	0
SYMBOL	$G_{LFC}3$	$G_{LFC}2$	$G_{LFC}1$	$G_{LFC}0$	$\alpha 3$	$\alpha 2$	$\alpha 1$	$\alpha 0$

Table 15 Description of register bits (address 6H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0110 = address 6H
11 to 8	G_{LFR}[3:0]	**Low frequency gain, radial path output stage.** 0000 to 1000: –15 to +9 dB in 3 dB steps.
7 to 4	G_{LFC}[3:0]	**Low frequency gain, central path output stage.** 0000 to 1000: –15 to +9 dB in 3 dB steps.
3 to 0	α[3:0]	**Dynamic radial offset compensation factor.** 0000 to 1111: 0.60 to 1.35 in 0.05 steps; 1000 = balanced value (default).

7.3.8 Register 7: servo path gain and bandwidth and RF path bandwidth and pre-emphasis

Definitions in register 7 are intended mainly for software compatibility with the TZA1033HL/V1. New features that require more bit-space to program are moved to registers 14 and 15. Only DPD stretch remains programmed in register 7. Some parameters are slightly modified.

Table 16 Register address 7H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	DPDLPF1	DPDLPF0	DPD_ stretch2	DPD_ stretch1

BIT	7	6	5	4	3	2	1	0
SYMBOL	DPD_ stretch0	DPD_ testmode	DVDALAS_ mode	$EQ_{RF}2$	$EQ_{RF}1$	$EQ_{RF}0$	$f_{start\_DPD}1$	$f_{start\_DPD}0$

Table 17 Description of register bits (address 7H)

BIT	SYMBOL	FUNCTION	
		K2_Mode = 0	K2_Mode = 1
15 to 12	AD[3:0]	0111 = address 7H	0111 = address 7H
11 and 10	DPDLPF[1:0]	**DPD low-pass filter.** 0X : B_{-3dB} = 50 MHz (equivalent to TZA1023) 1X : B_{-3dB} = 10 MHz	not applicable

BIT	SYMBOL	FUNCTION	
		K2_Mode = 0	K2_Mode = 1
9 to 7	DPD_stretch [2:0]	**DPD pulse stretcher (t_P).** 000 = 1.9 ns 001 = 3.8 ns (equivalent to TZA1023) 010 = 7.5 ns 011 = 15 ns 100 = 30 ns 101 = not used	**DPD pulse stretcher (t_P).** 000 = 30 ns 001 = 15 ns 010 = 7.5 ns 011 = 3.8 ns 100 = 1.9 ns 101 = 1.2 ns
6	DPD_ testmode	**For factory test purposes only.**	**For factory test purposes only.**
5	DVDALAS_ mode	**DVDALAS mode bit.** 0 = disables control of bits 11 to 6 and creates behaviour equivalent to TZA1023; 1 = enables DPD low-pass filter and time stretcher equivalent to TZA1033HL/V1.	not applicable
4 to 2	EQ_{RF}[2:0]	**RF channel low-pass filter (B_{RF}).** 001 = 10 MHz	not applicable
1 and 0	f_{start_DPD}[1:0]	**Start frequency lead/lag filter, DPD block.** 00 = 1 MHz 01 = 5 MHz 10 = 10 MHz 11 = not used	not applicable

7.3.9 Register 8: RF channel selection

Table 18 Register address 8H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	SW-D_{mute}	SW-D_{inv}	SW-C_{mute}	SW-C_{inv}	SW-B_{mute}	SW-B_{inv}	SW-A_{mute}	SW-A_{inv}

Table 19 Description of register bits (address 8H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1000 = address 8H.
11 to 8	–	not used
7	SW-D_{mute}	0 = pass D signal; 1 = mute D signal.
6	SW-D_{inv}	0 = pass D signal with no inversion; 1 = pass D signal with inversion.
5	SW-C_{mute}	0 = pass C signal; 1 = mute C signal.
4	SW-C_{inv}	0 = pass C signal with no inversion; 1 = pass C signal with inversion.
3	SW-B_{mute}	0 = pass B signal; 1 = mute B signal.

BIT	SYMBOL	FUNCTION
2	SW-B_{inv}	0 = pass B signal with no inversion; 1 = pass B signal with inversion.
1	SW-A_{mute}	0 = pass A signal; 1 = mute A signal.
0	SW-A_{inv}	0 = pass A signal with no inversion; 1 = pass A signal with inversion.

7.3.10 Register 11: radial servo offset cancellation

Table 20 Register address BH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$LF_{OFFS}1$	$LF_{OFFS}0$	SERVOOS	FTCHBW

BIT	7	6	5	4	3	2	1	0
SYMBOL	$R_{OFFSE}3$	$R_{OFFSE}2$	$R_{OFFSE}1$	$R_{OFFSE}0$	$R_{OFFSF}3$	$R_{OFFSF}2$	$R_{OFFSF}1$	$R_{OFFSF}0$

Table 21 Description of register bits (address BH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1011 = address BH
11 and 10	LF_{OFFS}[1:0]	**DC offset compensation for LF path (V_{LFOFFS}).** Common for all servo inputs: SERVOOS = 0 / SERVOOS = 1 00 = 0 mV / 00 = 0 mV 01 = 5 mV / 01 = 15 mV 10 = 10 mV / 10 = 30 mV 11 = 15 mV / 11 = 45 mV
9	SERVOOS	**Servo offset scale (DACs R_{OFFSx}, C_{OFFSx} and LF_{OFFS}).** 0 = normal range; 1 = triple range.
8	FTCHBW	**FTC bandwidth.** 0 = 600 kHz (approximately); 1 = 1.2 MHz (approximately.)
7 to 4	R_{OFFSE}[3:0]	**Programmable DC offset compensation for radial servo path (E input).** SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	R_{OFFSF}[3:0]	**Programmable DC offset compensation for radial servo path (F input).** SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.11 Register 12: central servo offset cancellation inputs A and B

Table 22 Register address CH

BIT	15	14	13	12	D11	D10	D9	D8
SYMBOL	AD3	AD2	AD1	AD0	TSTDPDRF	TSTSRV2	TSTSRV1	TSTSRV0

BIT	D7	D6	D5	D4	D3	D2	D1	D0
SYMBOL	$C_{OFFSA}3$	$C_{OFFSA}2$	$C_{OFFSA}1$	$C_{OFFSA}0$	$C_{OFFSB}3$	$C_{OFFSB}2$	$C_{OFFSB}1$	$C_{OFFSB}0$

Table 23 Description of register bits (address CH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1100 = address CH
11	TSTDPDRF	**DPD RF test bit.** With this bit the DPD filter performance is checked. 0 = normal operation; 1 = RF signal filtered by the DPD block is connected to the RF output.
10 to 8	TSTSRV[2:0]	**Test matrix for servo signals to pin OCENTRAL.** 000 = normal operation 001 = filter DAC current for test purposes 011 = CA (sum A to D) 100 = channel A 101 = channel B 110 = channel C 111 = channel D
7 to 4	C_{OFFSA}[3:0]	**Central servo input A offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	C_{OFFSB}[3:0]	**Central servo input B offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.12 Register 13: central servo offset cancellation inputs C and D

Table 24 Register address DH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	RFonly	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	$C_{OFFSC}3$	$C_{OFFSC}2$	$C_{OFFSC}1$	$C_{OFFSC}0$	$C_{OFFSC}3$	$C_{OFFSC}2$	$C_{OFFSC}1$	$C_{OFFSC}0$

Table 25 Description of register bits (address DH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1101 = address DH
11	RFonly	**Operation mode.** 0 = normal operation; 1 = RF only mode (servo outputs OA to OD, S1 and S2 are 3-state).
10 to 8	–	not used
7 to 4	C_{OFFSC}[3:0]	**Central servo input C offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	C_{OFFSD}[3:0]	**Central servo input D offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.13 Register 14: RF filter settings

Table 26 Register address EH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	RFNFEN	RFEQEN

BIT	7	6	5	4	3	2	1	0
SYMBOL	RFKEQ	BWRF6	BWRF5	BWRF4	BWRF3	BWRF2	BWRF1	BWRF0

Table 27 Description of register bits (address EH); bit K2_Mode = 1

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1110 = address EH
11 and 10	–	not used
9	RFNFEN	**Noise filter enable.** 0 = disable; 1 = enable.
8	RFEQEN	**Equalizer enable.** 0 = disable; 1 = enable.
7	RFKEQ	**Boost factor.** 0 = boost factor low; 1 = boost factor high.
6 to 0	BWRF[6:0]	**Bandwidth limitation in RF path.** 000 0000 to 111 1111: $f_{0(RF)}$ = 12 to 145 MHz.

7.3.14 Register 15: DPD filter settings

Table 28 Register address FH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	DPD_LL2	DPD_LL1	DPD_LL0	DPD_LPF2	DPD_LPF1	DPD_LPF0

Table 29 Description of register bits (address FH); bit K2_Mode = 1

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1111 = address FH
11 to 6	–	not used
5 to 3	DPD_LL[2:0]	**DPD lead/lag filter start frequency (f_{start}).** 000 = 1 MHz 001 = 5 MHz 010 = 10 MHz 011 = 18 MHz 100 = 24 MHz
2 to 0	DPD_LPF[2:0]	**DPD low-pass filter (f_{-3dB}).** 000 = 10 MHz 001 = 50 MHz 010 = 100 MHz 011 = 180 MHz 111 = 240 MHz

7.4 Internal digital control, serial bus and external digital input signal relationships

The settings of all internal switches, DACs and modes of operation can be programmed via the serial bus. There are also a few external digital signals which influence the programmed settings.

7.4.1 STANDBY MODE

To ensure a safe start-up, the TZA1038HW has an internal Power-on reset that resets on bit PWRON. During STANDBY mode, most circuits, including laser supplies, are switched off.

bit CD_LDON = 1 if CD laser is on and POWERON

bit DVD_LDON = 1 if DVD laser is on and POWERON.

7.4.2 RF ONLY MODE

The servo outputs can be disabled for easy interfacing in systems where two front-end signal processors are used. This mode will set the outputs OA to OD, S1 and S2 to 3-state. The RF data path remains active.

7.5 Signal descriptions

The variables A_1 to A_3, A_{RFSUM}, A_{LFC} and A_{LFR}, are the linear equivalents of G_1 to G_3, GRFSUM, G_{LFC} and G_{LFR}.

7.5.1 DATA PATH SIGNALS THROUGH PINS A TO D

With bit RFSUM = 0:

$$(DVD_{RFP} - DVD_{RFN}) =$$
$$A_2 \times {}^1/_4 \times [\text{SW-A}\ \{(A - OPUREF) \times A_1 - RF_{OFFSL}\}$$
$$+ \text{SW-B}\ \{(B - OPUREF) \times A_1 - RF_{OFFSL}\}$$
$$+ \text{SW-C}\ \{(C - OPUREF) \times A_1 - RF_{OFFSR}\}$$
$$+ \text{SW-D}\ \{(D - OPUREF) \times A_1 - RF_{OFFSR}\}]$$

$$RFP = RFREF + 0.5 \times A_3 \times (DVD_{RFP} - DVD_{RFN})$$

$$RFN = RFREF - 0.5 \times A_3 \times (DVD_{RFP} - DVD_{RFN})$$

Thus:

$$RF_{dif} =$$
$$A_3 \times A_2 \times A_1 \times \left(\frac{A + B + C + D}{4} - OPUREF - RF_{OFFS}\right)$$

Switches SW-A to SW-D can be programmed 1, –1 or 0 (respectively pass, invert or not pass the signal) for each channel. In this way the data can be read by any combination of diode inputs.

The first gain stage also carries the signals for DPD tracking. Therefore this stage will also be active when RFSUM input and DPD is selected. The DC offset cancellation is also active in this situation but left and right channels are controlled from a single DAC. Also in this situation, the A to D and RFSUM inputs are used simultaneously.

Control of the DC offset DACs can be chosen to be from the same register or from two independent registers (registers 4 and 5).

7.5.2 Data signal path through input pins RFSUMP and RFSUMN

With bit RFSUM = 1:

$(DVD_{RFP} - DVD_{RFN}) = A_{RFSUM} \times [RFSUMP - RFSUMN - RF_{OFFSS}]$

$RFP = RFREF + 0.5 \times A_3 \times (DVD_{RFP} - DVD_{RFN})$

$RFN = RFREF - 0.5 \times A_3 \times (DVD_{RFP} - DVD_{RFN})$

Thus:

$RF_{dif} = A_{RFSUM} \times [RFSUMP - RFSUMN - RF_{OFFSS}]$

7.5.3 HF filtering

The differential HF signal from the G_3 stage is sent to a filter section that consists of an equalizer and a noise filter, which are controlled by bits BWRF, RFKEQ, RFEQEN and RFNFEN. The equalizer has a transfer function H_1 (s) which is modelled after a target transfer function H_e (s):

$$H_e(s) = \frac{1 + k \times \frac{s^2}{\omega_{0RF}^2}}{1 + \frac{s^2}{\omega_{0RF}^2} + \alpha \times \frac{s}{\omega_{0RF}}} \times \frac{1}{1 + \tau \times \frac{s}{\omega_{0RF}}}$$

This represents a third-order equi-ripple phase filter with a good delay response. The boost factor k is programmable via the serial bus control bit RFKEQ. The corner frequency $\omega_{0RF} = 2\pi f_{0RF}$ is programmable via control parameter bit BWRF. The equalizer is switched on with control bit RFEQEN.

The noise filter has a transfer function H_2 (s) which is modelled after a third-order Butterworth low-pass filter with target transfer function H_n (s):

$$H_n(s) = \frac{1}{1 + \frac{s^2}{\omega_{0RF}^2} + \frac{s}{\omega_{0RF}}} \times \frac{1}{1 + \frac{s}{\omega_{0RF}}}$$

The corner frequency ω_{0RF} is equal to that of the equalizer filter. The noise filter is switched on with bit RFNFEN.

7.5.4 Focus signals

Focus servo signals:

$$OA = \frac{1}{R_{LFC}} \times A_{LFC} \times (A - OPUREF + LF_{OFFS} - C_{OFFSA}) + \beta \times F_{OFFS}$$

$$OB = \frac{1}{R_{LFC}} \times A_{LFC} \times (B - OPUREF + LF_{OFFS} - C_{OFFSB}) + (1 - \beta) \times F_{OFFS}$$

$$OC = \frac{1}{R_{LFC}} \times A_{LFC} \times (C - OPUREF + LF_{OFFS} - C_{OFFSC}) + \beta \times F_{OFFS}$$

$$OD = \frac{1}{R_{LFC}} \times A_{LFC} \times (D - OPUREF + LF_{OFFS} - C_{OFFSD}) + (1 - \beta) \times F_{OFFS}$$

The parameter β can be programmed via the serial bus.

The focus offset DAC can be switched on with the control bit F_{OFFSEN}.

7.5.5 Radial signals

7.5.5.1 DPD signals (DVD-ROM mode) with no drop-out concealment

DPD tracking can be activated with bits RT_mode[2:0] of register 1. Input signals are taken from the diode inputs A to D, through the input stage G_1 and the DC offset cancellation DAC. When bit RFSUM = 0, the input stage is also used for the RF signal. When bit RFSUM = 1, the setting for G_1 and DC offset control can be independent of the setting for the data signal which goes through RFSUM.

$$S1_{DPD} = I_{(FS)(DPD)} \times \frac{\Delta t}{T_P} + I_{REFRAD}$$

$$S2_{DPD} = -I_{(FS)(DPD)} \times \frac{\Delta t}{T_P} + I_{REFRAD}$$

$\frac{\Delta t}{T_P}$ is the time difference between the two input signals, relative to the period time T_P of the input signal. $I_{(FS)(DPD)}$ is the full scale range.

The bandwidth of the DPD signal is limited by the 100 kHz phase detector integration filters and the bandwidth of the output stages (100 kHz for S1 and S2).

The input signals used for DPD depend on the programmed radial tracking mode (bits RT_mode[2:0]):

DPD_{mode} = DPD2: $\frac{\Delta t}{T_P}$ (A,D) or DPD2: $\frac{\Delta t}{T_P}$ (A + C, B + D)

DPD_{mode} = DPD4: $0.5[\frac{\Delta t}{T_P}$ (A,D) + $\frac{\Delta t}{T_P}$ (C,B)]

Range of $\frac{\Delta t}{T_P}$ is from –0.5 to + 0.5.

$\frac{\Delta t}{T_P}$ > 0 if A,C phase leads with respect to D,B phase.

$FTC = (S1 - S2) \times (R_{FTC} + FTCREF)$

For S1 and S2 bit RAD_pol is assumed to be set to logic 1. Otherwise the signals appearing at S1 and S2 will be swapped.

7.5.5.2 DPD signals (DVD-ROM mode) with drop-out concealment

With bit DOCEN = 1, drop-out concealment is activated and the S1 and S2 outputs change:

- The common mode level (I_{REFRAD}) is now determined by the CA signal
- The scaling changes.

At low signal levels (SUM < $DOC_{threshold}$), the contribution of $\frac{\Delta t}{T_P}$ is reduced smoothly.

$S1_{DPD} = C \times I_{(FS)(DPD)(DOC)} \times \frac{\Delta t}{T_P} + 0.25 \times CA.$

$S2_{DPD} = -C \times I_{(FS)(DPD)(DOC)} \times \frac{\Delta t}{T_P} + 0.25 \times CA.$

Where:

- $I_{(FS)(DPD)(DOC)}$ is the full scale range
- C = concealment multiplier, C = 0 to 1 when CA is 0 to $DOC_{threshold}$
- CA = OA + OB + OC + OD
- $DOC_{threshold}$ is typically 3 μA.

For S1 and S2 bit RAD_pol is assumed to be set to logic 1. Otherwise the signals appearing at S1 and S2 will be swapped.

The DPD detection can not work properly when the input signal becomes very small. The output of the DPD may then show a significant offset. The DOC may not conceal this offset completely because:

- DOC is gradually controlled from the CA signal
- The CA signal may not become 0 during disc-defect.

7.5.5.3 Three-beam push-pull (CD mode)

When the three-beam system is used, the radial signals S1 and S2 can be composed from inputs E and F.

$$S1_{PP} = A_{LFR} \times \left\{ \frac{E - OPUREF + LF_{OFFS} + R_{OFFSE}}{R_{LFR}} \right\}$$

$$S2_{PP} = A_{LFR} \times \left\{ \frac{F - OPUREF + LF_{OFFS} - R_{OFFSF}}{R_{LFR}} \right\}$$

$FTC = (S1 - S2) \times R_{FTC}$ + FTCREF (bandwidth limited to 600 kHz).

For S1 and S2 bit RAD_pol is assumed to be set to logic 1. Otherwise the signals appearing at S1 and S2 will be swapped.

7.5.5.4 Enhanced push-pull

Top hold push-pull method is supported but only in conjunction with a compatible decoder. The peak hold function is executed in the decoder, by measuring the mirror levels of the gap-zones in each header. The TZA1038HW will compensate for offset errors in two ways:

- The DC offset from the pick-up can be compensated by means of a DAC (C_{OFFSx}) in each channel
- The dynamic offsets can be compensated by means of the multiplier ratio α.

The correction values must be calculated in the decoder and programmed via the serial bus. The method is called the enhanced push-pull method.

For S1 and S2 bit RAD_pol is assumed to be set to logic 1. Otherwise the signals appearing at S1 and S2 will be swapped.

$$S1_{PP} = A_{LFR} \times \alpha \times \left\{ \frac{A + B - 2 \times OPUREF + 2 \times LF_{OFFS} - (C_{OFFSA} - C_{OFFSB})}{R_{LFPP}} \right\}$$

$$S2_{PP} = A_{LFR} \times (2 - \alpha) \times \left\{ \frac{C + D - 2 \times OPUREF + 2 \times LF_{OFFS} - (C_{OFFSC} - C_{OFFSD})}{R_{LFPP}} \right\}$$

or:

$$S1_{PP} = A_{LFR} \times \alpha \times \left\{ \frac{A - OPUREF + LF_{OFFS} - C_{OFFSA}}{R_{LFPP}} \right\}$$

$$S2_{PP} = A_{LFR} \times (2 - \alpha) \times \left\{ \frac{D - OPUREF + LF_{OFFS} - C_{OFFSD}}{R_{LFPP}} \right\}$$

The signals from the B and C channels can be switched off, depending on the photodiode configuration (bit RT_mode[2:0]).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOLS	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	5.5	V
T_{amb}	ambient temperature		–40	+85	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); note 1	–	2000	V
		Machine Model (MM); note 1	–	200	V

Note

1. ESD behaviour is tested in accordance with JEDEC II standard:
   HBM is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
   MM is equivalent to discharging a 200 pF capacitor through a 0.75 μH series inductor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	27	K/W

10 CHARACTERISTICS

V_{DDA} = 5 V; V_{DDD3} = 3.3 V; V_{DDD5} = 5 V; V_{RFREF} = 1.2 V; T_{amb} = 25 °C; RF inputs A to D are referred to pin OPUREF; $f_{0(RF)}$ = 50 MHz; R_{ext} = 12.1 kΩ (pin REXT); RF output max. load on pins RFP and RFN is $Z_{O(max)}$: 5 pF parallel with 10 kΩ to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	ambient temperature		–40	–	+85	°C
Supplies						
V_{DDA1}, V_{DDA2}, V_{DDA3}, V_{DDA4}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD3}	3 V digital supply voltage		2.7	3.3	5.5	V
V_{DDD5}	5 V digital supply voltage		4.5	5.0	5.5	V
$V_{I(logic)}$	logic input compatibility	note 1	2.7	3.3	5.5	V
V_{POR}	Power-on reset voltage		3.3	3.5	3.7	V
I_{DD}	supply current	without laser supply	–	98	120	mA
		STANDBY mode	–	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF data path, input: pins A to D and OPUREF						
$V_{i(OPUREF)}$	input voltage on pin OPUREF	note 2	1.5	$0.5V_{DDA}$	$V_{DDA} - 2$	V
$V_{i(RF)(FS)}$	input voltage on pins A to D for full-scale at output	referred to V_{OPUREF}				
		G_1 = 0 dB	–	–	600	mV
		G_1 = 6 dB	–	–	300	mV
		G_1 = 12 dB	–	–	150	mV
$\lvert V_{I(DC)} \rvert$	DC component of input voltage		1.8	$0.5V_{DDA}$	$V_{DDA} - 1.4$	V
$V_{RFOFFSL}$, $V_{RFOFFSR}$	DC offset compensation voltage	G_1 = 0 dB	350	450	550	mV
		G_1 = 6 dB	175	225	275	mV
		G_1 = 12 dB	90	120	160	mV
$\Delta V_{RFOFFSL}$, $\Delta V_{RFOFFSR}$	DC offset compensation voltage resolution	G_1 = 0 dB	–	7.1	–	mV
		G_1 = 6 dB	–	3.6	–	mV
		G_1 = 12 dB	–	1.9	–	mV
$I_{I(bias)}$	input bias current on pins A to D		–	–	5	μA
Z_i	input impedance of pins A to D		100	–	–	kΩ
$A_{RF(min)}$	minimum gain	G_1 = 0 dB, G_2 = 6 dB, G_3 = 0 dB; note 3	4	6	8	dB
$A_{RF(max)}$	maximum gain	G_1 = 12 dB, G_2 = 24 dB, G_3 = 13 dB; note 3	48	49	52	dB
TC_{gain}	gain temperature coefficient		–	–0.025	–	dB/°C
ΔG_1	first RF amplifier stage gain step size		5	6	7	dB
ΔG_2	second RF amplifier stage gain step size		5	6	7	dB
RF data path, input: pins RFSUMP and RFSUMN						
$V_{I(DC)}$	DC input voltage	with respect to V_{SS}	1.3	–	$V_{DDA} - 1.0$	V
$V_{I(SUM)(dif)}$	differential input voltage	G_{RFSUM} = –6 dB	–	–	1800	mV
		G_{RFSUM} = 0 dB	–	–	1400	mV
		G_{RFSUM} = 6 dB	–	–	700	mV
		G_{RFSUM} = 12 dB	–	–	350	mV
		G_{RFSUM} = 18 dB	–	–	175	mV
$I_{I(bias)}$	input bias current		–	5	–	μA
Z_I	input impedance	note 4	50	–	600	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{RFOFFSS}$	DC offset compensation voltage	G_{RFSUM} = –6 dB	–	1700	–	mV
		G_{RFSUM} = 0 dB	–	850	–	mV
		G_{RFSUM} = 6 dB	–	425	–	mV
		G_{RFSUM} = 12 dB	–	210	–	mV
		G_{RFSUM} = 18 dB	–	105	–	mV
$\Delta V_{RFOFFSS}$	DC offset compensation voltage resolution	G_{RFSUM} = –6 dB	–	27	–	mV
		G_{RFSUM} = 0 dB	–	13.5	–	mV
		G_{RFSUM} = 6 dB	–	6.7	–	mV
		G_{RFSUM} = 12 dB	–	3.4	–	mV
		G_{RFSUM} = 18 dB	–	1.7	–	mV
$A_{RFSUM(min)}$	minimum gain	notes 3 and 5	–8	–6	–4	dB
$A_{RFSUM(max)}$	maximum gain	notes 3 and 5	29	31	33	dB
TC_{gain}	gain temperature coefficient		–	–0.02	–	dB/°C
ΔG_{RFSUM}	RFSUM amplifier stage gain step size		5	6	7.5	dB
RF data path, filter and output						
$V_{n(o)(dif)(rms)}$	differential RF output noise voltage (RMS value)	diode input: BWRF = 127; f = 0 to 500 MHz; RFNFEN = 1; note 6				
		A = 12 + 24 + 6 dB; RFEQEN = 0	–	7	-	mV
		A = 12 + 6 + 6 dB; RFEQEN = 0	–	6	–	mV
		A = 12 + 6 + 6 dB; RFEQEN = 1; RFKEQ = 0	–	9	–	mV
		A = 12 + 6 + 6 dB; RFEQEN = 1; RFKEQ = 1	–	11	–	mV
		SUM input: BWRF = 127; f = 0 to 500 MHz; RFNFEN = 1; note 6				
		A = 12 + 6 + 6 dB; RFEQEN = 0	–	12	–	mV
$V_{OO(ref)}$	DC output offset voltage with respect to V_{RFREF}	$V_{I(RF)}$ = 0 V; DVD_{OFFS} = 0; note 7				
		V_{RFREF} = 1.2 V	–	–	60	mV
		V_{RFREF} = 0.8 to 2.1 V	–	–	100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(dif)(p-p)}$	differential output voltage on pins RFP and RFN (peak-to-peak value)		–	–	1.4	V
$V_{O(RF)(DC)}$	DC output voltage on pins RFP and RFN		0.35	–	V_{DDA} – 1.9	V
$V_{i(RFREF)(CM)}$	input reference voltage for common mode output on pin RFREF		0.8	1.2	2.1	V
R_o	output impedance on pins RFP and RFN		–	100	–	Ω
ΔG_3	third RF amplifier stage gain step size	note 8	–	0.85	1.3	dB
$\|\|h_1\| - \|h_e\|\|$	equalizer amplitude error	flatness between f_0 and 100 kHz	–	–	1.5	dB
$\|\|h_1\| - \|h_n\|\|$	noise filter amplitude error	flatness between f_0 and 100 kHz	–	–	1.5	dB
$B_{RF(-3dB)}$	−3 dB bandwidth of RFP and RFN signal path	RFEQEN = 0; RFNFEN = 0	200	300	–	MHz
$f_{0(RF)}$	noise filter and equalizer corner frequency	BWRF = 0	8	12.0	14.5	MHz
		BWRF = 127	100	145	182	MHz
$\Delta f_{0(RF)}$	noise filter and equalizer corner frequency step size	ΔBWRF = 1; note 9	0.73	1.06	1.32	MHz
$t_{d(RF)}$	flatness delay in RF data path	equalizer off; f = 0 to 150 MHz	–	–	0.1	ns
		equalizer on; f = 0 to 100 MHz; BWRF = 127	–	–	0.5	ns
		equalizer and noise filter on; f = 0 to 0.7$f_{0(RF)}$				
		BWRF = 0	–	–	3.5	ns
		BWRF = 127	–	–	0.6	ns
$t_{st(G3)}$	amplifier G_3 gain change settling time	note 10	–	–	0.5	µs
α	equalizer parameter	see Section 7.5.3	1.125	1.25	1.375	
τ	equalizer parameter	see Section 7.5.3	1.18	1.31	1.44	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
k	equalizer parameter	see Section 7.5.3				
		RFKEQ = 0	3.2	4.0	4.8	
		RFKEQ = 1	4.8	6.0	7.2	
LF servo path						
$V_{I(LF)}$	input voltage range	path to focus servo outputs referred to V_{OPUREF}	700	–	–	mV
		path to radial servo outputs referred to V_{OPUREF}	500	–	–	mv
$V_{O(LF)}$	servo output voltage		–0.2	–	V_{DD} – 2.5	V
$V_{LFOFFS(CM)}$	common mode offset compensation voltage	SERVOOS = 0	–	15	–	mV
		SERVOOS = 1	–	45	–	mV
ΔV_{LFOFFS}	DC offset voltage resolution	SERVOOS = 0	4.25	5	5.75	mV
		SERVOOS = 1	13	15	17	mV
V_{ROFFS}, V_{COFFS}	offset voltage compensation	SERVOOS = 0	–	20	–	mV
		SERVOOS = 1	–	60	–	mV
ΔV_{ROFFS}, ΔV_{COFFS}	DC offset voltage resolution	SERVOOS = 0	1.0	1.3	1.6	mV
		SERVOOS = 1	3.0	4	4.8	mV
$V_{I(FTCREF)}$	FTC reference input reference voltage		1.25	–	2.75	V
$V_{O(FTC)(p-p)}$	FTC output voltage (peak-to-peak value)		2.0	–	–	V
$I_{O(LF)}$	output current	focus servo outputs	0	–	12	µA
		radial servo outputs	0	–	12	µA
I_{FOFFS}	focus compensation current	from F_{OFFS} DAC	310	390	480	nA
ΔI_{FOFFS}	compensation current resolution		–	12	–	nA
$I_{(FS)(DPD)}$	DPD full scale current	f = 3 MHz; V_i = 100 mV (p-p)				
		DOCEN = 0	17	20	23	µA
		DOCEN = 1	4.5	6.6	8	µA
$I_{th(DOC)}$	DOCEN threshold current	SUM value	2.5	3	3.5	µA
$I_{REFRAD(CM)}$	common mode DC current in DPD mode	DOCEN = 0	–	3.5	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{LFC}	LF path input transresistance	G_{LFC} = 0 dB	10.5	14	16.5	kΩ
R_{LFR}	CD satellite path input transresistance	G_{LFR} = 0 dB; α = 1	11	15	18	kΩ
R_{LFPP}	DVD push-pull transresistance	G_{LFR} = 0 dB; α = 1	23	30	36	kΩ
R_{FTC}	fast track count transimpedance	note 11	510	650	800	kΩ
G_{LFC}	gain range central channels		–15.5	–	+8.5	dB
ΔG_{LFC}	gain resolution		–	3	–	dB
G_{LFR}	gain range radial channels		–15.5	–	+8.5	dB
ΔG_{LFR}	gain resolution		–	3	–	dB
$B_{LF(-3dB)}$	–3 dB bandwidth of LF path		60	75	100	kHz
B_{FTC}	FTC bandwidth	FTCHBW = 0	–	600	–	kHz
		FTCHBW = 1; note 12	–	1200	–	kHz
LRM	dynamic radial left right matching	α = 1	–7	–	+7	%
CPM	channel pair matching	G_{LF} = 0 dB; note 13				
		$V_{I(LF)}$ = 96 mV; pairs OA, OD or OC, OB	–2	–	+2	%FS
		$V_{I(LF)}$ = 48 mV; pair S1 and S2	–7	–	+7	%FS
α	dynamic radial offset compensation factor		0.6	–	1.35	
Δα	dynamic radial offset compensation factor resolution		–	0.05	–	
ALPC Automatic Laser Power Control						
$V_{i(mon)}$	input voltage from laser monitor diode	P-type monitor diode				
		LOW level voltage	V_{DDA4} – 0.140	V_{DDA4} – 0.155	V_{DDA4} – 0.170	V
		HIGH level voltage	V_{DDA4} – 0.215	V_{DDA4} – 0.190	V_{DDA4} – 0.180	V
		N-type monitor diode				
		LOW level voltage	0.145	0.155	0.17	V
		HIGH level voltage	0.175	0.185	0.2	V
$V_{O(laser)}$	laser output voltage		–	–	V_{DDL} – 0.5	V
V_{prot}	low supply voltage protection level		3.6	3.8	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{prot}	low supply voltage protection hysteresis		–	200	–	mV
$I_{I(mon)}$	laser monitor diode input current		–	–	200	nA
$I_{o(laser)(max)}$	maximum current output to laser		–120	–	–	mA
$t_{on(laser)}$	laser switch on time		–	3	–	ms
FTC comparator						
$V_{I(CM)}$	common mode input voltage		0	–	2.5	V
V_{OL}	LOW-level output voltage		0	–	0.5	V
V_{OH}	HIGH-level output voltage		V_{DDD3} – 0.5	–	V_{DDD3}	V
V_{IO}	input offset voltage		–	–	10	mV
I_{LI}	input leakage current		–	–	100	nA
A_V	voltage gain		–	200	–	V/mV
t_r, t_f	rise and fall time	C_L = 15 pF	–	250	–	ns
t_{res}	response time	$V_{I(dif)}$ = 200 mV (p-p)	–	200	–	ns
Serial bus interface (see Fig.8)						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD3}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD3}$	V
I_{IH}	HIGH-level input current on pin TM	input incorporates internal pull-down resistor	–	–	100	μA
I_I	input current	pins SIDA, SICL and SILD	–	–	100	nA
$t_{su(strt)}$	start set-up time		0	–	–	ns
$t_{su(D)}$	data set-up time		5	–	–	ns
$t_{h(D)}$	data hold time		20	–	–	ns
$t_{clk(H)}$	clock HIGH time		10	–	–	ns
$t_{clk(L)}$	clock LOW time		10	–	–	ns
T_{clk}	clock period		30	–	–	ns
$t_{su(load)}$	load pulse set-up time		30	–	–	ns
$t_{load(H)}$	load pulse HIGH time		10	–	–	ns

Notes

1. Level follows the applied supply voltage at pin V_{DDD3}.

2. This range for the servo path is designed to be larger than for the data path so that the servo path can handle out-of-focus situations.
3. $A = 10^{\frac{(G1 + G2 + G3)}{20}}$ [dB] or $A = 10^{\frac{(Gsum + G3)}{20}}$ [dB] (see Section 7.5).
4. Input impedance depends on gain setting. Highest gain has lowest input impedance.
5. The gain of the RF sum channel, when programmed to −6 dB, will be increased when the supply voltage is below 4.8 V and at an ambient temperature of −40 °C.
6. Noise figures depend on gain and filter settings, examples given here.
7. $V_{OO(ref)} = \frac{V_{RFP} + V_{RFN}}{2} - V_{RFREF}$
8. Integral range for G_3 from minimum to maximum gain is 13 dB (typical).
9. At the transition BWRF = 63 to 64 the Δf may be between −0.2 and +1.7 MHz
10. Faster for small steps.
11. Overall gain from input to output is determined by R_{FTC}/R_{LFR} or R_{FTC}/R_{LFPP}, depending on radial tracking mode, three-beam push-pull (CD) or DVD push-pull. Gain FTC scales with G_{FRR}. When DPD tracking is selected the FTC gain is fixed.
12. High FTC bandwidth is achieved when I_{S1} and I_{S2} > 1.5 μA.
13. Channel pair matching is defined in % of full scale (FS) output at half of the full scale level.

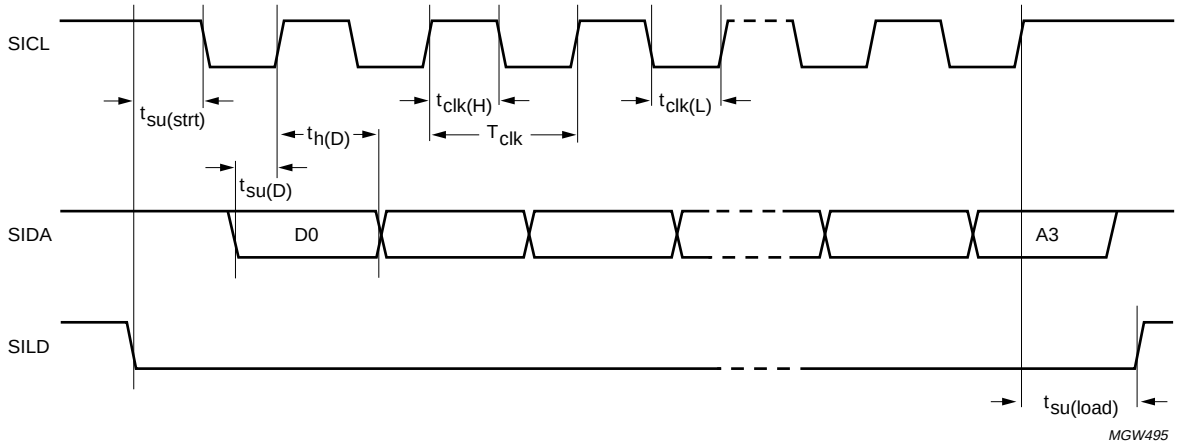


Fig.8 Single word transmission.

11 APPLICATION INFORMATION

11.1 Signal relationships

Simplified relationships between signals are described in this section. In the simplification, all built-in options for DVD-ROM are omitted. The variables A_1 to A_3, A_{LFC} and A_{LFR}, are the linear equivalents of bits G_1 to G_3, G_{LFC} and G_{LFR}.

11.1.1 DATA PATH

Pins RFP and RFN carry the RF data signals in opposite phases with respect to each other. This allows an ADC with a balanced or differential input to be used in the decoder. Depending on the DC input ranges of the ADC, in many cases the connection between TZA1038HW and the decoder can be a DC pin to pin connection. The common mode DC level of pins RFP and RFN can be chosen independently by means of input pin RFREF.

If bit RFSUM = 0

- $V_{RFP} = V_{RFREF} + 0.5 \times A_3 \times A_2 \times A_1 \times (V_I - V_{RFOFFS})$
- $V_{RFN} = V_{RFREF} - 0.5 \times A_3 \times A_2 \times A_1 \times (V_I - V_{RFOFFS})$
- $V_{RFDIF} = A_3 \times A_2 \times A_1 \times (V_I - V_{RFOFFS})$.

If bit RFSUM = 1

- $V_{RFP} = V_{RFREF} + 0.5 \times A_{RFSUM} \times A_3 \times (V_{RFSUMP} - V_{RFSUMN} - V_{RFOFFSS})$
- $V_{RFN} = V_{RFREF} - 0.5 \times A_{RFSUM} \times A_3 \times (V_{RFSUMP} - V_{RFSUMN} - V_{RFOFFSS})$
- $V_{RFDIF} = A_{RFSUM} \times A_3 (V_{RFSUMP} - V_{RFSUMN} - V_{RFOFFSS})$.

Where:

- A_1, A_2, A_3 and A_{RFSUM} are programmed gain values
- V_I = average input voltage at pins A to D, with respect to the voltage at pin OPUREF
- V_{RFOFFS} is the programmed RF_{OFFS} DAC voltage (register 4 and register 5)
- V_{RFREF} is the input voltage at pin RFREF.

Correct settings for V_{RFREF} and V_{RFOFFS} are required to keep both V_{RFP} and V_{RFN} at the DC voltage levels specified for the TZA1038HW and the decoder.

11.1.2 SERVO PATH

The current through output pins OA to OD represents the low-pass filtered input voltage of each individual pick-up segment. The gain from input to output can be programmed to adapt to different disc types or pick-ups (offset cancellation is omitted for simplicity):

$$I_{Ox} = \frac{V_{Ix} \times A_{LFC}}{14\ k\Omega}$$

$$I_{S1} = \frac{(V_{I(A)} + V_{I(B)}) \times A_{LFR}}{30\ k\Omega} \text{ (in DVD push-pull mode)}$$

$$I_{S2} = \frac{(V_{I(C)} + V_{I(D)}) \times A_{LFR}}{30\ k\Omega} \text{ (in DVD push-pull mode)}$$

or:

$$I_{S1} = \frac{V_{I(E)} \times A_{LFR}}{15\ k\Omega} \text{ (in CD three-beam push-pull mode)}$$

$$I_{S2} = \frac{V_{I(F)} \times A_{LFR}}{15\ k\Omega} \text{ (in CD three-beam push-pull mode)}$$

or:

$$I_{S1} = I_{DC} + I_{FS} \times \text{phase difference} \text{ (in DPD mode)}$$

$$I_{S2} = I_{DC} - I_{FS} \times \text{phase difference} \text{ (in DPD mode)}$$

Where:

- A_{LFC} and A_{LFR} are the programmable gains in central and radial paths
- Gain should be programmed such that maximum signal levels fit into the range of the servo processor ADC
- $V_{I(A)}$; $V_{I(B)}$; $V_{I(C)}$ and $V_{I(D)}$ are defined as input voltages at pins A to D with respect to pin OPUREF
- I_{DC} is a DC current that keeps I_{S1} and I_{S2} unipolar
- I_{FS} is the sensitivity to relative phase difference.

Phase difference = $\frac{\Delta t}{T_p} = \frac{\Delta\phi[\text{degrees}]}{360}$;

$-180° < \phi < +180°$.

11.2 Programming examples

Table 30 Sample of register values and mode settings.

REGISTER	REGISTER VALUE (HEX)			MODE SETTINGS
	DVD; LOW GAIN	DVD; HIGH GAIN(1)	CD; HIGH GAIN(1)	
0	005	045	043	switch on the laser power; V_{mon} = 150 mV; set GRFSUM
1	01D	01D	007	select diode or SUM inputs and corresponding tracking method
2	800	800	800	set K2 mode
3	800	–	800	set low RF gain = 18 dB + G_3
	–	800	–	set G_1 for DPD (G_3 = 0 dB in this example)
4	820	410	410	approximation for DVD_{OFFS} DAC
5	000	000	000	optional second RF offset setting
6	338	778	778	G_{LFC} = G_{LFR} = −6 dB (low gain) or +6 dB (high gain); α = 1
7	200	200	000	set bits DPD_stretch to 1.9 ns
8	000	000	000	enable inputs A to D for RF
9	000	000	000	not used
10	000	000	000	not used
11	000	000	000	set for electrical offset compensation from pick-up (see Section 11.4)
12	000	000	000	
13	000	000	000	
14	335	335	335	set bits BWRF to 80 MHz; RFEQEN = 1; RFNFEN = 1
15	022	022	000	set bits DPD_LL to 24 MHz; set bits DPD_LPF to 100 MHz

Note

1. Use RFSUM input.

11.3 Energy saving

Bit PWRON can be used to bring the TZA1038HW into STANDBY mode reducing the supply current to approximately 0.5 mA.

11.4 Initial DC and gain setting strategy

11.4.1 Electrical offset from pick-up

It is useful to compensate for electrical offset, especially with pick-ups that give a low output signal. It is possible to compensate for each individual servo channel. Due to internal circuitry, the TZA1038HW servo channels can handle only signals positive with respect to the reference input OPUREF. Therefore the potentially negative offset from the pick-up must first be cancelled. The LF_{OFFS} DAC can be programmed to do this, and will apply this to all six channels at the same time. The LF_{OFFS} DAC can be set to 0, 5, 10 or 15 mV.

As a second step, the offset between each channel can be compensated by connecting the DACs to each individual DAC (C_{OFFSA} to C_{OFFSD}, R_{OFFSE} and R_{OFFSF}). These DACs can be programmed between 0 and 20 mV with approximately 1.25 mV resolution. Where the LF_{OFFS} DAC increases the outputs signal level, the individual DACs decrease the output signal. In this way the output signal can be set very close to zero. The range of DACs, LF_{OFFS}, C_{OFFS} and R_{OFFS} can be tripled with control bit SERVOOS.

The output current of servo channel A is calculated by:

$$I_{OA} = \frac{[(V_A - V_{OPUREF}) + V_{FLOFFS} - V_{COFFSA}] \times A_{LFC}}{14\ k\Omega}$$

In case the laser is switched off, the term ($V_A - V_{OPUREF}$) represents the electrical offset from the pick-up.

The procedure to cancel the offset is:

1. Activate the pick-up and switch off the laser.
2. Set LF_{OFFS} to its maximum value.
3. Measure the output currents off all relevant servo outputs.
4. If all outputs represent a signal >5 mV equivalent input voltage, decrease V_{LFOFFS} then repeat step 3; if all outputs represent a signal <5 mV equivalent input voltage, go to step 5.
5. Measure each output and increase C_{OFFS} until the output current is close enough to zero.

This procedure needs only to be done once, or after a longer time when temperature may have changed the pick-up offset.

The test pin OCENTRAL can be useful to follow this procedure. This pin can be programmed to output a copy of the signal OA to OD (see register 12).

11.4.2 Gain setting servo

The servo gain has to be chosen dependant on the reflectivity of the disc. So this needs to be done each time when a new disc is inserted in the mechanism. A trial and error procedure should find the optimal setting. Gain can be set in 3 dB steps.

11.4.3 DC level in RF path

Once the gains in the servo path have been set, the average DC level at the inputs can be calculated from the value of the servo output signals:

$$V_I = \frac{I_{Ox} \times 14\ k\Omega}{A_{LFC} - (V_{LFOFFS} + V_{COFFSx})}$$

Where I_{Ox} is the average value of the output currents at pins OA to OD.

This value is a good estimate to use initially to set the RF DC compensation, V_{RFOFFS}. The range and resolution of the RF_{OFFS} DACs are scaled with the programmed gain of G_1.

In cases where a DC coupling between TZA1038HW and the decoder is made, a fine tuning of the RF DC compensation can be done during play. The zero-crossing level of the data-eye pattern can be used to judge the correct DC compensation level.

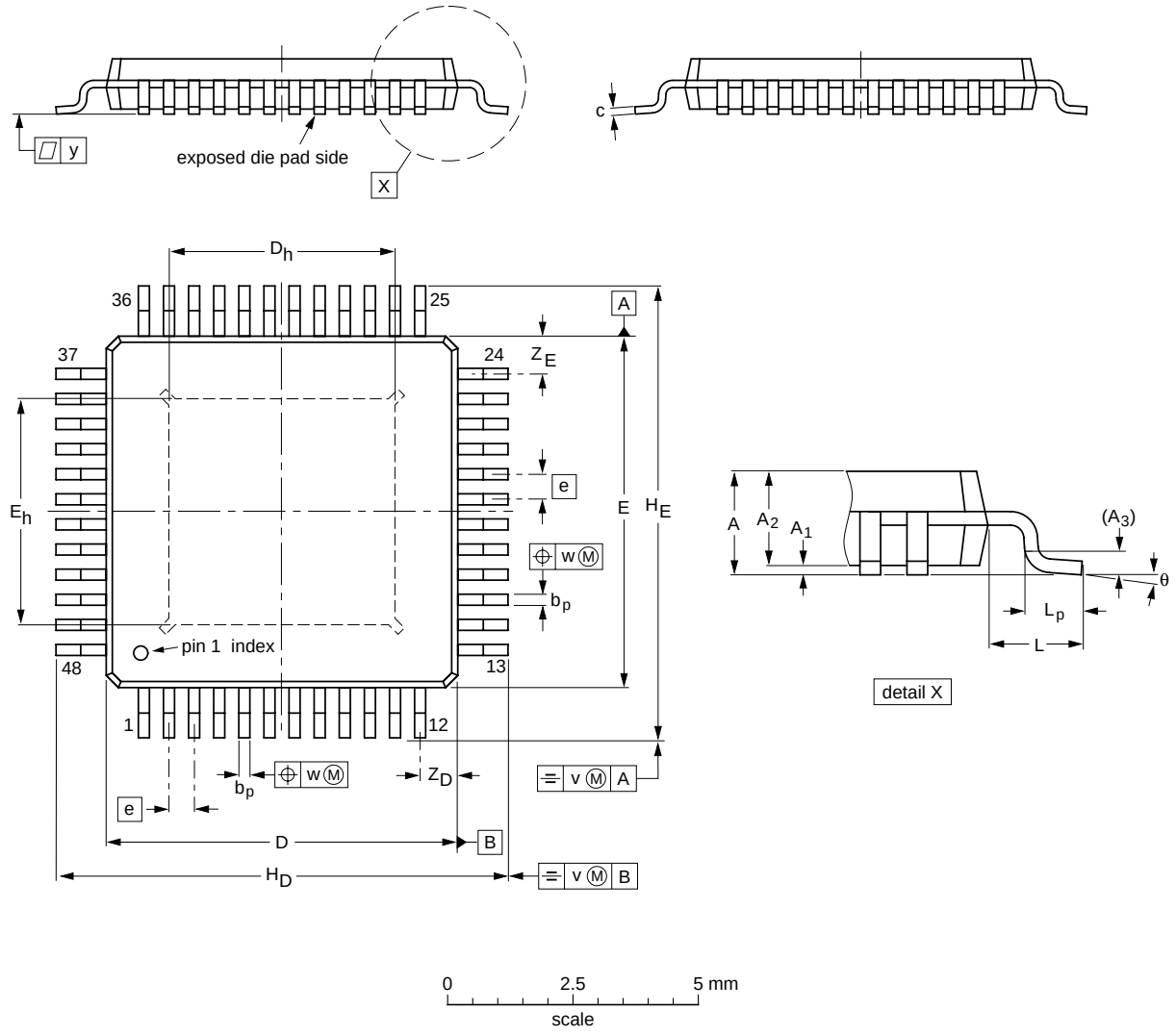
11.4.4 Gain setting RF path

The choice of RF gain is determined by the modulation of the disc, therefore the modulation needs to be checked each time a new disc is inserted in the mechanism. A trial and error procedure should be sufficient to find the optimum setting. For optimum use of the dynamic range:

- Use G_3 for fine tuning and AGC, so initially this should be set in the range 0 to 6 dB to leave an additional gain of 6 dB free to use during disc defects
- Use G_1 and G_2 to set the gain, increase G_1 first, when G_1 has reached its maximum then G_2 should be increased
- G_2 shows better noise performance in 12 and 24 dB settings than in 6 and 18 dB setting
- A similar procedure can be followed for RFSUM.

12 PACKAGE OUTLINE

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad **SOT545-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.89 0.61	0.89 0.61	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2						~~99-08-04~~ 03-04-07

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

14 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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