Actel POWER MATTERS

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Product Brief

Mixed Signal Power Manager (MPM) for Fusion

Mixed Signal Power Manager Features

Monitor, Control Power Supplies

- Simultaneously Monitor Up to 30 Power Supplies
- Up to 32 User-Defined, Digital Output Control Signals

Analog Input Monitoring

- Up to 30 Independent Analog Monitor Inputs, Plus 1 Internal Temperature, and 1 Internal Voltage Input
- 30 Analog Inputs Assignable to Voltage, Temperature, or Current Monitors
- Supported Analog Voltage Range from –10.5 V to 0 V or 0 V to +12 V

Integrated ADC and Analog I/O

- 12-Bit Resolution
- Internal 2.56 V or External Reference Voltage
- Current Monitor and Temperature Monitor Blocks
- Analog-to-Digital Converter (ADC) Accuracy Is Better Than 1%

Filters, Flags, and Control Signals

- User-Configurable Exponential Decay and Average Filtering
- Per-Channel Hysteresis and Glitch Filtering
- Five User-Configurable Thresholds Defining 6 Flag Signals Per Channel
  - OFF, UV2, UV1, NOMINAL, OV1, OV2
- 32 General Purpose Digital Output Control Signals
- 16 User-Defined Digital Inputs
- Control Signals Definable via AND/OR Combination of Inputs and Flags
  - Control Signals Can Be Inverted or Tristate Buffered
  - User-Configurable Control Signal Initial State (high, low, or high-impedance)
  - User-Configurable Control Signal Pulse Mode, Including Pulse Duration

Easy Power Sequencing

- Fifteen Power Sequence Slots—Sequenced Channels are Assignable to Any Slot
- User-Configurable Per Channel In-Slot Startup Delay, Shutdown Delay, Nominal Voltage, and Timeout
- Power-Off Sequencing Configurable as Same Order, Inverse Order, or Simultaneous

Flash-Based FPGA Fabric for Custom Control Logic

- Up to 1,500,000 System Gates Available for Custom Digital Extensions

On-Chip Clock Support

- Internal 100 MHz RC Oscillator (accurate to 1%)
- Programmable Real-Time Counter (RTC)

JTAG and I^2C Interface

- In-System Configurable via JTAG
- Single Channel Slave Mode I^2C

Block Diagram

Figure 1-1 shows a block diagram for the mixed signal power manager.

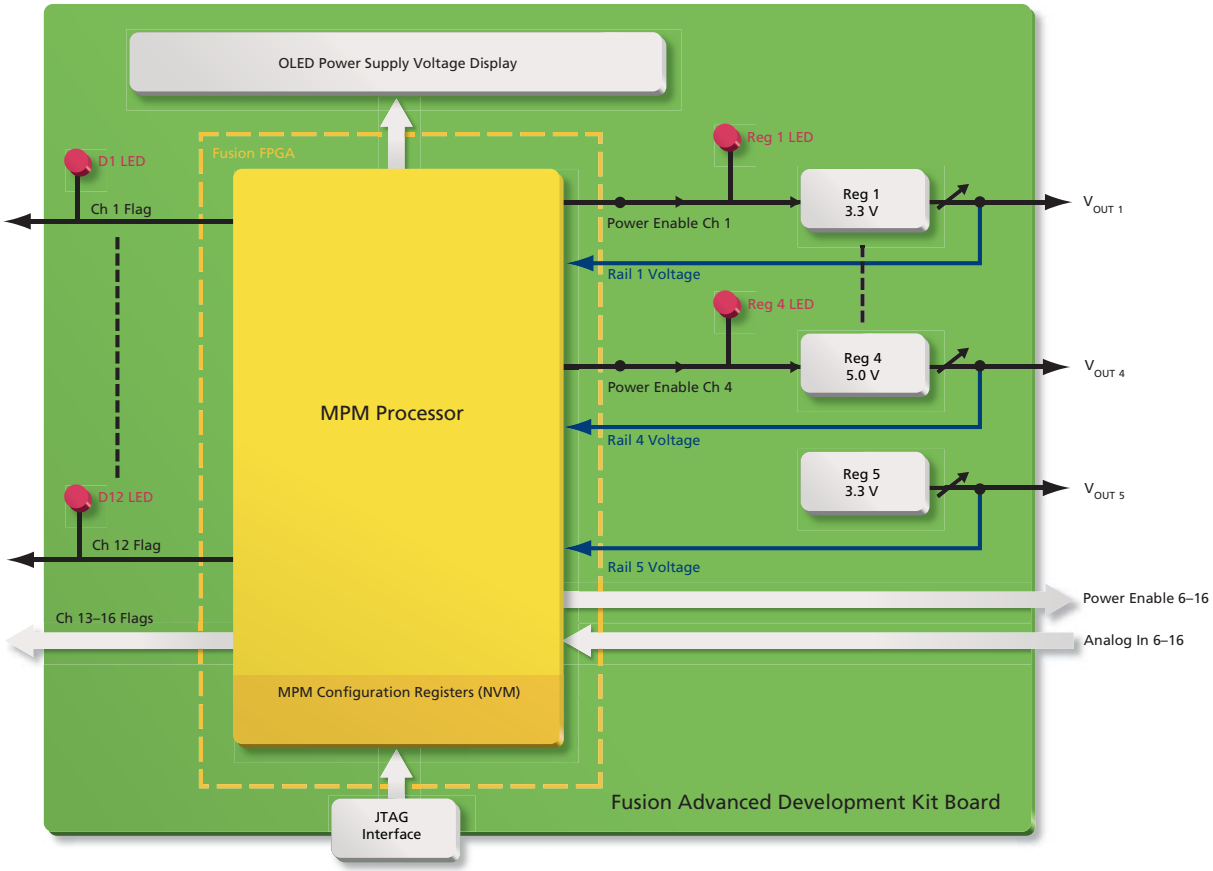

Figure 1-1 • **Block Diagram**

Description

Actel's Mixed Signal Power Manager leverages the ground-breaking Actel Fusion® mixed signal FPGA to deliver superior power monitoring, power sequencing, closed-loop trimming, and power-up and power-down control of up to 30 external power supplies. Designers do not need to deal with FPGA design tools to configure power management sequencing levels or thresholds; the MPM design is programmed into the Fusion device through an easy-to-use, standalone graphical user interface (GUI). The MPM GUI enables users to configure power management for up to 30 external power supplies and drive output signals as the monitored voltages meet or deviate from the user-programmed operating limits, all without reprogramming the FPGA. MPM reduces the total parts count at the board level, increases system reliability by eliminating the single points of failure, and delivers highly configurable, integrated power management using the highly-reliable, flash-based Fusion mixed signal FPGAs.

Using the MPM GUI, users can configure all MPM input and output requirements by writing values to the Fusion device's nonvolatile memory (NVM), using a low-cost programming stick (LCPS) via the joint test action group (JTAG) or inter-integrated circuit (I^2C) interfaces. The MPM GUI enables quick and easy setting of all threshold flag levels, output signals, power-sequencing, and debug level settings for the MPM power management operation. These settings can be quickly altered and reloaded from the GUI, allowing rapid validation in the functional hardware of all selections, settings, and sequencing without a necessity to reprogram the FPGA circuitry. All digital flag outputs are also definable via the GUI, allowing the monitoring of any condition or state for external use at the board level.

MPM functionality is demonstrated using four regulators on the Fusion Advanced Development Kit board; these four regulators function as independent power-supply channels controlled by the MPM. Additional regulator control channels and digital I/Os can be accessed using on-board mixed signal or digital headers.

Key MPM Benefits

- Configurable power management in a low-power, high-reliability, flash-based Fusion mixed signal FPGA
- Implements complex power management into hardware
- More capability than legacy non-reconfigurable application-specific standard product (ASSP) solutions
- Exploits Actel true flash key advantages
- Nonvolatile
- Live at power-up
- Low power
- Single-chip, low-power products simplify board design
- Low-power FPGA reduces thermal management and cooling needs.
- Proven in hardware
  - MPM demonstrator design available now with Fusion Advanced Development Kit at no extra cost

M1AFS1500 Demonstrator Design Example

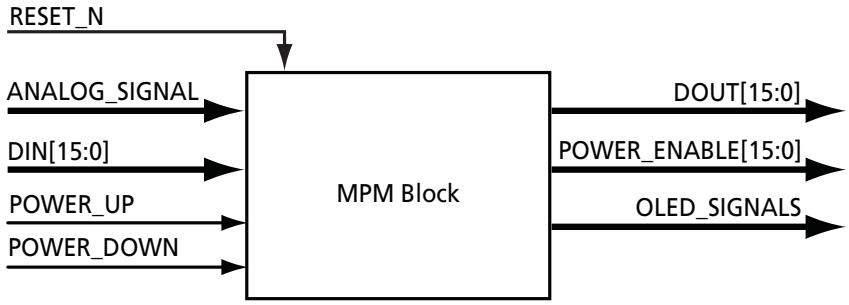

Figure 1-2 • **Analog I/O Pinout**

Pin Description Tables

Voltage ranges shown in Table 1-3 through Table 1-6 on page 1-5 are for recommended operating conditions in the commercial temperature range for the M1AFS1500 device.

Table 1-3 • **Analog I/O Pinout**

Name	Analog Pad	Description	V Range
Rail A1	AV9	On-board 5 V switching regulator output (REG3_5V)	–0.3 V to 12.0 V
Rail A2	AC9	On-board 5 V LDO regulator output (REG4_5V)	–0.3 V to 12.0 V
Rail A3	AT9	On-board 3.3 V switching regulator output (REG1_3P3)	–0.3 V to 15.5 V
Rail A4	AT7	On-board 1.5 V switching regulator output (REG2_1P5)	–0.3 V to 15.5 V
Rail A5	AC4	POT-regulated (RV5) output voltage (0 to 3.3 V)	–0.3 V to 12.0 V
Rail A6	AV3	Mixed signal header (J10) pin 5	–0.3 V to 12.0 V
Rail A7	AV5	Mixed signal header (J10) pin 7	–0.3 V to 12.0 V
Rail A8	AV6	Mixed signal header (J10) pin 11	–0.3 V to 12.0V
Rail A9	AT4	Mixed signal header (J10) pin 13	–0.3 V to 15.5V
Rail A10	AC2	Mixed signal header (J10) pin 2	–0.3 V to 12.0 V
Rail A11	AC3	Mixed signal header (J10) pin 6	–0.3 V to 12.0 V
Rail A12	AC5	Mixed signal header (J10) pin 8	–0.3 V to 12.0 V
Rail A13	AC6	Mixed signal header (J10) pin 12	–0.3 V to 12.0 V
Rail A14	AV4	PWM1 output voltage	–0.3 V to 12.0 V
Rail A15	AT5	PWM2 output voltage	–0.3 V to 15.5 V
Rail A16	AT3	Gate driver demo output voltage	–0.3 V to 15.5 V

Table 1-4 • **Digital Input Pinout**

Name	Pin	Description
DIN[0]	A3	P8051 legacy header (J31) pin 1
DIN[1]	A4	P8051 legacy header (J31) pin 3
DIN[2]	G12	P8051 legacy header (J31) pin 5
DIN[3]	A11	P8051 legacy header (J31) pin 7
DIN[4]	D11	P8051 legacy header (J31) pin 9
DIN[5]	D22	P8051 legacy header (J31) pin 11
DIN[6]	C10	P8051 legacy header (J31) pin 13
DIN[7]	F10	P8051 legacy header (J31) pin 17
DIN[8]	A9	P8051 legacy header (J31) pin 19
DIN[9]	C9	P8051 legacy header (J31) pin 21
DIN[10]	E9	P8051 legacy header (J31) pin 23
DIN[11]	A8	P8051 legacy header (J31) pin 27
DIN[12]	B8	P8051 legacy header (J31) pin 29
DIN[13]	E8	P8051 legacy header (J31) pin 31
DIN[14]	C7	P8051 legacy header (J31) pin 33
DIN[15]	A6	P8051 legacy header (J31) pin 35

Table 1-5 • Digital Output Pinout

Name	Pin	Description
DOUT[0]	B3	P8051 legacy header (J31) pin 2
DOUT[1]	B5	P8051 legacy header (J31) pin 4
DOUT[2]	B11	P8051 legacy header (J31) pin 8
DOUT[3]	E11	P8051 legacy header (J31) pin 10
DOUT[4]	A10	P8051 legacy header (J31) pin 12
DOUT[5]	D10	P8051 legacy header (J31) pin 14
DOUT[6]	G10	P8051 legacy header (J31) pin 18
DOUT[7]	B9	P8051 legacy header (J31) pin 20
DOUT[8]	D9	P8051 legacy header (J31) pin 22
DOUT[9]	F9	P8051 legacy header (J31) pin 24
DOUT[10]	G9	P8051 legacy header (J31) pin 26
DOUT[11]	D8	P8051 legacy header (J31) pin 30
DOUT[12]	A7	P8051 legacy header (J31) pin 32
DOUT[13]	D7	P8051 legacy header (J31) pin 34
DOUT[14]	B6	P8051 legacy header (J31) pin 36
DOUT[15]	D6	P8051 legacy header (J31) pin 38

Table 1-6 • Enable Output Pinout

Name	Pin	Description
POWER_ENABLE[0]	T1	On-board 5 V switching regulator enable (REG3_EN)
POWER_ENABLE[1]	P7	On-board 5 V LDO regulator enable (REG4_EN)
POWER_ENABLE[2]	R6	On-board 3.3 V switching regulator enable (REG1_EN)
POWER_ENABLE[3]	R5	On-board 1.5 V switching regulator enable (REG2_EN)
POWER_ENABLE[4]	U21	Mixed signal header (J10) pin 27
POWER_ENABLE[5]	U22	Mixed signal header (J10) pin 29
POWER_ENABLE[6]	T22	Mixed signal header (J10) pin 31
POWER_ENABLE[7]	T16	Mixed signal header (J10) pin 80
POWER_ENABLE[8]	R17	Mixed signal header (J10) pin 22
POWER_ENABLE[9]	T17	Mixed signal header (J10) pin 24
POWER_ENABLE[10]	R18	Mixed signal header (J10) pin 26
POWER_ENABLE[11]	R19	Mixed signal header (J10) pin 30
POWER_ENABLE[12]	T19	Mixed signal header (J10) pin 32
POWER_ENABLE[13]	T20	Mixed signal header (J10) pin 34
POWER_ENABLE[14]	R21	Mixed signal header (J10) pin 36
POWER_ENABLE[15]	C6	P8051 legacy header (J31) pin 37

Pin Descriptions – AFS090 Design Example

Voltage ranges shown in Table 1-7 through Table 1-10 on page 1-7 are recommended operating conditions in the commercial temperature range for the AFS090 device.

Table 1-7 • **Analog I/O Pinout**

Name	Analog Pad	Description	V Range
Rail A1	AV9	On-board 5 V switching regulator output (REG3_5V)	–0.3 V to 12.0 V
Rail A2	AC9	On-board 5 V LDO regulator output (REG4_5V)	–0.3 V to 12.0 V
Rail A3	AT9	On-board 3.3 V switching regulator output (REG1_3P3)	–0.3 V to 15.5 V
Rail A4	AT7	On-board 1.5 V switching regulator output (REG2_1P5)	–0.3 V to 15.5 V
Rail A5	AC4	POT-regulated (RV5) output voltage(0 to 3.3 V)	–0.3 V to 12.0 V
Rail A6	AV3	Mixed signal header (J10) pin 5	–0.3 V to 12.0 V
Rail A7	AV5	Mixed signal header (J10) pin 7	–0.3 V to 12.0 V
Rail A8	AV6	Mixed signal header (J10) pin 11	–0.3 V to 12.0 V
Rail A9	AT4	Mixed signal header (J10) pin 13	–0.3 V to 15.5 V
Rail A10	AC2	Mixed signal header (J10) pin 2	–0.3 V to 12.0 V
Rail A11	AC3	Mixed signal header (J10) pin 6	–0.3 V to 12.0 V
Rail A12	AC5	Mixed signal header (J10) pin 8	–0.3 V to 12.0 V
Rail A13	AC6	Mixed signal header (J10) pin 12	–0.3 V to 12.0 V
Rail A14	AV4	PWM1 output voltage	–0.3 V to 12.0 V
Rail A15	AT5	PWM2 output voltage	–0.3 V to 15.5 V
Rail A16	AT3	Gate driver demo output voltage	–0.3 V to 15.5 V

Table 1-8 • **Digital Input Pinout**

Name	Pin	Description
DIN[0]	A3	P8051 legacy header (J31) pin 1
DIN[1]	A4	P8051 legacy header (J31) pin 3
DIN[2]	G12	P8051 legacy header (J31) pin 5
DIN[3]	A11	P8051 legacy header (J31) pin 7
DIN[4]	D11	P8051 legacy header (J31) pin 9
DIN[5]	D22	P8051 legacy header (J31) pin 11
DIN[6]	C10	P8051 legacy header (J31) pin 13
DIN[7]	F10	P8051 legacy header (J31) pin 17
DIN[8]	A9	P8051 legacy header (J31) pin 19
DIN[9]	C9	P8051 legacy header (J31) pin 21
DIN[10]	E9	P8051 legacy header (J31) pin 23
DIN[11]	A8	P8051 legacy header (J31) pin 27
DIN[12]	B8	P8051 legacy header (J31) pin 29
DIN[13]	E8	P8051 legacy header (J31) pin 31
DIN[14]	C7	P8051 legacy header (J31) pin 33
DIN[15]	A6	P8051 legacy header (J31) pin 35

Table 1-9 • **Digital Output Pinout**

Name	Pin	Description
DOUT[0]	B3	P8051 legacy header (J31) pin 2
DOUT[1]	B5	P8051 legacy header (J31) pin 4
DOUT[2]	B11	P8051 legacy header (J31) pin 8
DOUT[3]	E11	P8051 legacy header (J31) pin 10
DOUT[4]	A10	P8051 legacy header (J31) pin 12
DOUT[5]	D10	P8051 legacy header (J31) pin 14
DOUT[6]	G10	P8051 legacy header (J31) pin 18
DOUT[7]	B9	P8051 legacy header (J31) pin 20
DOUT[8]	D9	P8051 legacy header (J31) pin 22
DOUT[9]	F9	P8051 legacy header (J31) pin 24
DOUT[10]	G9	P8051 legacy header (J31) pin 26
DOUT[11]	D8	P8051 legacy header (J31) pin 30
DOUT[12]	A7	P8051 legacy header (J31) pin 32
DOUT[13]	D7	P8051 legacy header (J31) pin 34
DOUT[14]	B6	P8051 legacy header (J31) pin 36
DOUT[15]	D6	P8051 legacy header (J31) pin 38

Table 1-10 • **Enable Output Pinout**

Name	Pin	Description
POWER_ENABLE[0]	T1	On-board 5 V switching regulator enable (REG3_EN)
POWER_ENABLE[1]	P7	On-board 5 V LDO regulator enable (REG4_EN)
POWER_ENABLE[2]	R6	On-board 3.3 V switching regulator enable (REG1_EN)
POWER_ENABLE[3]	R5	On-board 1.5 V switching regulator enable (REG2_EN)
POWER_ENABLE[4]	U21	Mixed signal header (J10) pin 27
POWER_ENABLE[5]	U22	Mixed signal header (J10) pin 29
POWER_ENABLE[6]	T22	Mixed signal header (J10) pin 31
POWER_ENABLE[7]	T16	Mixed signal header (J10) pin 80
POWER_ENABLE[8]	R17	Mixed signal header (J10) pin 22
POWER_ENABLE[9]	T17	Mixed signal header (J10) pin 24
POWER_ENABLE[10]	R18	Mixed signal header (J10) pin 26
POWER_ENABLE[11]	R19	Mixed signal header (J10) pin 30
POWER_ENABLE[12]	T19	Mixed signal header (J10) pin 32
POWER_ENABLE[13]	T20	Mixed signal header (J10) pin 34
POWER_ENABLE[14]	R21	Mixed signal header (J10) pin 36
POWER_ENABLE[15]	C6	P8051 legacy header (J31) pin 37

```
**********************************************************************
Pin Report - Date: Tue Sep 08 16:08:44 2009 Pinchecksum: NOT-AVAILABLE
Product: Designer
Release: v8.6
Version: 8.6.0.34
Design Name: MPM_SYSTEM
Family: Fusion
Die: AFS090
Package: 256 FBGA
**********************************************************************
```

Port	Pin	Fixed	Function	I/O Standard	Output Drive (mA)	Slew	Resistor Pull	Skew	Output Load (pF)	Use I/O Reg	Hot Swappable
AC[0]	L8	Yes	AC0	LVTTL	---	Low	---	---	---	No	No
AC[1]	N7	Yes	AC1	LVTTL	---	Low	---	---	---	No	No
AC[2]	M9	Yes	AC2	LVTTL	---	Low	---	---	---	No	No
AC[3]	L10	Yes	AC3	LVTTL	---	Low	---	---	---	No	No
AC[4]	M10	Yes	AC4	LVTTL	---	Low	---	---	---	No	No
AT[0]	R6	Yes	AT0	LVTTL	---	Low	---	---	---	No	No
AT[1]	T5	Yes	AT1	LVTTL	---	Low	---	---	---	No	No
AT[2]	T7	Yes	AT2	LVTTL	---	Low	---	---	---	No	No
AT[3]	R8	Yes	AT3	LVTTL	---	Low	---	---	---	No	No
AT[4]	T9	Yes	AT4	LVTTL	---	Low	---	---	---	No	No
AV[0]	R5	Yes	AV0	LVTTL	---	Low	---	---	---	No	No
AV[1]	R7	Yes	AV1	LVTTL	---	Low	---	---	---	No	No
AV[2]	L9	Yes	AV2	LVTTL	---	Low	---	---	---	No	No
AV[3]	N9	Yes	AV3	LVTTL	---	Low	---	---	---	No	No
AV[4]	R9	Yes	AV4	LVTTL	---	Low	---	---	---	No	No
DIN[0]	C11	Yes	IO20RSB0V0	LVTTL	---	---	None	---	---	No	No
DIN[1]	D11	Yes	IO23RSB0V0	LVTTL	---	---	None	---	---	No	No
DIN[2]	B13	Yes	GBC1/IO26RSB0V0	LVTTL	---	---	None	---	---	No	No
DIN[3]	A13	Yes	GBC0/IO25RSB0V0	LVTTL	---	---	None	---	---	No	No
DIN[4]	N2	Yes	GEA2/IO42NDB3V0	LVTTL	---	---	None	---	---	No	No
DIN[5]	A14	Yes	GBA0/IO29RSB0V0	LVTTL	---	---	None	---	---	No	No
DIN[6]	D2	Yes	GFA2/IO51NDB3V0	LVTTL	---	---	None	---	---	No	No

Port	Pin	Fixed	Function	I/O Standard	Output Drive (mA)	Slew	Resistor Pull	Skew	Output Load (pF)	Use I/O Reg	Hot Swappable
DIN[7]	H2	Yes	GEB0/IO45NDB3V0	LVTTL	---	---	None	---	---	No	No
DOUT[0]	G1	Yes	GEC0/IO46NPB3V0	LVTTL	8	High	None	No	35	No	No
DOUT[1]	J16	Yes	GDA2/IO40NDB1V0	LVTTL	8	High	None	No	35	No	No
DOUT[2]	J11	Yes	GDC2/IO41NPB1V0	LVTTL	8	High	None	No	35	No	No
DOUT[3]	J14	Yes	GDA0/IO40PDB1V0	LVTTL	8	High	None	No	35	No	No
DOUT[4]	E11	Yes	IO24RSB0V0	LVTTL	8	High	None	No	35	No	No
DOUT[5]	N1	Yes	GEB2/IO42PDB3V0	LVTTL	8	High	None	No	35	No	No
DOUT[6]	B14	Yes	GBA1/IO30RSB0V0	LVTTL	8	High	None	No	35	No	No
DOUT[7]	F6	Yes	GFC1/IO49PDB3V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[0]	B3	Yes	GAA0/IO00RSB0V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[1]	A10	Yes	IO17RSB0V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[2]	E14	Yes	GCC2/IO33NDB1V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[3]	H11	Yes	GDC0/IO38NDB1V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[4]	D15	Yes	GBC2/IO32PDB1V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[5]	D16	Yes	GCA2/IO32NDB1V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[6]	A4	Yes	GAB1/IO03RSB0V0	LVTTL	8	High	None	No	35	No	No
POWER_ENABLE[7]	L15	Yes	GDB2/IO41PPB1V0	LVTTL	8	High	None	No	35	No	No
PSW[0]	D3	Yes	GAC2/IO51PDB3V0	LVTTL	---	---	None	---	---	No	No
PSW[1]	D4	Yes	GAA2/IO52PDB3V0	LVTTL	---	---	None	---	---	No	No
RESET_N	D1	Yes	GFC2/IO50NPB3V0	LVTTL	---	---	None	---	---	No	No
VAREF	T15	Fixed	VAREF								
XTL	H4	Fixed	XTAL								

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

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