NCV7729

8 A H-Bridge Driver

The NCV7729 is an intelligent, fully protected H−Bridge Driver designed specifically for control of DC and stepper motors in safety critical applications under automotive/industrial environment.

Features

- Operating V_S Battery Supply Voltage 5 V to 28 V
- Operating V_{CC} Supply Voltage 3.0 to 5.5 V
- 18 V Survivability on V_{CC} and All Logic I/O Pins
- Typical $R_{DS(on)}$ = 150 mΩ, $R_{DS(MAX)}$ = 300 mΩ (150°C)
- Continuous DC Load Current 5A (TC < 100°C)
- Selectable Output Current Limitation (2.5 A to 9.6 A)
- Output Switching Frequency Up to 30 kHz
- Monitoring of All Supply Voltages, Safe Power−up State
- Loss of GND Detection
- Short−Circuit Protection and Thermal Shutdown
- Full Diagnosis Capability for Open Load, Short to GND/VS and Shorted Load Conditions
- SPI Interface for Configuration and Diagnosis
- Undervoltage Lockout
- Regulated Charge Pump for Optimized EMI Behavior
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- This is a Pb−Free Device

Typical Applications

- Automotive
  - Electronic Throttle Control (ETC)
  - Variable Intake Geometry
  - Exhaust Gas Recirculation
  - Variable Swirl
  - Blow−off Flap
- Industrial

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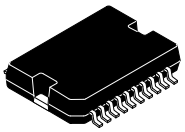
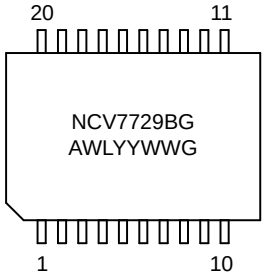
http://onsemi.com



PSOP−20
CASE 525AB

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7729BPPR2G	PSOP−20 (Pb−Free)	750 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

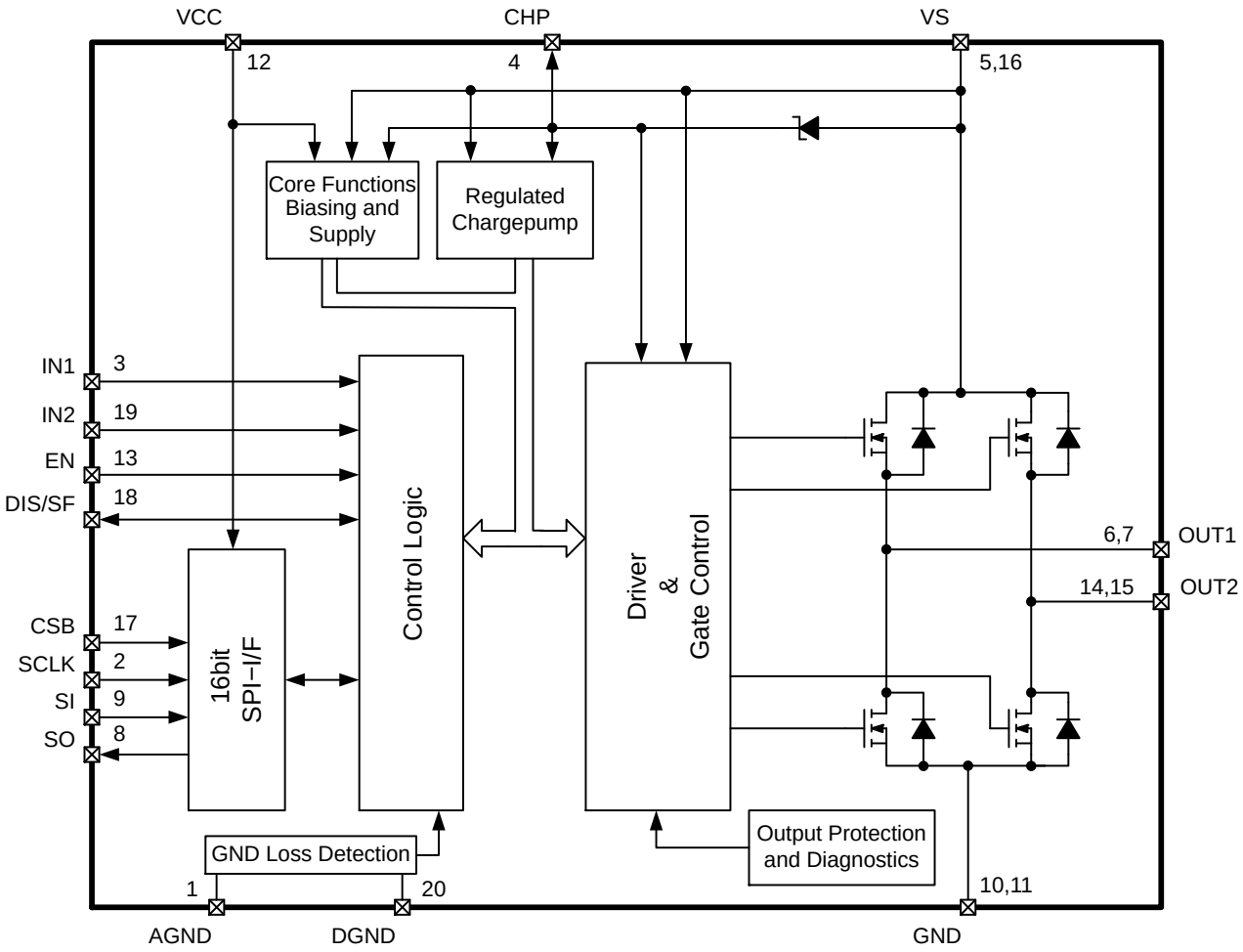


Figure 1. Block Diagram

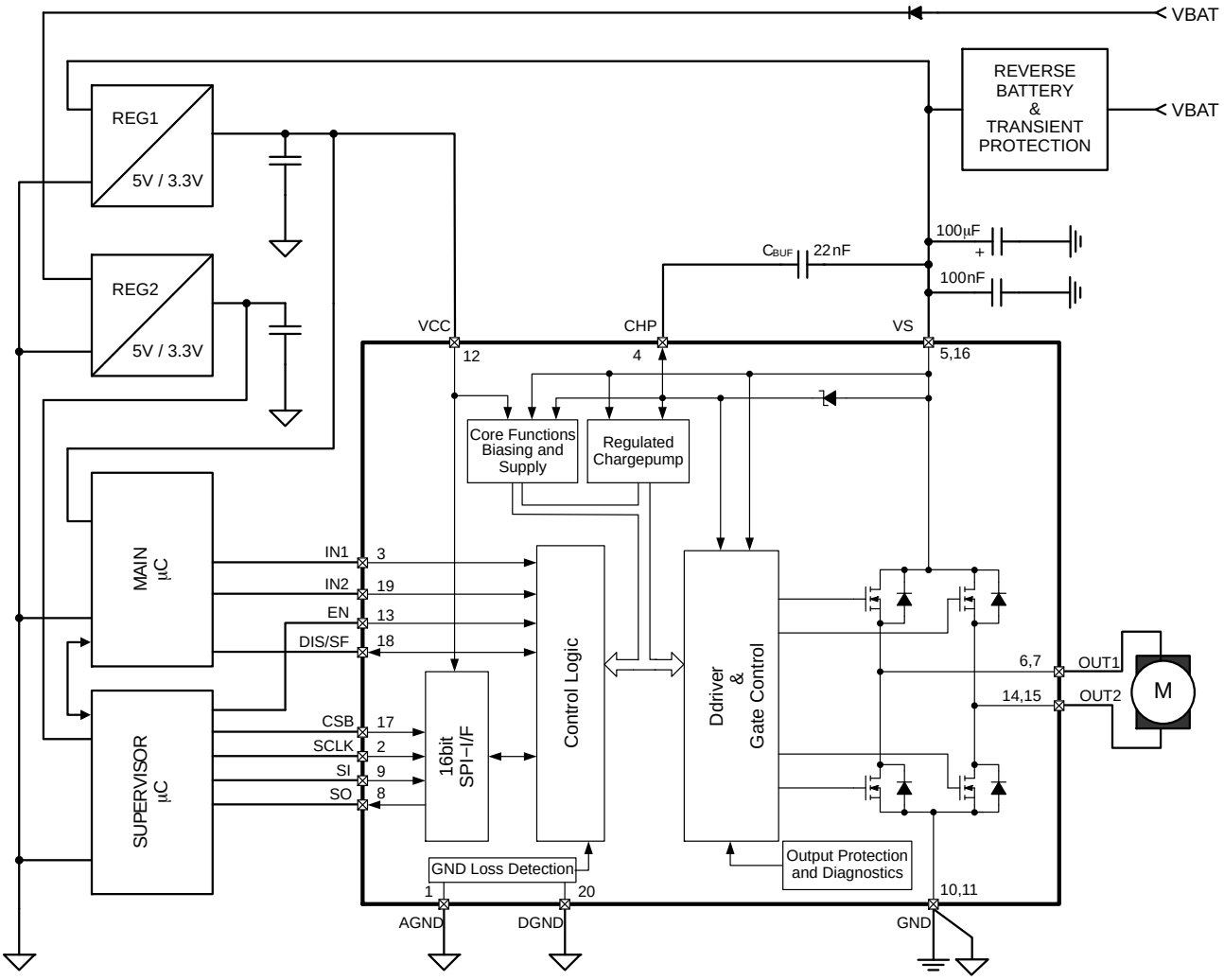


Figure 2. ETC Application Diagram

PACKAGE PIN DESCRIPTION

Pin#	Symbol	Description
1	AGND	Analog Ground; Device Substrate.
2	SCLK	Serial Clock. Clock input for SPI communication (internal pullup to V_{CC})
3	IN1	Control Input 1 (internal pullup to V_{CC})
4	CHP	Charge pump in/output
5	VS	Supply voltage; must be connected to pin 16 externally
6	OUT1	Output1; must be connected to pin 7 externally
7	OUT1	Output1; must be connected to pin 6 externally
8	SO	Serial Output. 16 bit SPI communications output.
9	SI	Serial Input. 16 bit SPI communications input (internal pullup to V_{CC})
10	GND	Power Ground.
11	GND	Power Ground.
12	VCC	Power supply for logic
13	EN	Enable input (internal pulldown to AGND)
14	OUT2	Output2; connect to pin 15 externally
15	OUT2	Output2; connect to pin 14 externally
16	VS	Supply voltage; must be connected to pin 5 externally
17	CSB	Chip Select Bar Input. Active low SPI port operation (internal pullup to V_{CC})
18	DIS/SF	Disable Input / Status Flag Output (Open drain w/ internal pullup to V_{CC})
19	IN2	Control Input 2 (pullup to V_{CC})
20	DGND	Digital Ground.
HEAT SLUG		Internally Connected to AGND; Device Substrate

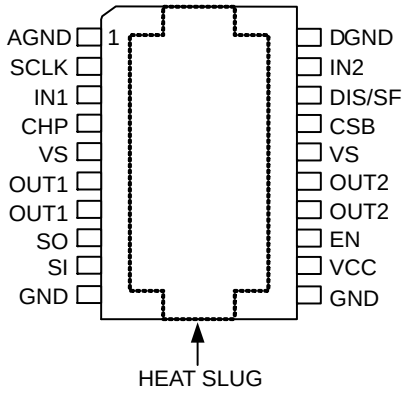


Figure 3. Package Pinout
(Top View)

MAXIMUM RATINGS (Voltages are with respect to device substrate.)

Rating	Value	Unit
Battery Supply and Power Outputs (VS, OUTx) (DC) (AC), t < 500 ms	 −1 to 40 −2	V
Digital Supply (V_{CC}), Logic input/output pins (EN, DIS/SF, INx, CSB,SCLK, SO, SI)	 −0.5 to 18	V
Charge pump Supply, relative to VS V(CHP) − V(VS)	16	V
Operating Junction Temperature Continuous t < 1 s	 −40 to 150 175	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free − 60 to 150 seconds at 217°C (Note 1)	260 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For additional information, see or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D, and Application Note AND8003/D.

ATTRIBUTES

Characteristic	Value	Unit
Electrostatic Discharge, Human Body Model (MIL Std 883D) All pins Battery / Output Pins (VS, OUTx) (Note 3)	 ≥ ±2 ≥ ±8	kV
Electrostatic Discharge, CDM	≥ ±800	V
Moisture Sensitivity Level (Note 2)	MSL 1	−
Thermal Resistances Junction − to − ambient (copper area, thickness) Theta JA (100 mm2, 2 oz) (Note 4) Theta JA (300 mm2, 2 oz) (Note 4) Theta JA (600 mm2, 2 oz) (Note 4) Psi J−Board solder pad	 78 47 36 1.5	°C/W
Package Thermal Time Constant	1	sec

2. For additional information, see or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D, and Application Note AND8003/D.
3. VS pins (pin 5, 16) connected together; all GND pins (pin 1, 10, 11, 20) connected together.
4. Thermal estimates are based on mounting the package on a 30 x 70 x 1.5 mm FR4 substrate. Copper areas include traces and mounting area of the device. 1 oz is equivalent to 0.035 mm thick copper. Test/simulation is based on JEDEC JESD51.1, JESD51.2, and JESD51.3 standards still air chamber boundary conditions steady state thermal performance.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCCop	Digital supply input voltage (V_{CC})	3	5.5	V
VSop	Battery supply input voltage (V_S)	5	28	V
 fophi foplo	INx PWM Frequency (C_{BUF} = 22 nF) Charge pump in full power mode Charge pump in reduced power mode	 −	 30 4	kHz
T_J	Junction temperature	−40	150	°C
T_{Jac}	Junction temperature − transient (t < 1s)		175	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5 V < V_S < 28 V, 3 V < V_{CC} < 5.5 V, EN = V_{CC}, DIS/SF = GND, C_{BUF} = 22 nF, unless otherwise specified) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
V_S Supply Current	IVSop,pwm	f_{pwm} = 20 kHz, I_{out} = 0 A	−	−	30	mA
	IVSop,dc	f_{pwm} = 0, I_{out} = 0 A	−	−	5.5	mA
	IVSdiag	DIS/SF = V_{CC}, EN = 0, SCLK = 0, VS = 13.2 V Config.Enx = 1 OUT1 tied to OUT2	−	−	6.0	mA
	IVSdis	DIS/SF = V_{CC}, EN = 0, SCLK = 0, V_S = 13.2 V Config.Enx = 0 0 ≤ V_{CC} ≤ 5.5V T_A ≤ 85°C; (Note 6)	−	−	5.0	μA
V_{CC} Supply Current	IVCCop	CSB = V_{CC}, Outputs enabled	−	−	2.0	mA
V_{CC} Undervoltage Lockout	VCCPORon	Power−on reset, rising	2.5	−	3.0	V
V_{CC} POR Hysteresis	VCCPORhy		0.1	−	−	V
V_{CC} Overvoltage Lockout	VCCOV		5.5	−	−	V
V_S Undervoltage Lockout	VSPORoff	Switch−off threshold, falling; (Note 7)	3.6	4.4	5.0	V
	VSPORon	Switch−on threshold, rising	3.8	4.6	5.2	V
V_S POR Hysteresis	VSPORhy		0.1	−	0.5	V
Power supply lockout delay	PORdly	V_{CC}, V_S, or CHP	−	20	50	μs
Loss of Ground Lockout Threshold	G_{DIF}	|V(AGND) − V(DGND)|	−	−	300	mV
C_{BUF} = 22 nF, f_{pwm} = 30 kHz, CHP Full Power Mode						
CHP regulation voltage	VCHP	V(CHP) − V(VS)	−	10	13	V
CHP Undervoltage lockout	VCHPLV	V(CHP) − V(VS) falling	4.5	−	6	V
CHP Undervoltage Hysteresis	VCHPhy		100	−	400	mV
CHP output current limitation	ILIMCHP	V(CHP) = 0 V	−	−	30	mA
CHP allowable external leakage	ICHPlkg	V(CHP) − V(VS), V_S = 13.2 V, ICHPlkg = −150 μA	8	−	−	V
CHP power on delay time V_{CC} or V_S POR release Until OUTx active	t_{dact}	V(CHP) > VCHPLV	−	−	1.0	ms
POWER OUTPUTS − DC Characteristics						
Output Transistor ON Resistance	RonOUTx	V_S > 5 V, I_{OUT} = 3 A	−	150	300	mΩ
	RonOUTxGM	V_S > 5 V, I_{OUT} = 3 A, T_J = −30°C	−	−	135	mΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
6. The load must be connected between OUT1 and OUT 2 to achieve the low−quiescent current standby mode.
7. VS must first exceed the VSPORon switch−on threshold for operation down to VSPORoff.
8. The ISDLSx and ISDHSx thresholds are unaffected during temperature dependant current limit reduction.
9. No production test.
10. Latency time between overcurrent or overtemp shutdown to reactivation of output stage via ENA or DIS/SF.
11. Minimum latency between successive frames.
12. Minimum hold time after ENA H → L or DIS/SF L → H.

ELECTRICAL CHARACTERISTICS (continued)
(−40°C < T_J < 150°C, 5 V < V_S < 28 V, 3 V < V_{CC} < 5.5 V, EN = V_{CC}, DIS/SF = GND, C_{BUF} = 22 nF, unless otherwise specified) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER OUTPUTS − DC Characteristics						
LS Current limit switch−off threshold	ILIMLSx	Config.OCx = IC4 Config.OCx = IC3 (default) Config.OCx = IC2 Config.OCx = IC1	8.0 5.4 4.4 2.0	9.6 6.6 5.5 2.5	11.1 7.8 6.6 3.0	A
LS Current limit vs. Overcurrent tracking	ItrackLS	ISDLSx − ILIMLSx	2	−	−	A
LS Overcurrent shutdown threshold	ISDLSx (Note 8)	Config.OCx = IC4 Config.OCx = IC3 (default) Config.OCx = IC2 Config.OCx = IC1	− 8.5 − −	15.0 10.8 9.5 4.9	− 13.0 − −	A
LS Overcurrent shutdown tracking	ItrackSDLS	IC4 − IC3 IC3 − IC2 IC3 − IC1	3.0 0.8 4.1	4.3 1.2 5.5	5.6 1.6 6.9	A
HS Overcurrent shutdown threshold	ISDHSx (Note 8)	Config.OCx = IC4 Config.OCx = IC3 (default) Config.OCx = IC2 Config.OCx = IC1	− −13.0 − −	−15.0 −10.8 −9.5 −4.9	− −8.5 − −	A
HS Overcurrent shutdown tracking	ItrackSDHS	IC4 − IC3 IC3 − IC2 IC3 − IC1	−5.6 −1.6 −6.9	−4.3 −1.2 −5.5	−3.0 −0.8 −4.1	A
OUTx leakage current	Ileak, OUTx	DIS/SF = V_{CC}, EN = 0, SCLK = 0, V_S = 28 V Config.Enx = 0 V(OUTx) = 0 V	−20	0	−	μA
Start of temperature dependant current limit reduction	TLIM	(Note 9)	150	165	−	°C
Thermal Shutdown	TSD	(Note 9)	175	−	−	°C
Free−wheel diode forward voltage	VD	OUTx off, I(OUT) = 3 A	−	−	2.0	V
POWER OUTPUTS − AC Characteristics						
Free−wheel diode reverse recovery time	trr	(Note 9)	−	−	100	ns
Disable delay time EN or DIS/SF→OUTx	tpddis		−	−	2.0	μs
Output ON delay − INx→OUTx	tdon	RL = 5 Ω, V_S = 15 V	−	−	4.0	μs
Output OFF delay − INx→OUTx	tdoff		−	−	4.0	μs
Output switching time OUTxH→OUTxL or OUTxL→OUTxH	tr,tf		−	−	4.0	μs
LS Current limit blanking time	tb	V_S = 13.2 V; L = 0.75 mH, R = 0.2 Ω	14	20.5	27	μs
LS Current limit switch−off time	ta		16	23.5	31	μs
Switch−off to blanking tracking	ta/tb		1.0	−	−	−
Overcurrent fault filter time	tdfault		1.0	2.0	−	μs
Reactivation time after internal shutdown	treact	(Notes 9 and 10)	−	−	200	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
6. The load must be connected between OUT1 and OUT 2 to achieve the low−quiescent current standby mode.
7. VS must first exceed the VSPORon switch−on threshold for operation down to VSPORoff.
8. The ISDLSx and ISDHSx thresholds are unaffected during temperature dependant current limit reduction.
9. No production test.
10. Latency time between overcurrent or overtemp shutdown to reactivation of output stage via ENA or DIS/SF.
11. Minimum latency between successive frames.
12. Minimum hold time after ENA H → L or DIS/SF L → H.

ELECTRICAL CHARACTERISTICS (continued)
(−40°C < T_J < 150°C, 5 V < V_S < 28 V, 3 V < V_{CC} < 5.5 V, EN = V_{CC}, DIS/SF = GND, C_{BUF} = 22 nF, unless otherwise specified) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
OPEN LOAD DIAGNOSTICS						
Open Load Diagnostic Threshold	Vth1	EN = GND or DIS/SF = V_{CC} Config.ENx = 1	1.25	−	2	V
	Vth2		1.25	−	2	V
Diagnostic Pullup current	I(OUT1)	V(VS) = 13.2 V, V(OUT1) = 2 V	−2000	−	−1000	μA
Diagnostic Pulldown current	I(OUT2)	V(VS) = 13.2 V, V(OUT2) = 1.25 V	700	−	1400	μA
Diagnostic current tracking	I(OUT1) / I(OUT2)		1.2	−	1.8	−
Open Load Detection Delay time	tddiag		40	−	110	ms
MICROCONTROLLER INTERFACE − DC CHARACTERISTICS						
Digital Input Threshold SI, SCLK, CSB, EN, DIS/SF, INx	VTHIN		− 30	−	70 −	%VCC
Input Hysteresis	VHYIN		2	−	10	%VCC
Input Pulldown Current EN	IPDEN	V(EN) = V_{CC}	−	−	100	μA
Input Pullup Current DIS/SF, INx SI, SCLK, CSB	IPUx	V(pin) = 0 V	−200 −50	−125 −20	−	μA
DIS/SF Output voltage Output condition LOW	VSFL	Config.DIS/SF = 1, I(DIS/SF) = 1 mA	−	−	0.4	V
SO − Output High	VSOH	I(SO) = −1 mA, V_{CC} = 5.0 V	V_{CC} − 0.5	−	−	V
SO − Output Low	VSOL	I(SO) = 1.6 mA	−	−	0.4	V
SO Tristate Leakage	ILSO	CSB = V_{CC}	−10	−	10	μA
MICROCONTROLLER INTERFACE − AC CHARACTERISTICS (V_{CC} = 5 V, unless otherwise specified)						
Input Capacitance SI, SCLK, CSB, EN, DIS/SF, INx	CINx	(Note 9)	−	−	20	pF
SO Tristate Capacitance	CSO	(Note 9)	−	−	35	pF
SCLK Frequency		V_{CC} = 5 V V_{CC} = 3.3 V	− −	− −	5 2	MHz
SCLK Clock Period			200	−	−	ns
SCLK High Time	Figure 4 #1		85	−	−	ns
SCLK Low Time	Figure 4 #2		85	−	−	ns
SCLK Setup Time	Figure 4 #3,4		85	−	−	ns
SI Setup Time	Figure 4 #11		50	−	−	ns
SI Hold Time	Figure 4 #12		50	−	−	ns
CSB Setup Time	Figure 4 #5,6		100	−	−	ns
CSB High Time	Figure 4 #7	(Note 11)	200	−	−	ns

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5. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
6. The load must be connected between OUT1 and OUT 2 to achieve the low−quiescent current standby mode.
7. VS must first exceed the VSPORon switch−on threshold for operation down to VSPORoff.
8. The ISDLSx and ISDHSx thresholds are unaffected during temperature dependant current limit reduction.
9. No production test.
10. Latency time between overcurrent or overtemp shutdown to reactivation of output stage via ENA or DIS/SF.
11. Minimum latency between successive frames.
12. Minimum hold time after ENA H → L or DIS/SF L → H.

ELECTRICAL CHARACTERISTICS (continued)
(−40°C < T_J < 150°C, 5 V < V_S < 28 V, 3 V < V_{CC} < 5.5 V, EN = V_{CC}, DIS/SF = GND, C_{BUF} = 22 nF, unless otherwise specified) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE − AC CHARACTERISTICS (V_{CC} = 5 V, unless otherwise specified)						
SO Rise Time		Cload = 40 pF	−	−	25	ns
SO Fall Time		Cload = 40 pF	−	−	25	ns
SO Valid time	Figure 4 #10	Cload = 40 pF; (Note 9)	−	−	40	ns
		Cload = 200 pF; (Note 9)	−	−	150	ns
EN or DIS/SF Hold time		EN = L or DIS/SF = H (Note 12)	2.0	−	−	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
6. The load must be connected between OUT1 and OUT 2 to achieve the low−quiescent current standby mode.
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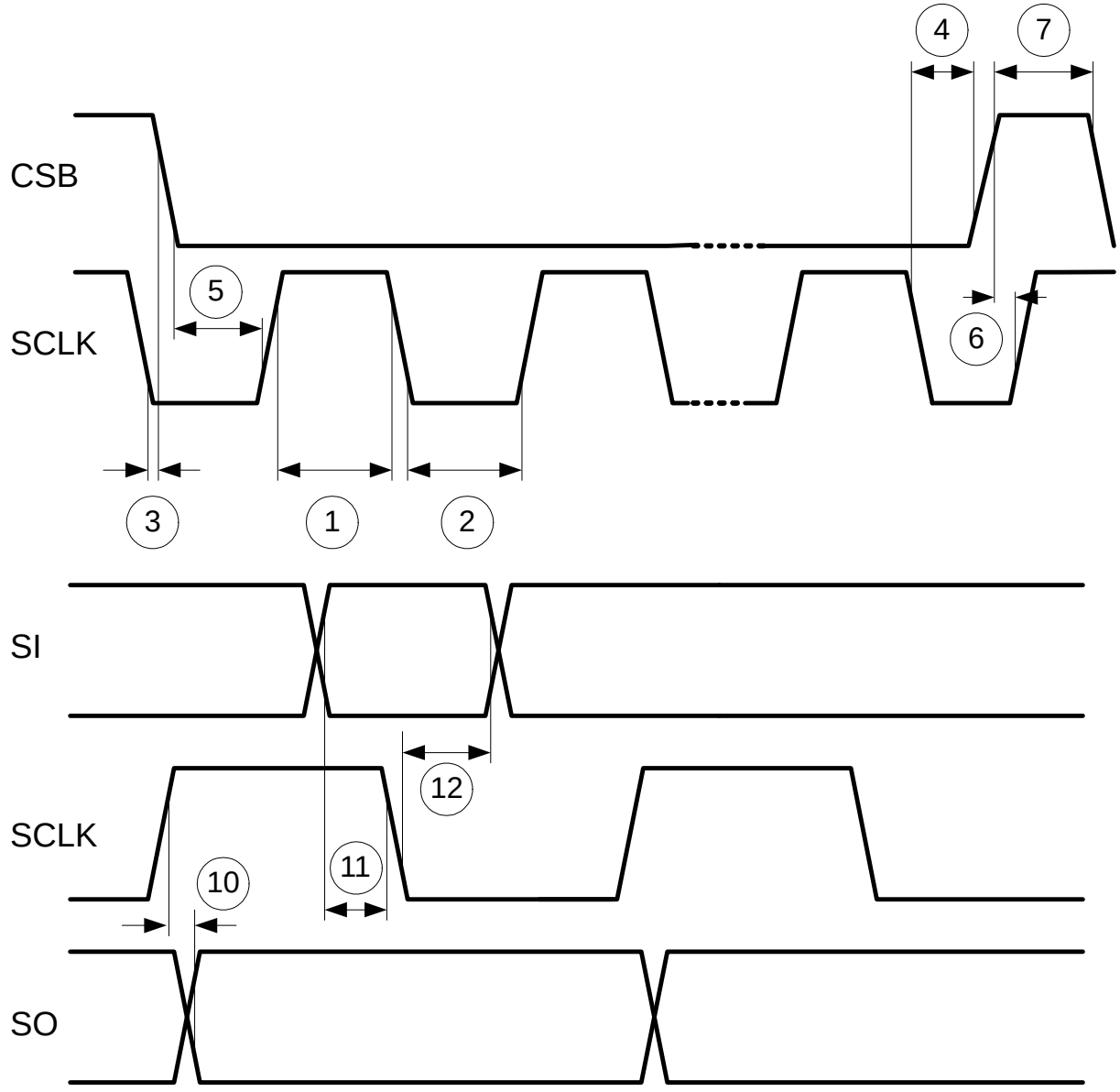


Figure 4. SPI Timing Parameters

DETAILED OPERATING DESCRIPTION

Bridge Control Inputs

The integrated switches can be controlled by input signals (INx) as well as via the SPI Interface. Mode selection is performed via the SPI configuration register. The device provides two enable inputs: EN = active high and DIS/SF = active low. Besides the two direct enable inputs EN and DIS/SF, the device provides two SPI−controllable bits in the configuration register (Config.ENx) to support a low−quiescent current standby mode or advanced error handling (e.g. channel deactivation).

The default setting for DIS/SF is to operate as an enable input. By setting bit Config.SFMODE in the Config register (SPI command WR_Config), the functionality of DIS/SF can be altered to operate as an open−drain status flag output. The Config register can be accessed via the SPI port independently of the setting at DIS/SF.

All control inputs provide internal pullup (IN1, IN2, DIS/SF) or pulldown (EN) to ensure defined functionality in case of open pin conditions. Bridge control logic is shown in Figure 5 and Table 1 demonstrates all Operational Modes.

Table 1. H−BRIDGE OPERATIONAL MODES

Operational Mode	EN (Note 13)	DIS/SF IN (Note 14)	IN1 (Note 16)	IN2 (Note 16)	OUT1	OUT2	SPI	DIS/SF OUT (Note 15)
Forward	H	L	H	L	H	L	see SPI diagnostic description	H
Reverse	H	L	L	H	L	H		H
Free−wheeling low	H	L	L	L	L	L		H
Free−wheeling high	H	L	H	H	H	H		H
Disable via DIS/SF (Note 14)	X	H	X	X	Z	Z		−
Disable via EN	L	X	X	X	Z	Z		L
EN disconnected	L	X	X	X	Z	Z		L
DIS/SF disconnected	X	H	X	X	Z	Z		X
IN1 disconnected	H	L	H	X	H	X		H
IN2 disconnected	H	L	X	H	X	H		H
Current limitation active	H	L	X	X	(Note 17)	(Note 17)		H
Under voltage (V_S, CHP)	H	L	X	X	Z	Z		L
Overtemp shutdown	H	L	X	X	Z	Z		L
Overcurrent shutdown	H	L	X	X	Z	Z		L
V_{CC} under/over voltage	X	X	X	X	Z	Z		H

13. EN pulled down by internal current IPDEN.
14. DIS/SF configured as enable input (Config.SFMODE = 0, default setting); pulled up by internal current IPUx.
15. DIS/SF configured as status flag output (Config.SFMODE= 1); pulled up by internal current IPUx or external resistor.
16. Device outputs enabled in Config Register (Config.EN1 = 1, Config.EN2 = 1, default setting); pulled up by internal current IPUx.
17. Affected output pulsing. See output protection description.

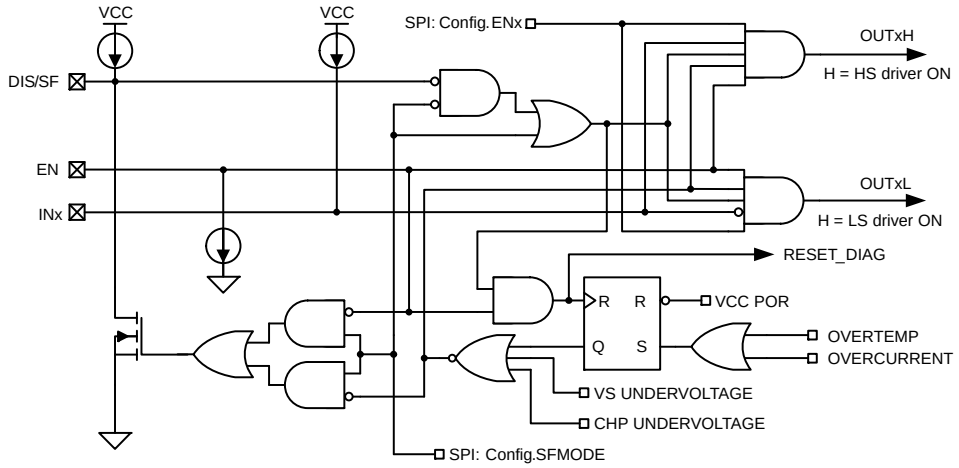


Figure 5. Bridge Control Logic

Bridge Outputs

The H−Bridge output is built up by four N−channel power DMOS devices (150 mΩ typ, 300 mΩ max @ 150°C). All transistors are protected against overcurrent and overtemperature conditions induced by short circuit conditions to GND, V_S, or across the load. Positive and negative voltage transients that occur during switching events of inductive loads are clamped by integrated freewheeling diodes. An integrated regulated chargepump is provided to drive the gates of the high−side DMOS transistors.

Output Protection

To prevent device destruction in case of external fault conditions (OUTx shorted to GND/VS or shorted load), all four output stages provide overcurrent shutdown and overtemperature shutdown functionality.

Low−side Current Limitation and Overcurrent Shutdown

To minimize the power dissipation in case of current limitation, a peak value control principle (Figure 6) is integrated in each LS power stage. The current limitation level Ic can be programmed by SPI (Config.OCx). The high−side and low−side I_{SD} overcurrent levels are designed to track the programmed Ic level. When the current limit Ic is exceeded for a time tb, the affected low side stage is switched off, the corresponding high side stage is switched on for a fixed time ta, and the diagnostic register bit “CLIM” will be latched to indicate peak current limitation active. The status flag (Config.SFMODE = 1) is not set in this case.

If the overcurrent shutdown threshold I_{SD} is exceeded for t > tdfault during the blanking time tb (Figure 7), a short−to−VS condition is detected and the device transitions into the fault lockout state. All output transistors will be latched off, the status flag will be set and latched (Config.SFMODE = 1), and diagnostic register bits “Short circuit to V_S” will be latched to indicate the fault condition.

High−side Overcurrent Shutdown

Both HS transistors are protected against shorted outputs to GND by an individual overcurrent shutdown. The high−side and low−side I_{SD} overcurrent levels are designed to track the programmed Ic level. If the overcurrent shutdown threshold I_{SD} is exceeded for t > tdfault (Figure 7), a short−to−GND condition is detected and the device transitions into the fault lockout state. All output transistors will be latched off, the status flag will be set and latched (Config.SFMODE = 1), and diagnostic register bits “Short circuit to GND” will be latched to indicate the fault condition.

Shorted Load

In case of a shorted load, both active HS and LS stages indicate an overcurrent condition. (LS: current limitation level exceeded, HS: overcurrent shutdown threshold level exceeded). All output transistors will be latched off, the status flag will be set and latched (Config.SFMODE = 1), and diagnostic register bits “Short circuit overload” will be latched to indicate the fault condition.

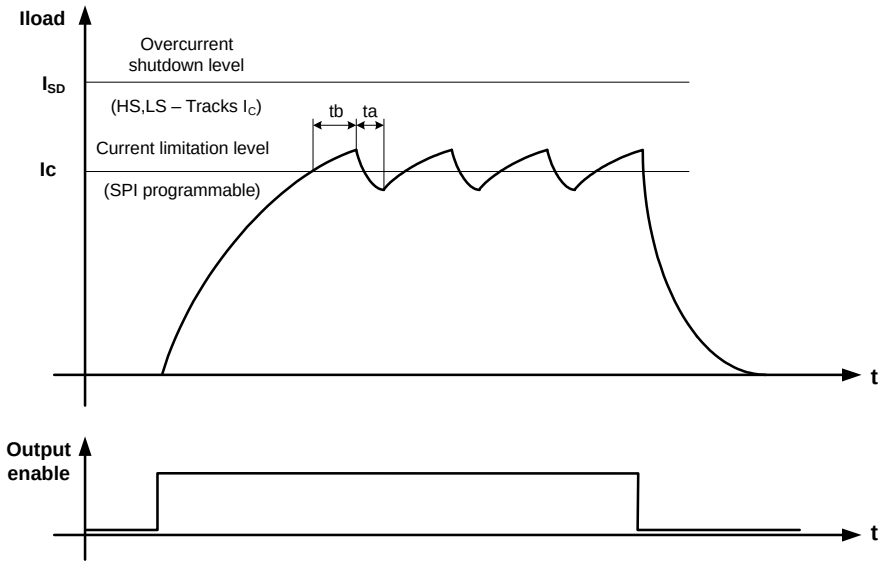


Figure 6. LS Peak Current Limitation

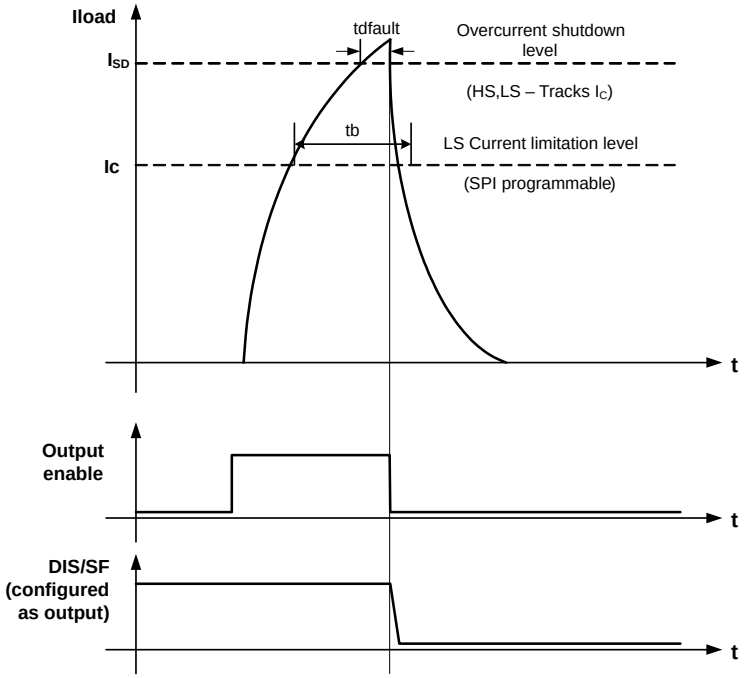


Figure 7. Overcurrent Shutdown (HS & LS)

Overtemperature

The device is protected against excessive junction temperatures by integrated temperature sensors. In case of exceeding the overtemperature shutdown point TSD (175°C min), all output transistors will be latched off, the status flag will be set and latched (Config.SFMODE = 1), and diagnostic register bit “OT” will be latched to indicate the fault condition.

Temperature−Dependent Peak Current Reduction

When the junction temperature is between TLIM (165°C typ.) and TSD, the programmed peak current is reduced as shown in Figure 8. The diagnostic register bit “CRED” will be latched to indicate peak current reduction active. The status flag (Config.SFMODE = 1) is not set in this case. The region of operation is indicated by RD_Config register bits “TH1”and “TH0”. THx bits are cleared by a rising edge on EN while DIS/SF = 0 or a falling edge on DIS/SF while EN = 1, or by reading the diagnostic register via the RD_Diag command.

Whenever the programmed I_C level is reduced in the region between TLIM and TSD, the reduced I_C level is latched. The high−side and low−side I_{SD} overcurrent levels are unaffected during temperature dependant current limit reduction. The originally programmed I_C level is restored by a rising edge on EN while DIS/SF = 0 or a falling edge on DIS/SF while EN = 1, or by reading the diagnostic register via the RD_Diag command.

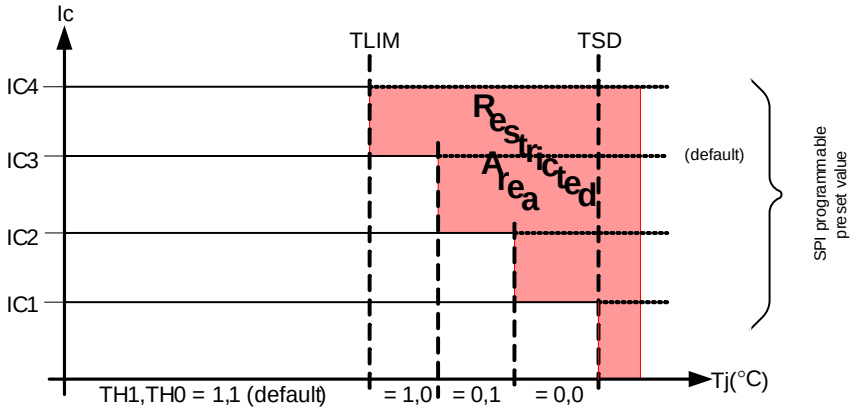


Figure 8. Temperature−dependent Peak Current Reduction

Open Load Diagnostics

While short to GND/VS or shorted load fault conditions at the outputs will be detected in active mode**,** open load detection is performed in off−mode. The open load diagnostic is activated by disabling the NCV7729's power stages via the enable inputs EN and DIS/SF (Config.SFMODE = 0). To allow a low−quiescent current mode, the diagnostic function can be deactivated via the SPI Config register (Config.ENx = 0). The device's operating modes invoked via the enable inputs and the Config.ENx register bits are detailed in Table 2.

Figure 9 shows the open load diagnostic scheme. The diagnostic is performed by applying two different currents to the outputs OUT1 and OUT2. The diagnostic result is determined by a simple comparison of both pin voltages to two separate reference voltages. The diagnostic results are shown in Table 3.

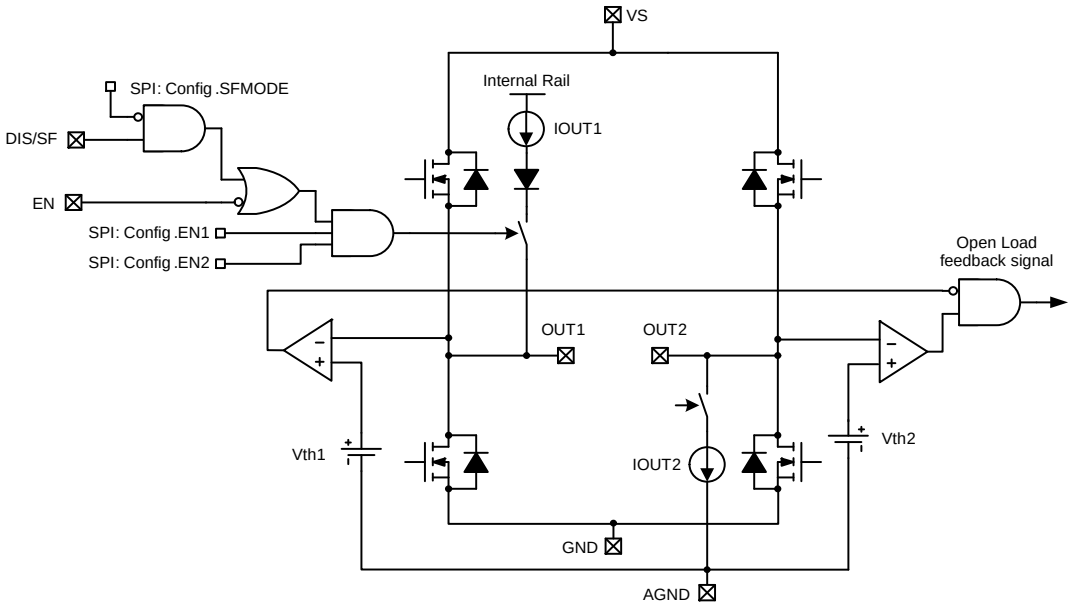


Figure 9. Open Load Detection

Table 2. NCV7729 OPERATING MODES

EN	DIS/SF	Config.EN1	Config.EN2	Operating Mode
0	X	0	X	Standby
0	X	X	0	Standby
0	X	1	1	Open Load Diagnosis
X	1	1	1	Open Load Diagnosis
1	0	0	0	Standby
1	0	1	1	Normal Operation (Outputs active)

Table 3. OPEN LOAD DIAGNOSTICS RESULTS

Failure Mechanism	V(OUT1)	V(OUT2)	Diagnostic Result
Load inserted	> Vth1	> Vth2	No fault
Open Load	> Vth1	< Vth2	Open load detected
OUT1: Short to GND AND Open Load	< Vth1	< Vth2	No Open load detected
OUT2: Short to GND AND Open Load	> Vth1	< Vth2	Open load detected
OUT1: Short to VS AND Open Load	> Vth1	< Vth2	Open load detected
OUT2: Short to VS AND Open Load	> Vth1	> Vth2	No Open load detected

Power Supplies

The device is powered by two supply voltages:

V_S: Battery voltage (analog and power stages supply voltage)

V_{CC}: Digital supply voltage

In order to provide the required gate−overdrive for the HS power transistors, a boost supply voltage is generated by the internal regulated chargepump. To ensure low−EMI operation the chargepump power is regulated to the actual drive current (deactivated in steady state operation). An external buffering cap (C_{BUF} in Figure 10) is used to provide high peak currents required for fast output switching.

The chargepump output current capability is sized to allow PWM operation up to 30 kHz. To optimize the device's EMI performance, the chargepump output power can be reduced via SPI bit Config.CHPmode. In case of low−power CHP mode, the maximum output PWM frequency is limited to 4 kHz. Any current limitation event automatically turns the chargepump into high power mode.

All three supply voltages (V_S, V_{CC} and CHP) are monitored for undervoltage. In case of any undervoltage event, the device's output stages are turned into Hi−Z mode. CHP and VS undervoltage events result in a non−latched output lockout and the output stages are automatically re−enabled after normal operating conditions are re−established.

A V_{CC} undervoltage event causes the device to transition into fault lockout state (see Figure 11). V_{CC} undervoltage is handled as a latched lockout condition, requiring re−enable of the device by appropriate transitions on the EN and DIS/SF (Config.SFMODE = 0) enable inputs. Diagnostic and status information is lost when V_{CC} undervoltage occurs and it is required to re−program the configuration register unless default settings are used.

V_S current can be reduced to a minimum in the low−quiescent current standby mode by setting EN = L, DIS/SF = H, and setting Config.EN[1,2] = 0,0. The load must be connected between OUT1 and OUT2 to achieve the low−quiescent current standby mode.

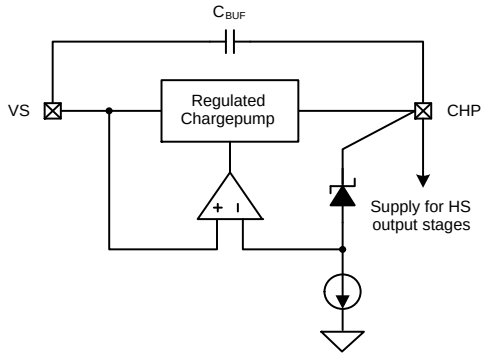


Figure 10. Regulated Charge Pump

Power Supply Failure

In the event of a voltage regulator failure (e.g. Figure 2 "REG 2"), the NCV7729 is designed to allow up to 18 V at the logic input/output pins (EN, DIS/SF, INx, CSB, SCLK, SI, SO). However, if the voltage applied to the device's V_{CC} pin (e.g. Figure 2 "REG 1") exceeds VCCOV (V_{CC} overvoltage event) the output stages are turned into Hi−Z mode and the V_{CC} pin is internally disconnected.

A V_{CC} overvoltage event causes the device to transition into fault lockout state similar to V_{CC} undervoltage. V_{CC}

overvoltage is handled as a latched lockout condition, requiring re−enable of the device by appropriate transitions on the EN and DIS/SF (Config.SFMODE = 0) enable inputs. Diagnostic and status information is lost when V_{CC} overvoltage occurs and it is required to re−program the configuration register unless default settings are used.

Loss of Ground Failure

Loss of ground failure is detected when a difference in potential (G_{DIF}) between the AGND and DGND pins exists. In the event of ground loss failure, the device transitions into fault lockout state and the output stages are turned into Hi−Z mode. Loss of ground is handled as a latched lockout condition. Diagnostic and status information is lost when loss of ground occurs.

Fault Handling

Fault handling states are shown in Figure 11. All overcurrent and overtemperature events cause a latched lockout of the output stages. V_{CC} under/over voltage faults or loss of AGND or DGND faults are handled as a latched lockout condition, requiring re−enable of the device. The device can be returned to normal operating mode by either a rising edge on EN while DIS/SF = 0, or a falling edge on DIS/SF while EN = 1. Undervoltage on V_S or CHP result in a non−latched lockout event (OUTx = Z until the supply voltage returns into operating range).

In status flag mode (Config.SFMODE = 1), DIS/SF will be set low when EN goes H→L and is reset when EN goes L→H. The status flag is set and latched when a fault condition is detected that causes transition to a latched lockout state. In the case of V_S or CHP undervoltage the status flag is set, but is reset when the supply voltage returns into operating range (see Table 1).

All fault conditions (except V_{CC} or loss of ground faults) that lead to a fault lockout state are stored in the diagnostic register in a latched manner. A fault lockout state also causes the configuration register “LOCK” bit to be set (RD_Config:b4 = 1). In the case of VS or CHP undervoltage the configuration “LOCK” bit is not set and diagnostic register data is not latched (see Note 18 on Page 21).

Diagnostic and configuration register data will persist until the microcontroller performs an action to reset the device or register. The device status can be read by accessing the diagnostic register via the RD_Diag or WR_Config SPI commands. The state of the “LOCK” bit can be accessed via the RD_Config command.

The diagnostic register can be reset by:

- A read access to the register via SPI command RD_Diag (reset occurs on the rising edge of CSB if valid SPI frame)
- A rising edge on EN while DIS/SF = 0 or a falling edge on DIS/SF while EN = 1
- VCC under/over voltage or loss of AGND or DGND

Accessing the diagnostic register via the WR_Config command or disabling the outputs via the Config.ENx bits does not reset the diagnostic register contents.

The configuration register “LOCK” bit can be reset by:

- A rising edge on EN while DIS/SF = 0 or a falling edge on DIS/SF while EN = 1
- VCC under/over voltage or loss of AGND or DGND

At power−up, default diagnostic register content is b[7:0] = 0xF0 and configuration register “LOCK” bit b4 = 1.

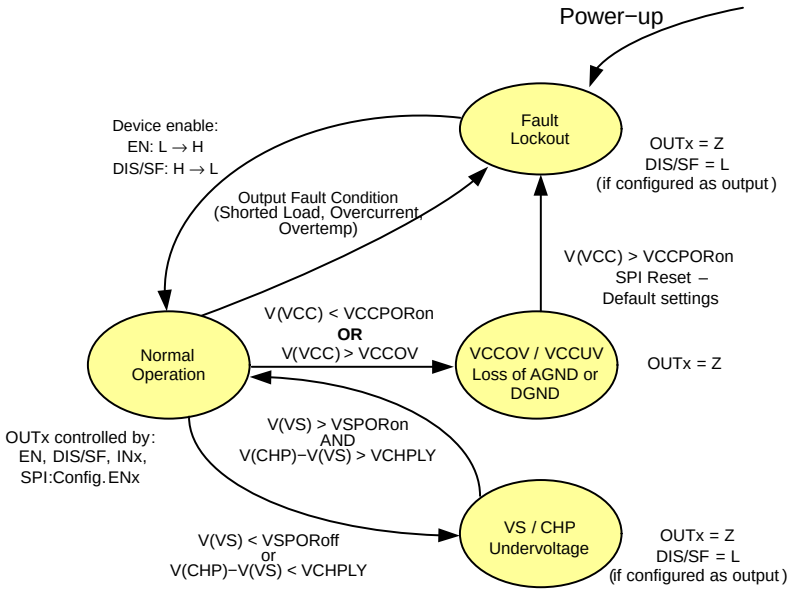


Figure 11. Fault Handling State Diagram

16−bit SPI Interface

The 4−wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7729 and the application's microcontroller. The NCV7729 always operates in slave mode whereas the controller provides the master function. The NCV7729 is accessed by the SPI master by applying an active−low slave select signal at CSB. SI is the data input, SO the data output. The SPI master provides the clock to the NCV7729 via the SCLK input. The data output SO is high impedance (tri−state) when CSB is high.

The uppermost two bits of the SI data frame are used as a chip ID to allow extended addressing. The chip ID is fixed to 00 for the NCV7729. To avoid a bus conflict, the SO output is held in tri−state until the ID bits have been successfully received and decoded. If the ID does not match the fixed NCV7729 ID, the entire frame is ignored and SO remains tri−state. The extended addressing feature therefore does not allow SPI daisy−chaining through the NCV7729.

SPI Frame Format

The general format of the NCV7729's SPI frame is shown in Figure 12. Both 16−bit input and 14−bit output data are MSB first. The device supports in−frame response to minimize the amount of CPU overhead for communication. The response data is transmitted within the same access cycle immediately after decoding the ID and command bits. Each SPI access is checked for consistency such that input data written to internal registers (a write access is executed) only when all of the following occur:

- Recognition of a valid chip ID
- A valid number of SCLK cycles (16)
- Recognition of a valid command

A transmission error is indicated by setting a flag bit (TF) in the case of an invalid number of SCLK cycles or receipt of an invalid command. The TF bit can be checked by the microcontroller in the verification response following the frame in which transmission error occurred. The TF bit is reset after receipt of the next valid frame. Data stored in the device's configuration and diagnostic registers is unaffected in the case of a transmission error.

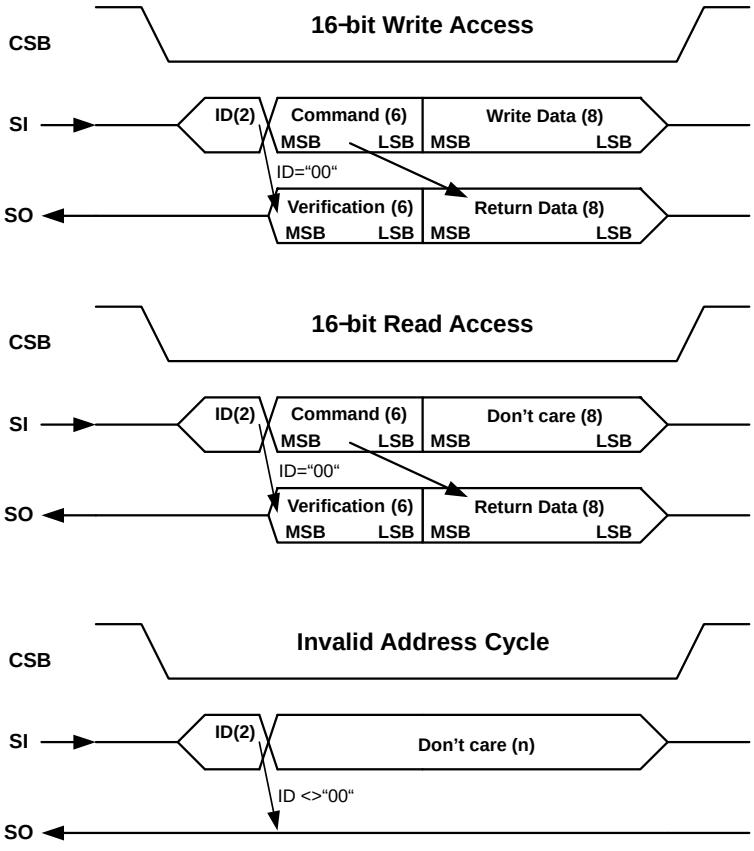


Figure 12. General 16−bit SPI frame format.

General SPI Timing

The general SPI timing shown in Figure 13 is defined as follows for the NCV7729:

- The change at output SO is forced by the rising edge of the SCLK signal if a valid chip ID is recognized; otherwise SO remains tri−state
- The SI input signal is latched on the falling edge of the SCLK signal
- The data received during a write access are written into the internal registers at the rising edge of the CSB signal only when all of the following occur:
  - A valid chip ID is recognized
  - Exactly 16 SCLK cycles were counted during CSB = low
  - A valid command is recognized

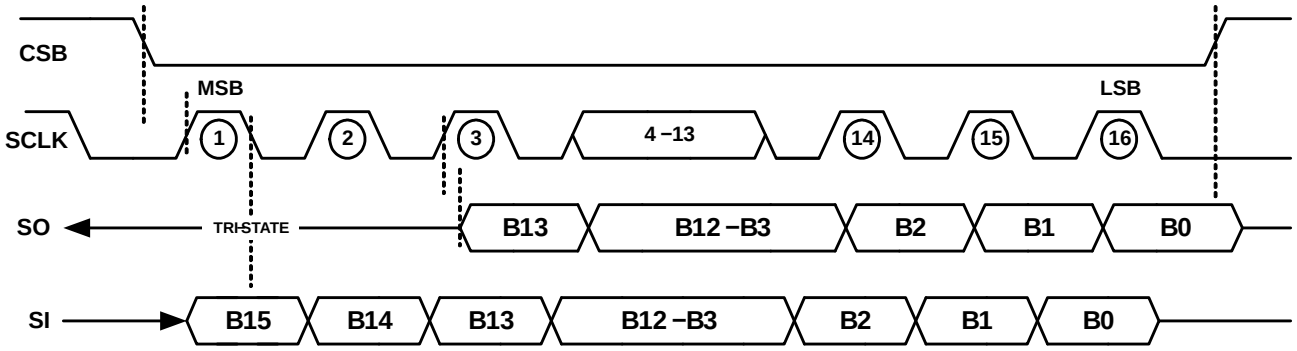


Figure 13. SPI Timing diagram

REGISTER AND COMMAND STRUCTURE OVERVIEW

PROTOTYPE	R/W		COMMAND													
IN	ID1	ID0	CD5	CD4	CD3	CD2	CD1	CD0	Data in [7:0]							
			VERIFICATION													
OUT	Z	Z	1	0	1	0	1	TF	Data out [7:0]							

BIT #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

WR_CONFIG	W		Advanced Feature Control													
IN	0	0	1	1	0	0	1	1	SF Mode	CHP Mode	EN2	EN1	OC1	OC0	b1	b0
OUT	Z	Z	1	0	1	0	1	TF	EN	OT	CRED	CLIM	D21	D20	D11	D10

RD_ID	R															
IN	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	ID[7:0]							

RD_REV	R															
IN	0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	SWR[3:0]				MSR[3:0]			

RD_CONFIG	R															
IN	0	0	1	0	1	0	0	0	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	SF Mode	CHP Mode	ENX	LOCK	OC1	OC0	TH1	TH0

RD_DIAG	R															
IN	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	EN	OT	CRED	CLIM	D21	D20	D11	D10

INVALID ID	–															
IN	< > “00”		X	X	X	X	X	X	X	X	X	X	X	X	X	X
OUT	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

INVALID CMD	–															
IN	0	0	UNDEFINED						X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	1	1	1	1	1	1	1	1

DETAILED COMMAND DESCRIPTION

WR_CONFIG

Type: W

Function: Programs the device configuration (valid SPI frame detected).

The WR_CONFIG returns the diagnostic register contents without resetting the register. The RD_DIAG command returns the diagnostic register contents and resets all latched data in the register.

The WR_CONFIG register can only be changed when EN = 0.

Command Prototype:

WR_CONFIG	W		Advanced Feature Control													
IN	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	SF MODE	CHP MODE	EN2	EN1	OC1	OC0	b1	b0
OUT	Z	Z	1	0	1	0	1	TF	EN	OT	CRED	CLIM	D21	D20	D11	D10

Input Parameter Description:

Parameter		Description	Remarks
b1	b0	Reserved	Future use
X	X		
OC1	OC0	OUTx LS Current Limit	
1	1	IC4	
1	0	IC3	Default
0	1	IC2	
0	0	IC1	
EN1		OUT1 Control	
0		Output 1 disabled	
1		Output 1 enabled	Default
EN2		OUT2 Control	
0		Output 2 disabled	
1		Output 2 enabled	Default
CHPMODE		Charge pump Mode	
0		Full power mode	Default
1		Reduced power mode	
SFMODE		DIS/SF Mode	
0		DIS/SF configured as enable input	Default
1		DIS/SF configured as status flag output	

Output Parameter Description:

Parameter				Description	Remarks
D21	D20	D11	D10	Priority encoded diagnostic data	(Note 18)
OUT2 Status		OUT1 Status			
1	1	0	0	Shorted Load	Data is latched
X	X	0	1	OUT1 short to V_S	Data is latched
X	X	1	0	OUT1 short to GND	Data is latched
X	X	1	1	OUT1 Normal	−
0	0	1	1	Open Load	Data is latched
0	1	X	X	OUT2 Short to VS	Data is latched
1	0	X	X	OUT2 Short to GND	Data is latched
1	1	X	X	OUT2 Normal	−
0	0	0	0	V_{CC} Power−on Reset	Data is latched
				V_S or CHP Undervoltage	Data is not latched
CLIM				OUTx LS Current Limit	
0				OUTx LS Current > ICx	Data is latched
1				Normal Operation	−
CRED				OUTx LS Current Limit Reduction	
0				T_J > TLIM	Data is latched
1				Normal Operation	−
OT				Overtemperature	
0				T_J > TSD	Data is latched
1				Normal operation	−
EN				Enable Status	(Note 19)
0				Outputs disabled	Data is not latched
1				Outputs enabled	−
TF				Transmission Error Flag	
0				Previous SPI Frame Valid	−
1				Transmission Error Detected	Data is latched
b[13:9]				Verification = “1 0 1 0 1”	Hard−coded

18. The D[21:20] and D[11:10] diagnostic data are stored according to the following priority scheme:

    Priority 1 (highest): VS or CHP undervoltage
    Priority 2: Shorted load
    Priority 3: Short to GND or VS
    Priority 4: Open load

    Lower priority faults are overwritten by higher priority faults in the case of multiple faults. In the case of V_S or CHP undervoltage, overwritten fault data are restored after V_S or CHP returns into normal operating range. Overwritten fault data can be retrieved via the WR_CONFIG command. Resetting the diagnostic register via the enable inputs or the RD_DIAG command resets all latched data and overwritten fault data cannot be retrieved. At VCC power−on reset D[21:10] = 0000.
19. The EN bit reflects the enabled/disabled state of the outputs based on the state of the EN or DIS/SF input pins or the state of the WR_CONFIG bits EN1or EN2.

RD_ID
Type: R
Function: Returns the hard−coded device identification (ID).

Command Prototype:

RD_ID	R															
IN	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	ID[7:0]							

Input parameter description:
n/a

Output Parameter Description:

Parameter	Description	Remarks
ID[7:0]	ID = “1 0 1 0 0 0 1 0”	Hard−coded
TF	Transmission Error Flag	
0	Previous SPI Frame Valid	–
1	Transmission Error Detected	Data is latched
b[13:9]	Verification = “1 0 1 0 1”	Hard−coded

RD_REV
Type: R
Function: Returns the hard−coded device revision counters.

Command Prototype:

RD_REV	R															
IN	0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	SWR[3:0]				MSR[3:0]			

Input Parameter Description:
n/a

Output Parameter Description:

Parameter	Description	Remarks
MSR[3:0]	MSR = “0 0 0 1”	Hard−coded
SWR[3:0]	SWR = “0 0 0 0”	Hard−coded
TF	Transmission Error Flag	
0	Previous SPI Frame Valid	–
1	Transmission Error Detected	Data is latched
b[13:9]	Verification = “1 0 1 0 1”	Hard−coded

RD_CONFIG
Type: R
Function: Returns the device configuration parameters.

Command Prototype:

RD_CONFIG	R															
IN	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	SF MODE	CHP MODE	ENX	LOCK	OC1	OC0	TH1	TH0

Input Parameter Description:
n/a

Output Parameter Description:

Parameter		Description	Remarks
TH1	TH0	State of Temperature−Dependent Current Limit	Data is latched
1	1	T_J < TLIM	Default
1	0	TLIM < T_J < TSD	See Figure 8
0	1	TLIM < T_J < TSD	
0	0	T_J > TSD	
OC1	OC0	OUTx LS Current Limit via WR_CONFIG OCx	
1	1	IC4	
1	0	IC3	Default
0	1	IC2	
0	0	IC1	
LOCK		Fault Lockout	Data is latched
0		Outputs enabled	
1		Output disabled	Default
ENX		Output Control via WR_CONFIG ENx	(Note 20)
0		OUTx disabled	
1		OUT1 AND OUT2 enabled	Default
CHPMODE		Charge pump Mode	
0		Full power mode	Default
1		Reduced power mode	
SFMODE		DIS/SF Mode	
0		DIS/SF configured as enable input	Default
1		DIS/SF configured as status flag output	
TF		Transmission Error Flag	
0		Previous SPI Frame Valid	−
1		Transmission Error Detected	Data is latched
b[13:9]		Verification = “1 0 1 0 1”	Hard−coded

20. The ENX bit reflects the enabled/disabled state of the outputs based on the state of the WR_CONFIG bits EN1or EN2.

RD_DIAG
Type: R
Function: Returns the diagnostic register contents and resets the register (valid SPI frame detected).
The RD_DIAG command returns the diagnostic register contents and resets all latched data in the register. The WR_CONFIG command can be used to return the diagnostic register contents without resetting the register.

Command Prototype:

RD_DIAG	R															
IN	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X
OUT	Z	Z	1	0	1	0	1	TF	EN	OT	CRED	CLIM	D21	D20	D11	D10

Input Parameter Description:
n/a

Output Parameter Description:

Parameter				Description	Remarks
D21	D20	D11	D10	Priority encoded diagnostic data	(Note 18)
OUT2 Status		OUT1 Status			
1	1	0	0	Shorted Load	Data is latched
X	X	0	1	OUT1 short to V_S	Data is latched
X	X	1	0	OUT1 short to GND	Data is latched
X	X	1	1	OUT1 Normal	−
0	0	1	1	Open Load	Data is latched
0	1	X	X	OUT2 Short to V_S	Data is latched
1	0	X	X	OUT2 Short to GND	Data is latched
1	1	X	X	OUT2 Normal	−
0	0	0	0	V_{CC} Power−on Reset	Data is latched
				V_S or CHP Undervoltage	Data is not latched
CLIM				OUTx LS Current Limit	
0				OUTx LS Current > ICx	Data is latched
1				Normal Operation	−
CRED				OUTx LS Current Limit Reduction	
0				T_J > TLIM	Data is latched
1				Normal Operation	−
OT				Overtemperature	
0				T_J > TSD	Data is latched
1				Normal operation	−
EN				Enable Status	Note 18
0				Outputs disabled	Data is not latched
1				Outputs enabled	−
TF				Transmission Error Flag	
0				Previous SPI Frame Valid	−
1				Transmission Error Detected	Data is latched
b[13:9]				Verification = “1 0 1 0 1”	Hard−coded

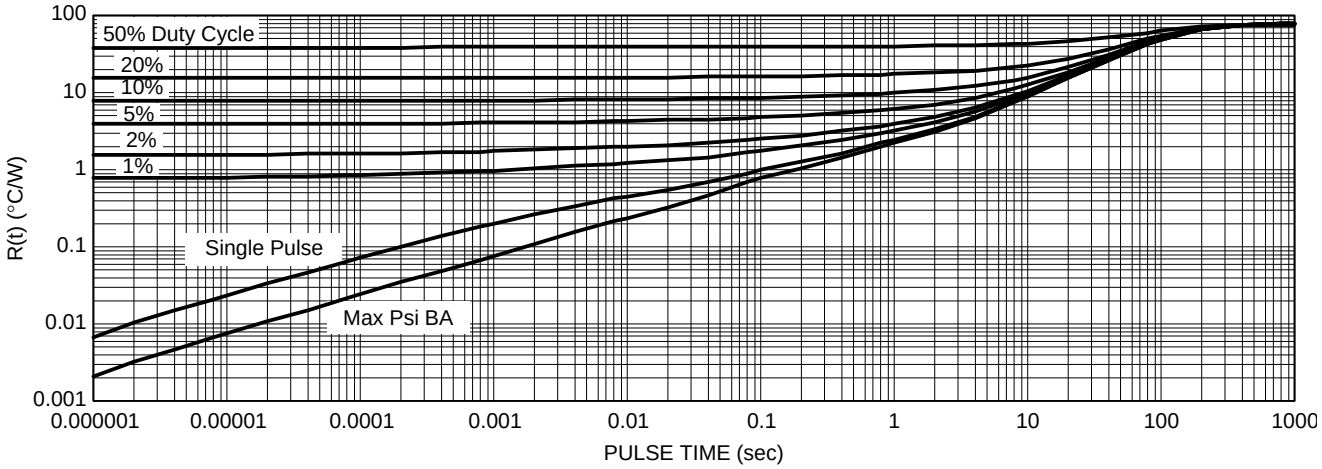


Figure 14. Transient Thermal Performance on 100 mm^2 2 oz. Heat Spreader

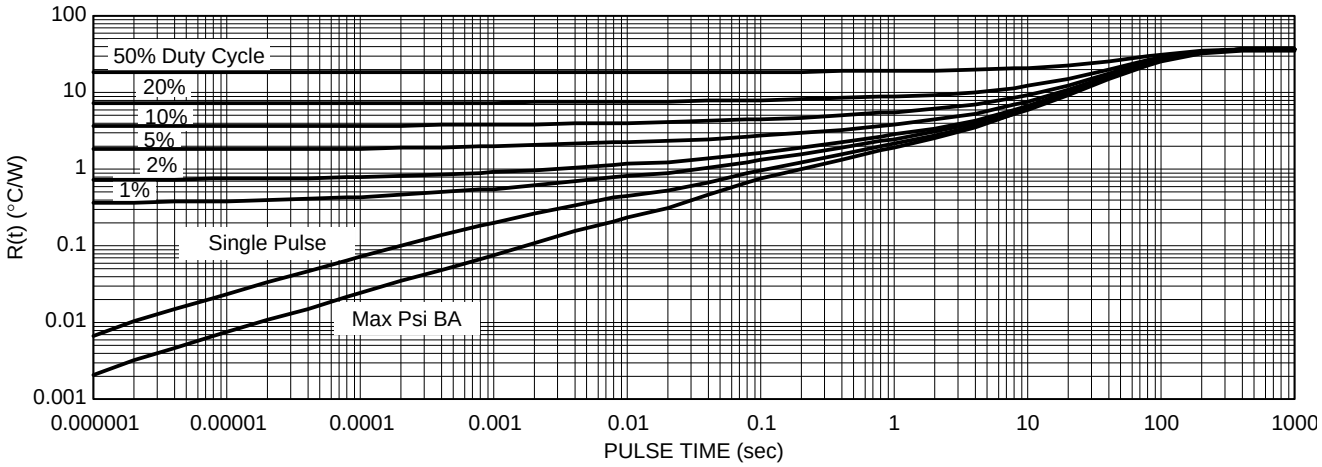


Figure 15. Transient Thermal Performance on 600 mm^2 2 oz. Heat Spreader

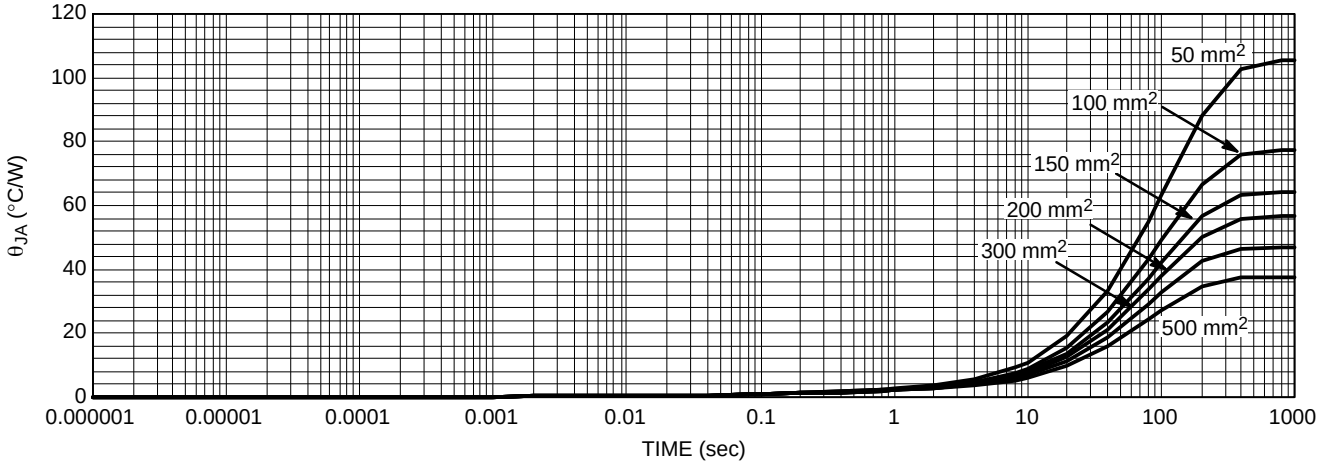
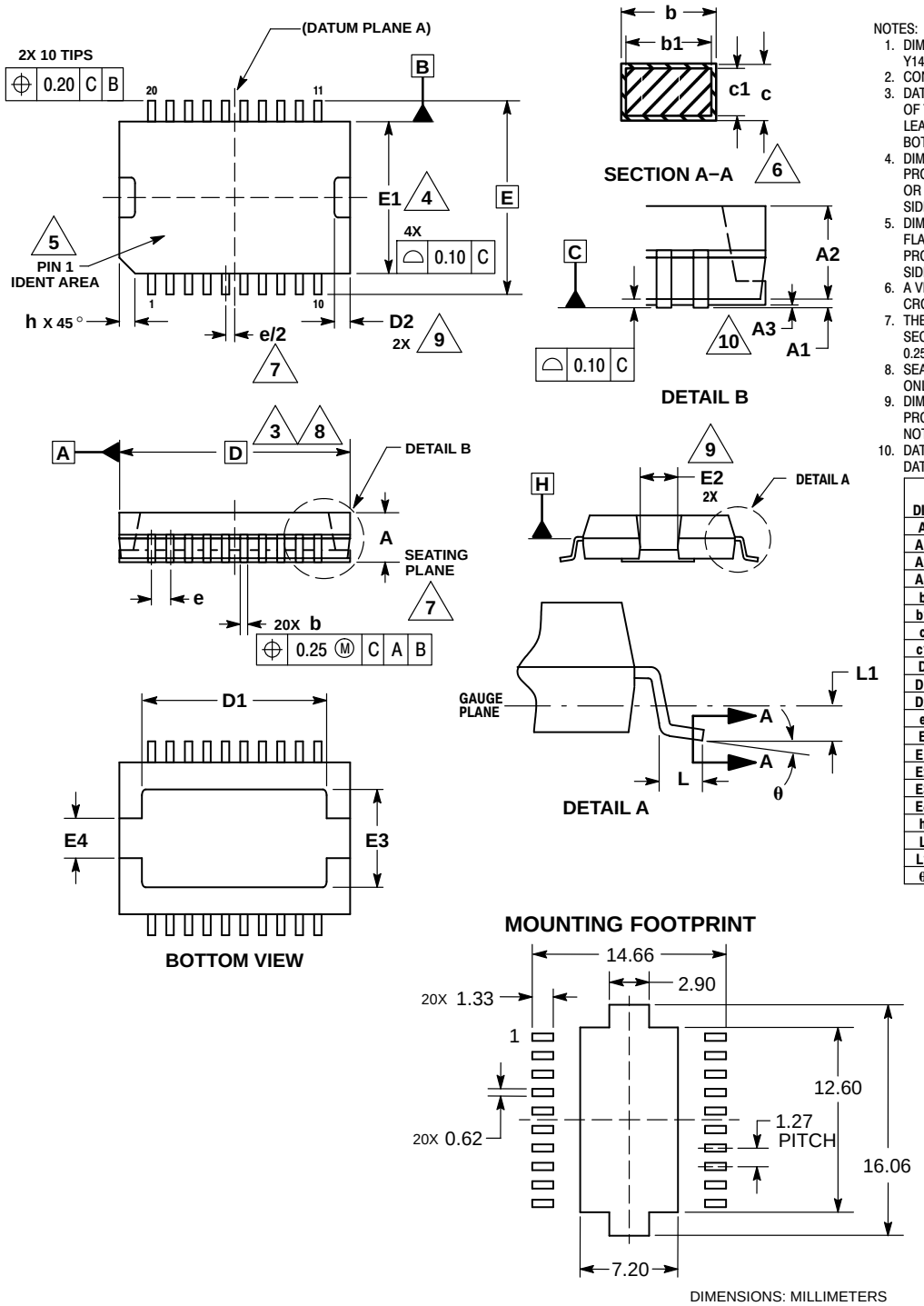


Figure 16. Transient Thermal Performance on Various 2 oz. Heat Spreaders

PACKAGE DIMENSIONS

PSOP−20
CASE 525AB
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE LEAD AND IS COINCIDENT WITH THE LEAD WHERE IT EXITS THE BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH PROTRUSION. INTERLEAD FLASH PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. E1 IS DETERMINED AT DATUM H.
6. A VISUAL IDENTIFIER IS LOCATED WITHIN THE CROSS−HATCHED AREA.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM THE TIP.
8. SEATING PLANE IS DEFINED BY THE LEAD TIPS ONLY.
9. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. TIEBAR PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.
10. DATUMS A AND B TO BE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00	3.40
A1	0.10	0.30
A2	2.90	3.10
A3	0.00	0.10
b	0.40	0.52
b1	0.40	0.49
c	0.23	0.32
c1	0.23	0.28
D	15.90 BSC	
D1	11.70	12.60
D2	0.90	1.10
e	1.27 BSC	
E	13.95	14.45
E1	11.00 BSC	
E2	2.50	2.70
E3	6.40	7.20
E4	2.70	2.90
h	---	1.10
L	0.84	1.10
L1	0.35 BSC	
θ	0°	8°

MOUNTING FOOTPRINT

DIMENSIONS: MILLIMETERS

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