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Kind regards,

Team Nexperia

# BUK7226-75A

## N-channel TrenchMOS standard level FET

Rev. 02 — 22 February 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP General Purpose Automotive (GPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features

- 175 °C rated
- Q101 compliant
- Low on-state resistance
- Standard level compatible

### 1.3 Applications

- 12 V, 24 V and 42 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

### 1.4 Quick reference data

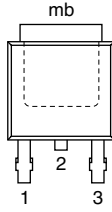
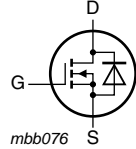
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	75	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a> and <a href="#">4</a>	[1]	-	45	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	158	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 12</a> and <a href="#">13</a>	-	22	26	mΩ
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 45\text{ A}; V_{sup} \leq 75\text{ V};$ $R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$ $T_{j(init)} = 25\text{ °C};$ unclamped inductive load	-	-	215	mJ

[1] Capped at 45 A due to bondwire.

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT428 (DPAK)**

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7226-75A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

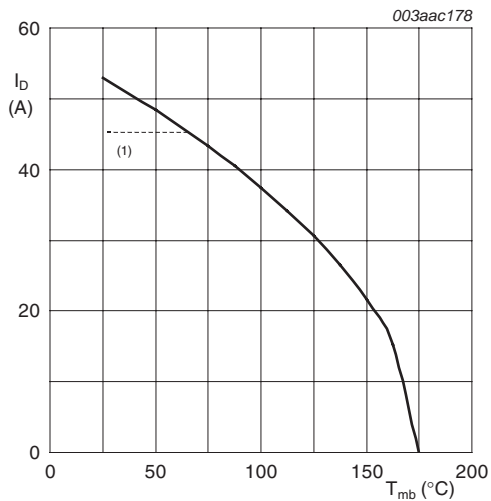
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	75	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	75	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	[1]	45	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	38	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 4</a>	-	215	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	158	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 45\text{ A}; V_{sup} \leq 75\text{ V}; R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}$ ; unclamped inductive load	-	215	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	[2][3] [4]	-	J
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	45	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	215	A

[1] Capped at 45 A due to bondwire.

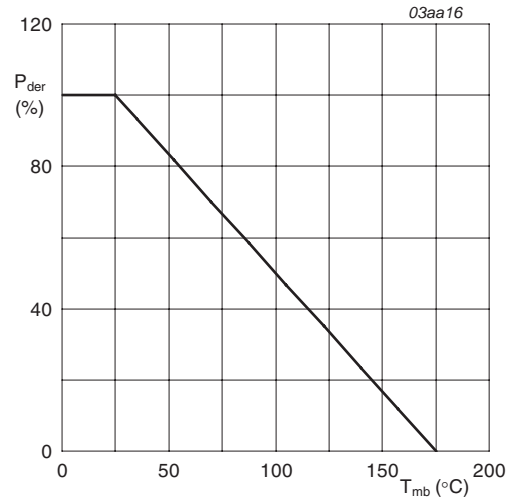
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Repetitive avalanche rating limited by an average junction temperature of 170 °C.
- [4] Refer to application note AN10273 for further information.



$V_{GS} \geq 10 V$

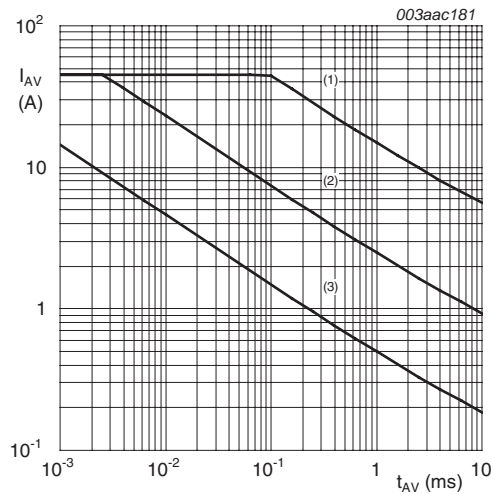
(1) Capped at 45 A due to bondwire.

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

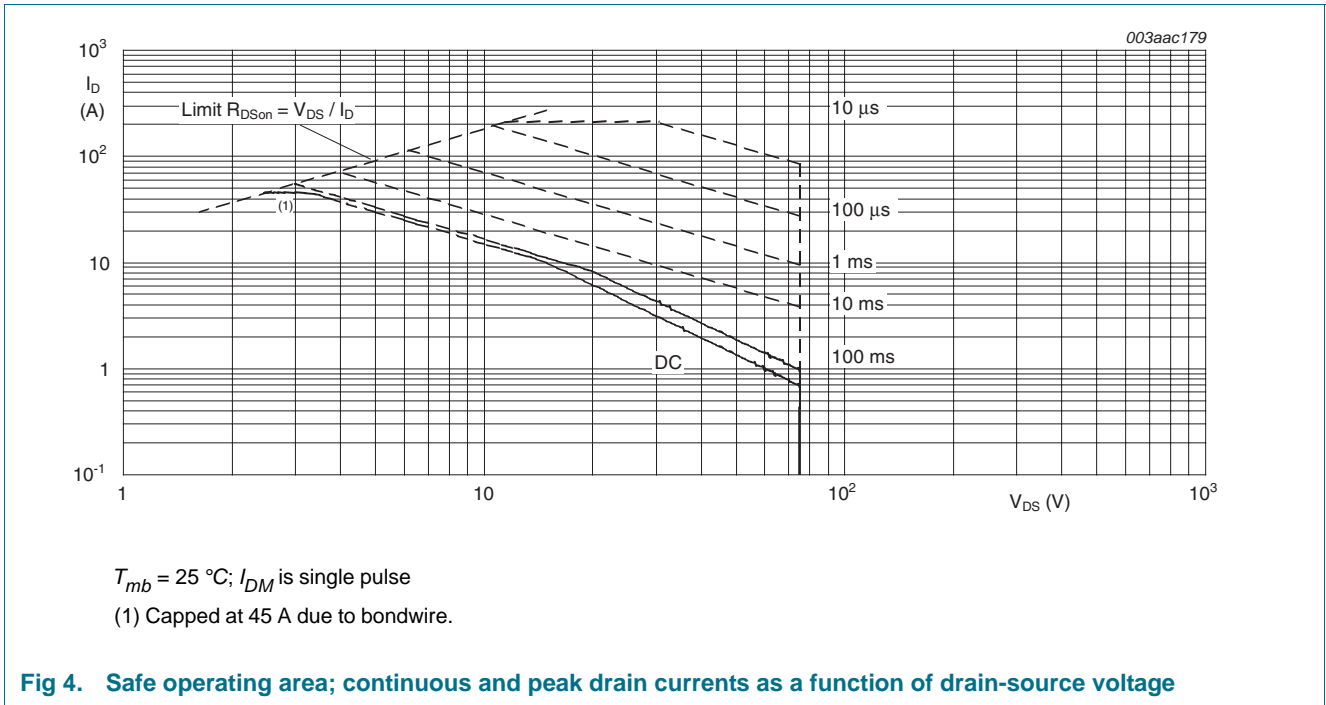


(1) Single-pulse;  $T_j = 25 \text{ }^\circ\text{C}$ .

(2) Single-pulse;  $T_j = 150 \text{ }^\circ\text{C}$ .

(3) Repetitive.

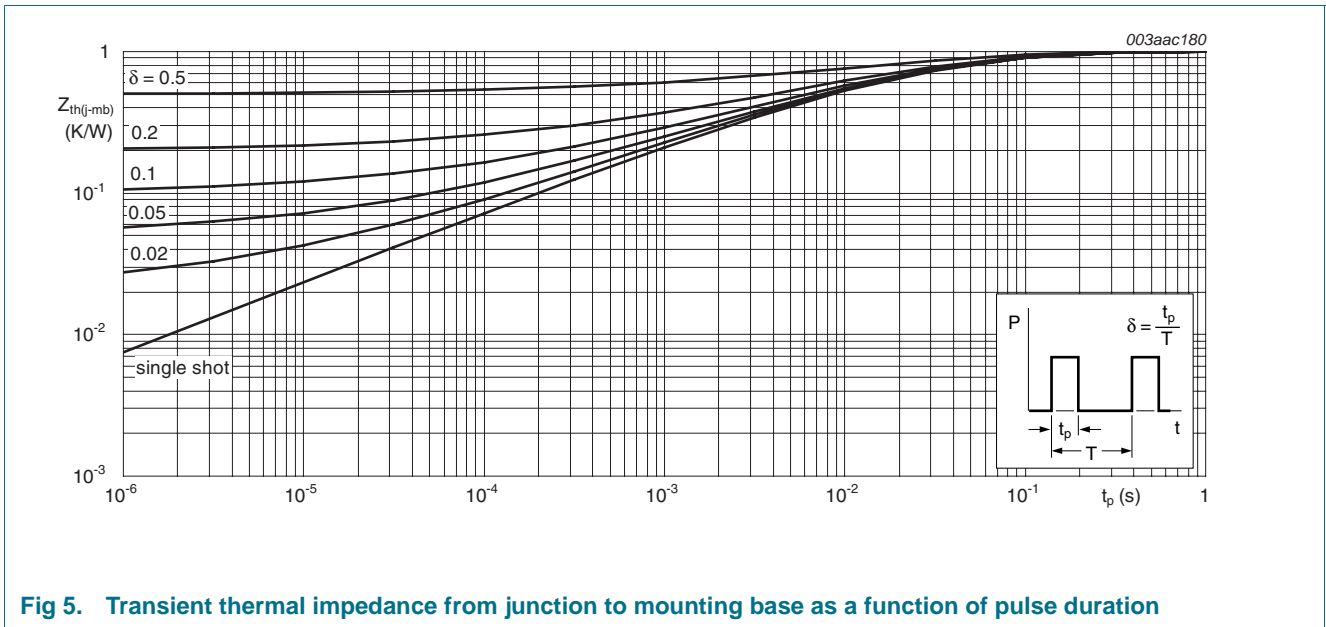
**Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**



## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	70	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	-	1	K/W



**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

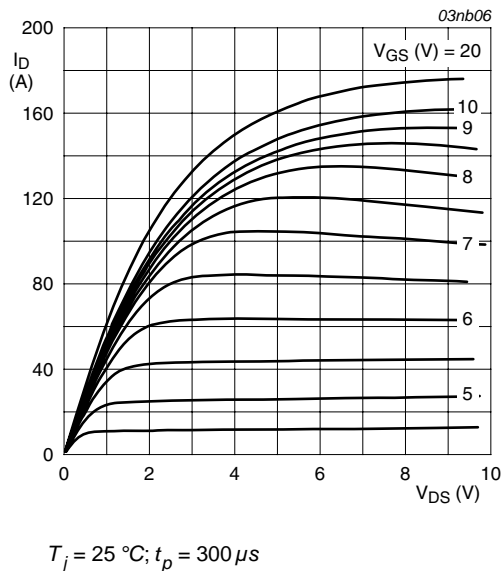
## 6. Characteristics

**Table 6. Characteristics**

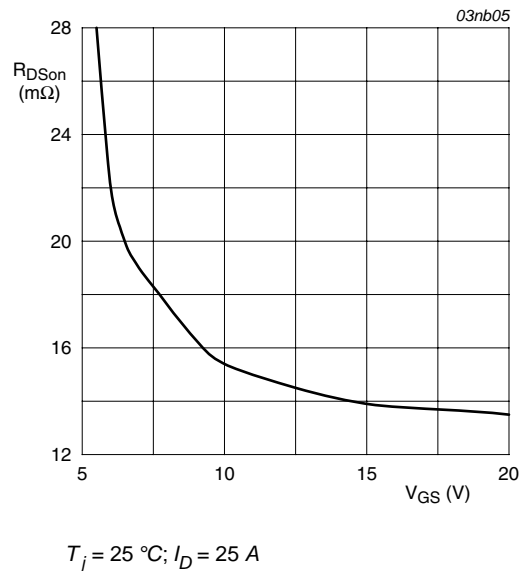
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	70	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> and <a href="#">13</a>	-	-	54	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> and <a href="#">13</a>	-	22	26	m $\Omega$
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	0.85	1.2	V

**Table 6. Characteristics ...continued**

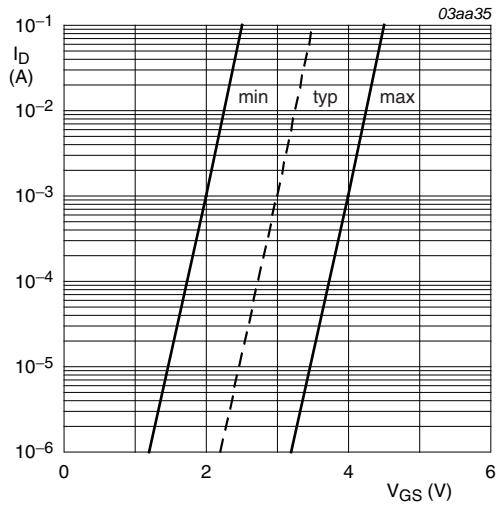
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	53	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	144	-	nC
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 60\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 14</a>	-	48	-	nC
$Q_{GS}$	gate-source charge		-	7.5	-	nC
$Q_{GD}$	gate-drain charge		-	17	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ;	-	1789	2385	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	382	458	pF
$C_{rss}$	reverse transfer capacitance		-	219	300	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\ \Omega$ ;	-	14	-	ns
$t_r$	rise time	$V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 10\ \Omega$ ; $T_j = 25\text{ }^\circ\text{C}$	-	66	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	61	-	ns
$t_f$	fall time		-	41	-	ns
$L_D$	internal drain inductance	measured from drain lead from package to center of die; $T_j = 25\text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	measured from source lead from package to source bond pad; $T_j = 25\text{ }^\circ\text{C}$	-	7.5	-	nH



**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**

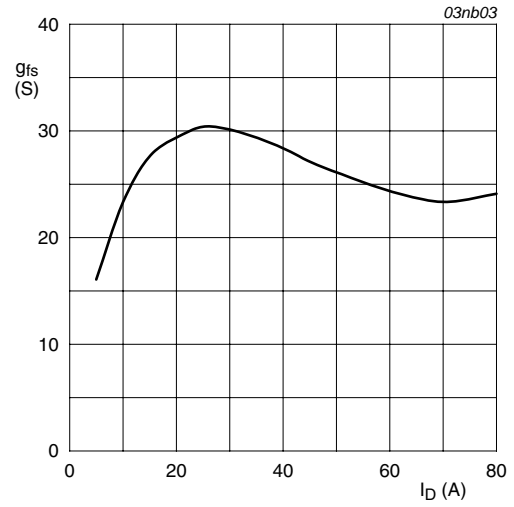


**Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



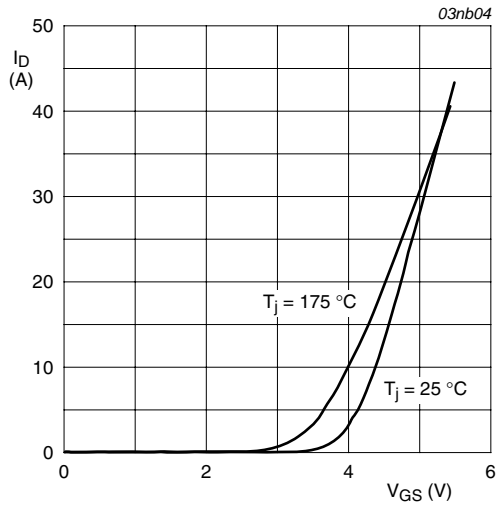
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



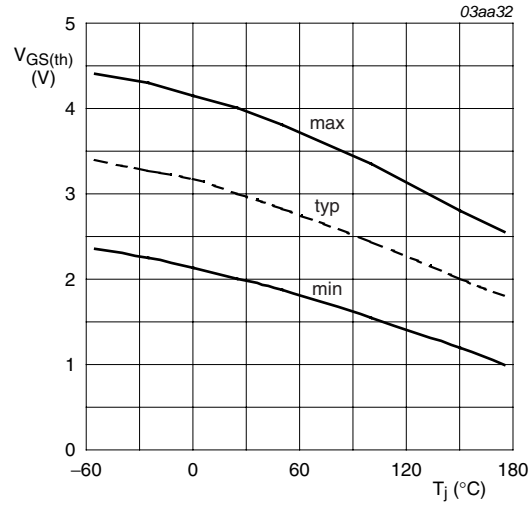
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 9. Forward transconductance as a function of drain current; typical values**



$V_{DS} = 25\text{ V}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



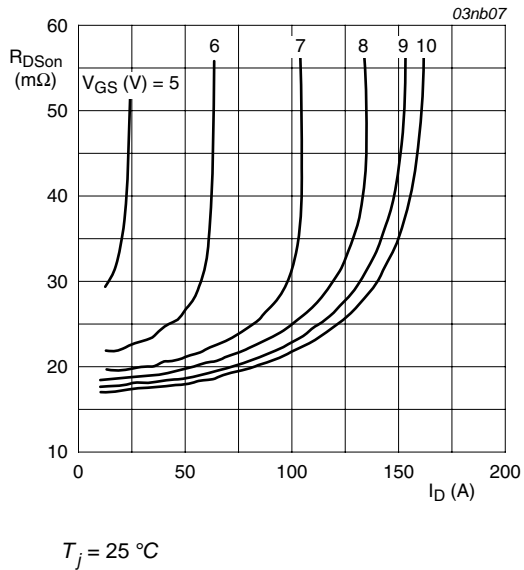


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

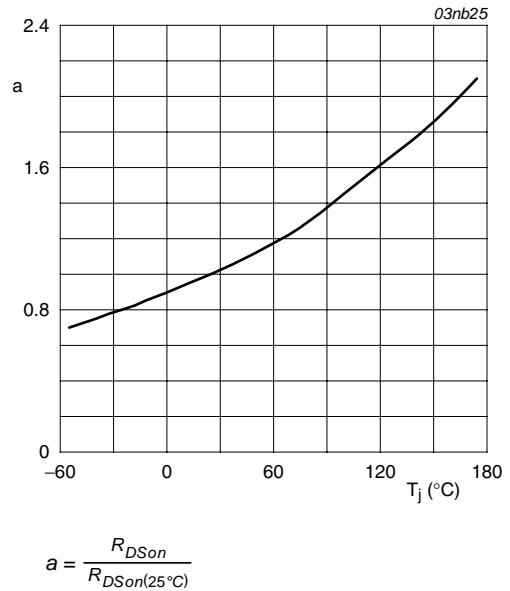


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

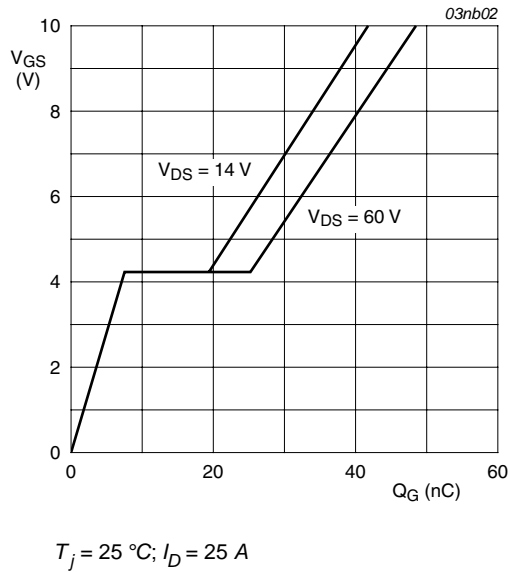


Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values

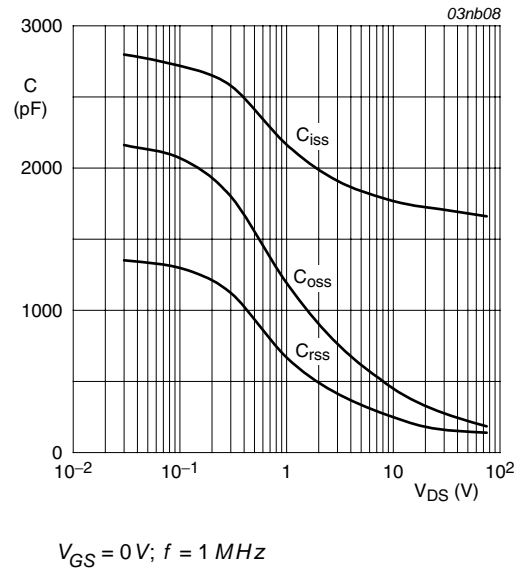


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

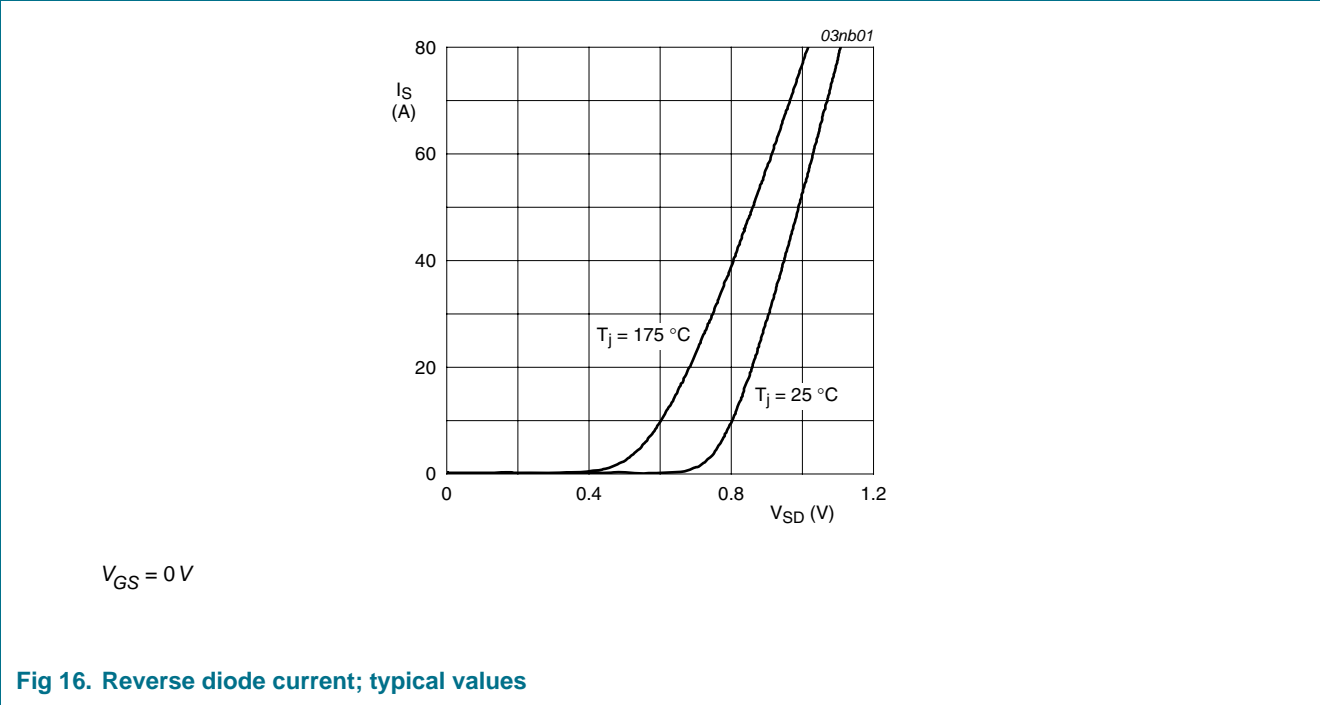


Fig 16. Reverse diode current; typical values

**7. Package outline**

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

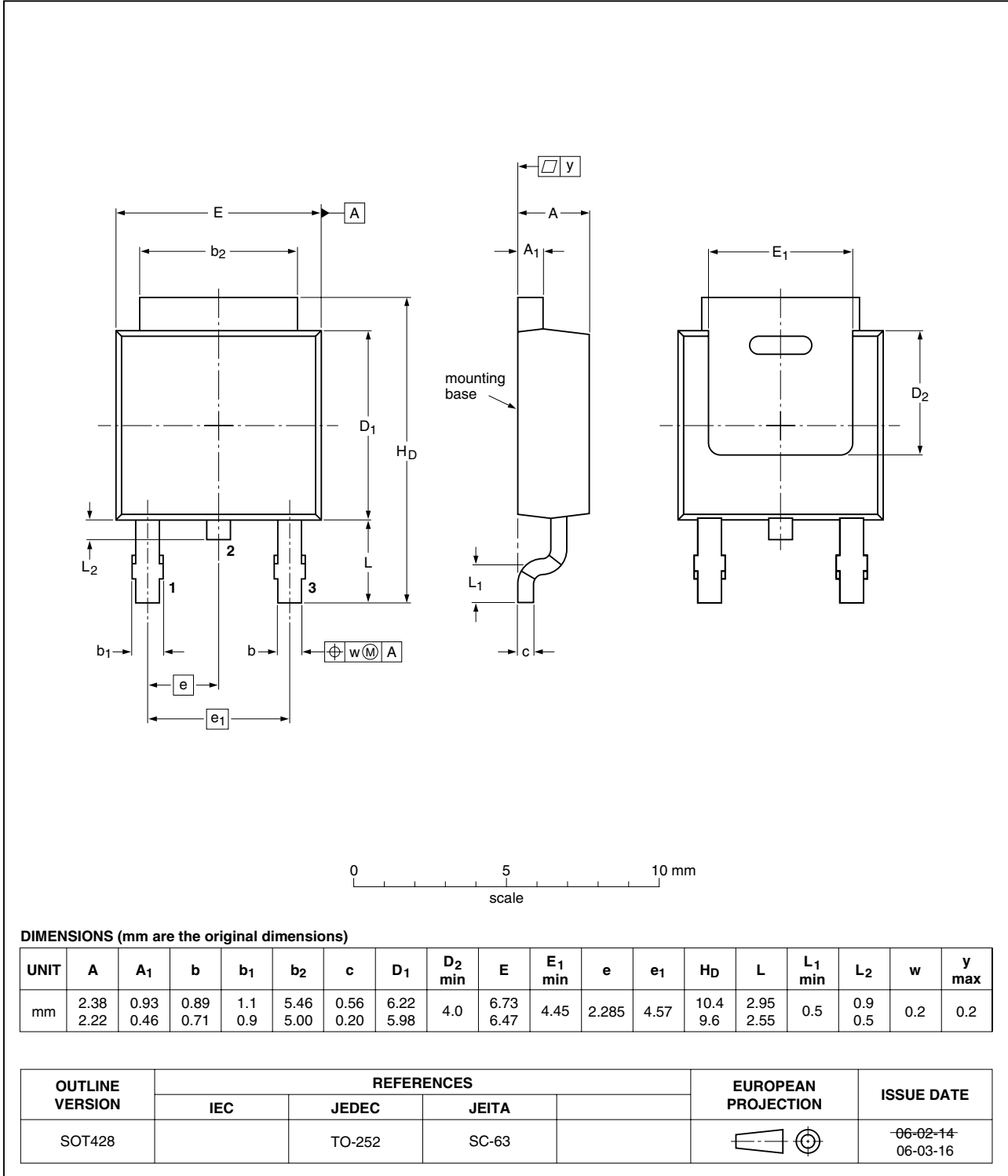


Fig 17. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7226-75A_2	20080222	Product data sheet	-	BUK7226_75A-01
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>
BUK7226_75A-01	20001009	Product specification; initial version		-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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