Clock Distribution Fanout Buffers

A family of 28 buffers offers six fanout combinations, supports clock rates up to 750 MHz, and a wide range of input and output clock signals making it ideal to use across multiple applications with minimal design efforts.

Internal input termination eliminates the need for external termination and biasing components. In addition, the ultra low-additive jitter and highly effective power supply noise filtering leaves the majority of the jitter budget to the clock source.

The clock buffers devices are synergistic with Microsemi® industry-leading timing portfolio and, when used together, these devices provide customer improved board performance and complete timing solutions.

28 Part Family

3X3mm   5X5mm   5X5mm
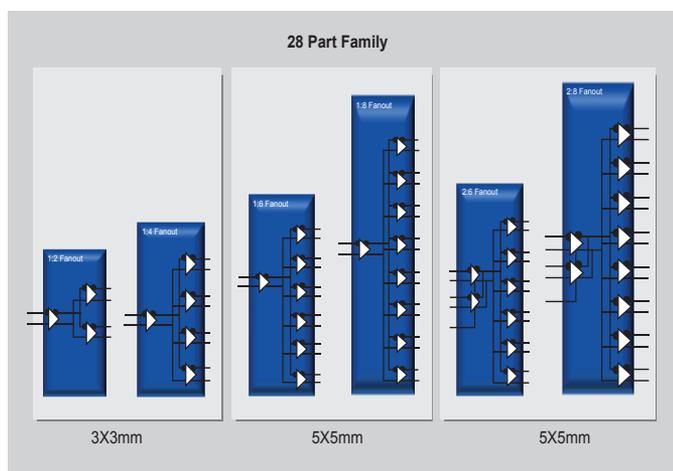
Available and Support

Clock Distribution Clock Buffers are in volume production. To learn more about Microsemi new clock buffers visit www.microsemi.com/timing-and-synchronization/clock-fan-out-buffers. Full information, including complete data sheets and design manuals, is available to registered Microsemi customers. To register for a Microsemi account, visit www.microsemi.com/create-an-account.

Key Features

Clock Rates up to 750 MHz

Inputs

- LVPECL, LVDS, CML, HCSL or LVCMOS
- Devices with internal or external input termination available

Outputs

- LVPECL or LVDS

Ultra-Low Additive Jitter

- As low as 39 fs RMS

Power Supply Noise

- As low as 48 fs RMS

Key Benefits

Preserve Signal Integrity

- Offer industry leading additive jitter and best power supply noise rejection (PSNR) performance

Ease Board Design

- Provide a flexible I/O structure; accept different types of input signals and produce different types of output signals
- Eliminate the need for external circuitry at the inputs with on-chip internal input terminations

Building Block of a Complete Timing Solution

- Clock buffers are highly synergistic with Microsemi industry-leading timing portfolio and offer tested interoperability and optimized performance

Preserve Signal Integrity, Ease Board Design With Microsemi Clock Distribution Fanout Buffers

Today's modern systems often require the distribution of several clock frequencies to multiple loads. Clock buffers complement clock synthesis devices by providing additional fanout capability as needed.

The ability to create multiple copies of a clock signal and distribute them among several loads with minimal additive jitter is a key advantage of a strong clock management solution. Jitter budget is mostly dedicated to the clock source and very little is left for clock management. Microsemi high performance buffers add minimal jitter combined with industry leading power supply noise filtering. This results in reduced system cost and easier design.

This family of buffers has a flexible I/O structure where inputs

are compatible with LVPECL, LVDS, CML, HCSL, LVCMOS, HSTL and SSTL, and outputs support LVPECL and LVDS signals.

Buffers with internal termination reduce the need for external components to save board cost and complexity. Buffers without internal termination support the use of precision external termination components and additional termination methods.

The family offers six fanout combinations—1:2, 1:4, 1:6, 1:8, 2:6, and 2:8—all available with internal or external input termination and LVDS or LVPECL outputs. These options provide the ideal devices for meeting application needs and easing component sourcing requirements.

Output Type	Input Termination	1:2	1:4	1:6	1:8	2:6	2:8	2:8
						Glitch-Free Switching		Simple Switching
		QFN-16 3x3mm	QFN-16 3x3mm	QFN-32 5x5mm	QFN-32 5x5mm	QFN-32 5x5mm	QFN-32 5x5mm	QFN-32 5x5mm
LVPECL	External	ZL40200	ZL40202	ZL40204	ZL40206	ZL40208	ZL40210	ZL40224
	Internal	ZL40201	ZL40203	ZL40205	ZL40207	ZL40209	ZL40211	ZL40225
LVDS	External	ZL40212	ZL40214	ZL40216	ZL40218	ZL40220	ZL40222	ZL40226
	Internal	ZL40213	ZL40215	ZL40217	ZL40219	ZL40221	ZL40223	ZL40227

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