LTC3636/LTC3636-1

Dual Channel 6A, 20V Monolithic Synchronous Step-Down Regulator

FEATURES

- **Wide V_{IN} Range: 3.1V to 20V**
- **Wide V_{OUT} Range:**
    0.6V to 5V (LTC3636)
    1.8V to 12V (LTC3636-1)
- **Output Current per Channel: 6A**
- **High Efficiency: Up to 95%**
- **Die Temperature Monitor**
- **Adjustable Switching Frequency: 500kHz to 4MHz**
- **External Frequency Synchronization**
- **Current Mode Operation for Excellent Line and Load Transient Response**
- 0.6V Reference Allows Low Output Voltages
- User Selectable Burst Mode® Operation or Forced Continuous Operation
- Output Voltage Tracking and Soft-Start Capability
- Short-Circuit Protected
- Overvoltage Input and Overtemperature Protection
- Power Good Status Outputs
- Low Profile 4mm × 5mm 28-Lead QFN Package

APPLICATIONS

- Distributed Power Systems
- Battery-Powered Instruments
- Point-of-Load Power Supplies

DESCRIPTION

The LTC®3636/LTC3636-1 is a high efficiency, dual-channel monolithic synchronous buck regulator using a controlled on-time current mode architecture, with phase lockable switching frequency. The operating supply voltage range is from 3.1V to 20V, making it suitable for lithium-ion battery stacks as well as point of load power supply applications from a 12V or 5V input.

The operating frequency is programmable from 500kHz to 4MHz with an external resistor and may be synchronized to an external clock signal. The high frequency capability allows the use of small surface mount inductors and capacitors. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that operate at high frequency while demanding fast transient response.

The LTC3636/LTC3636-1 can select between forced continuous mode and high efficiency Burst Mode operation. The LTC3636 and LTC3636-1 differ in their output voltage sense range.

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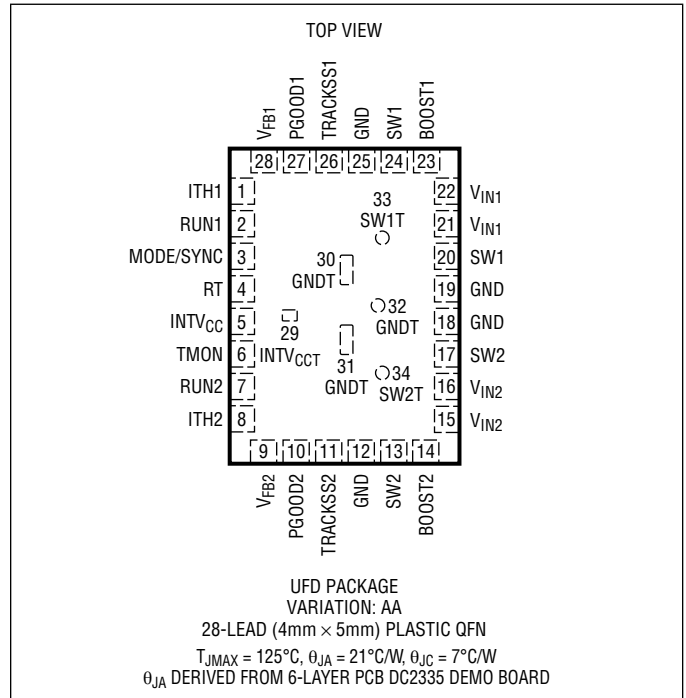
TYPICAL APPLICATION

Efficiency vs Load Current
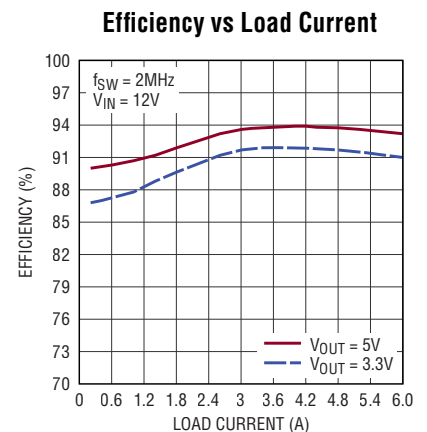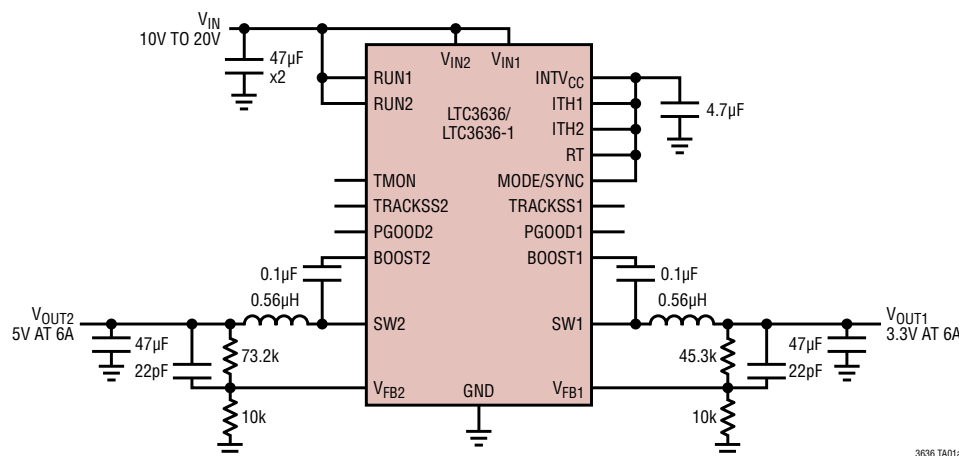
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2} .... −0.3V to 22V
PGOOD1, PGOOD2.................................... −0.3V to 22V
BOOST1-SW1, BOOST2-SW2 .... −0.3V to 3.6V
TRACKSS1, TRACKSS2 .... −0.3V to 3.6V
ITH1, ITH2, RT, MODE/SYNC........−0.3V to $INTV_{CC}$ + 0.3V
V_{FB1}, V_{FB2}, TMON. ....−0.3V to $INTV_{CC}$ + 0.3V
RUN1, RUN2.. −0.3V to 22V
Operating Junction Temperature Range
(Notes 3, 4).. −40°C to 125°C
Storage Temperature Range..................−65°C to 150°C

PIN CONFIGURATION

TOP VIEW

ITH1 1
RUN1 2
MODE/SYNC 3
RT 4
$INTV_{CC}$ 5
TMON 6
RUN2 7
ITH2 8

22 V_{IN1}
21 V_{IN1}
20 SW1
19 GND
18 GND
17 SW2
16 V_{IN2}
15 V_{IN2}

28 V_{FB1}
27 PGOOD1
26 TRACKSS1
25 GND
24 SW1
23 BOOST1

9 V_{FB2}
10 PGOOD2
11 TRACKSS2
12 GND
13 SW2
14 BOOST2

33 SW1T
30 GNDT
32 GNDT
29 $INTV_{CCT}$
31 GNDT
34 SW2T

UFD PACKAGE
VARIATION: AA
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 21°C/W, θ_{JC} = 7°C/W
θ_{JA} DERIVED FROM 6-LAYER PCB DC2335 DEMO BOARD

ORDER INFORMATION

http://www.linear.com/product/LTC3636#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3636IUFD#PBF	LTC3636IUFD#TRPBF	3636	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C
LTC3636EUFD#PBF	LTC3636EUFD#TRPBF	3636	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C
LTC3636IUFD-1#PBF	LTC3636IUFD-1#TRPBF	36361	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C
LTC3636EUFD-1#PBF	LTC3636EUFD-1#TRPBF	36361	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Selection Table

PART NUMBER	V_{OUT} SENSE RANGE
LTC3636	0.6V to 5V
LTC3636-1	1.8V to 12V

3636fb

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_J = 25°C$ (Note 2). $V_{IN1} = V_{IN2} = 12V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}	Supply Range		●	3.1		20	V
	V_{IN1} Supply Range		●	3.1		20	V
	V_{IN2} Supply Range	$3.1V < V_{IN1} < 20V$	●	1.5		20	V
	Output Voltage Range (Note 4)	LTC3636		0.6		5	V
		LTC3636-1		1.8		12	V
I_Q	Input DC Supply Current ($V_{IN1} + V_{IN2}$) Both Channels Active (Note 5)	MODE = 0V			1.3		mA
	Sleep Current	MODE = $INTV_{CC}$, V_{FB1}, $V_{FB2} > 0.6$			600		µA
	Shutdown	RUN1 = RUN2 = 0V			13		µA
V_{FB}	Feedback Reference Voltage		●	0.594	0.6	0.606	V
ΔV_{LINE_REG}	Reference Voltage Line Regulation	V_{IN} = 3.1V to 20V			0.002		%/V
ΔV_{LOAD_REG}	Output Voltage Load Regulation	ITH = 0.8V to 1.6V			0.05		%
I_{FB}	Feedback Pin Input Current					±30	nA
$g_{m(EA)}$	Error Amplifier Transconductance	ITH = 1.2V			1.8		mS
t_{ON}	Minimum On Time	LTC3636			30	35	ns
		LTC3636-1			30		
t_{OFF}	Minimum Off Time				100		ns
f_{OSC}	Oscillator Frequency	$V_{RT} = INTV_{CC}$		1.4	2	2.6	MHz
		RT = 162k		1.7	2	2.3	MHz
		RT = 80.6k		3.4	4	4.6	MHz
I_{LIM}	Valley Switch Current Limit	ITH = 1.8V		6	6.6	7.2	A
	Negative Valley Switch Current Limit				−4.2		A
$R_{DS(ON)}$	Top Switch On-Resistance				32		mΩ
	Bottom Switch On-Resistance				18		mΩ
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 20V, V_{RUN} = 0V			0.01	±1	µA
	Internal Temperature Monitor	$T_A = 25°C$			1.5		V
	Internal Temperature Monitor Slope (Note 6)				200		°C/V
V_{VIN-OV}	V_{IN} Overvoltage Lockout Threshold	V_{IN} Rising			22.5		V
		V_{IN} Falling		20.3	21.5	22.5	V
	$INTV_{CC}$ Voltage	$3.6V < V_{IN} < 20V$, 0mA Load		3.1	3.3	3.5	V
	$INTV_{CC}$ Load Regulation	0mA to 50mA Load, V_{IN} = 4V to 20V			1.3		%
	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising, $V_{IN} = INTV_{CC}$			2.7	2.9	V
		$INTV_{CC}$ Falling, $V_{IN} = INTV_{CC}$			2.55		V
	RUN Threshold Rising		●	1.16	1.22	1.28	V
	RUN Threshold Falling		●	0.96	1.01	1.06	V
	RUN Leakage Current				0	±3	µA
	PGOOD Good-to-Bad Threshold	V_{FB} Rising			8	10	%
		V_{FB} Falling			−8	−10	%
	PGOOD Bad-to-Good Threshold	V_{FB} Rising		−3	−5		%
		V_{FB} Falling		3	5		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_J = 25°C$ (Note 2). $V_{IN1} = V_{IN2} = 12V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			25		Ω
t_{PGOOD}	Power Good Filter Time			20	40		µs
t_{SS}	Internal Soft-Start Time	10% to 90% Rise Time			1000	1500	µs
	V_{FB} During Tracking	TRACKSS = 0.3V		0.28	0.3	0.315	V
$I_{TRACKSS}$	TRACKSS Pull-Up Current				1.4		µA
$V_{MODE/SYNC}$	MODE/SYNC Threshold Voltage	MODE V_{IH} MODE V_{IL}		1		0.4	V V
	SYNC Threshold Voltage	SYNC V_{IH}		0.95			V
I_{MODE}	MODE/SYNC Input Current	MODE = 0V MODE = $INTV_{CC}$			1.5 −1.5		µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3636 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3636E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the −40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3636I is guaranteed over the −40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and

power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \cdot \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Output voltages outside the specified range are not optimized for controlled on-time operation. Refer to the Applications Information section for further discussions related to the output voltage range.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.
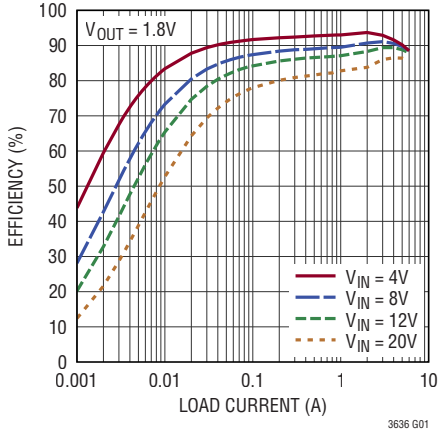
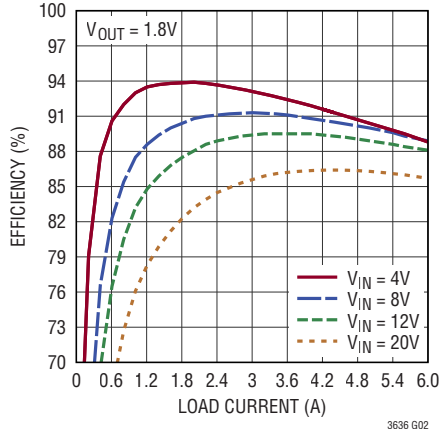**Note 6:** Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_J = 25°C$, $V_{IN1} = V_{IN2} = 12V$, $f_{SW} = 1MHz$, $L = 0.55μH$ unless otherwise noted.

Efficiency vs Load Current Burst Mode Operation

$V_{OUT} = 1.8V$

- V_IN = 4V
- V_IN = 8V
- V_IN = 12V
- V_IN = 20V

LOAD CURRENT (A)

EFFICIENCY (%)

3636 G01

Efficiency vs Load Current Forced Continuous Mode Operation

$V_{OUT} = 1.8V$

- V_IN = 4V
- V_IN = 8V
- V_IN = 12V
- V_IN = 20V

LOAD CURRENT (A)

EFFICIENCY (%)

3636 G02

Efficiency vs Load Current

Burst Mode OPERATION

FORCED CONTINUOUS MODE

L = 1µH

- V_OUT = 5V
- V_OUT = 3.3V
- V_OUT = 5V
- V_OUT = 3.3V

LOAD CURRENT (A)

EFFICIENCY (%)

3636 G03

Efficiency vs Load Current Burst Mode Operation

$V_{OUT} = 1.2V$

- V_IN = 4V
- V_IN = 8V
- V_IN = 12V
- V_IN = 15V
- V_IN = 20V

LOAD CURRENT (A)

EFFICIENCY (%)

3636 G04
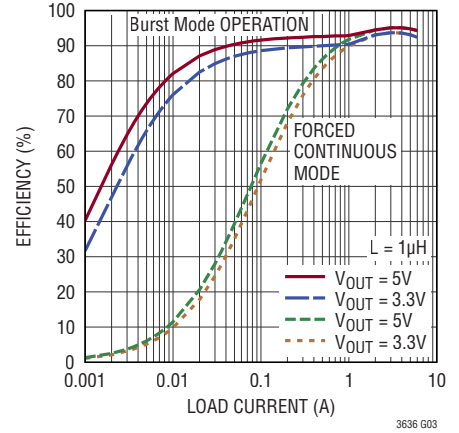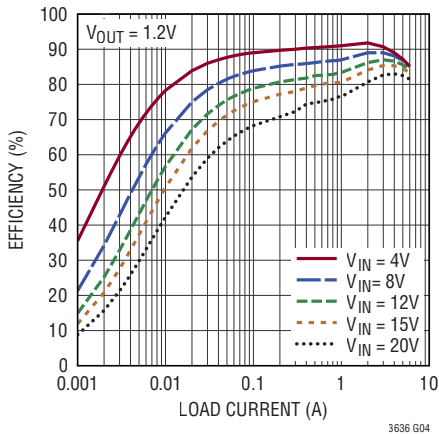
Efficiency vs Input Voltage Burst Mode Operation

$V_{OUT} = 1.8V$

- I_LOAD = 10mA
- I_LOAD = 100mA
- I_LOAD = 1A
- I_LOAD = 6A

INPUT VOLTAGE (V)

EFFICIENCY (%)

3636 G05
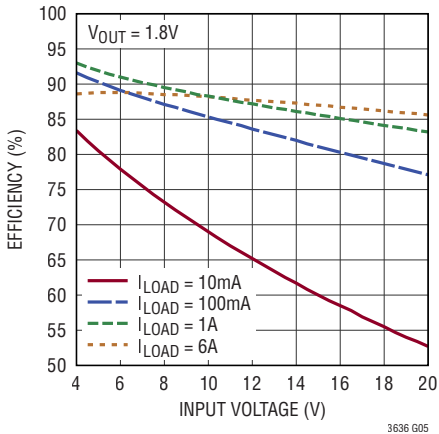
Reference Voltage vs Temperature

TEMPERATURE (°C)

REFERENCE VOLTAGE (V)

3636 G06

Load Regulation

$V_{OUT} = 1.8V$

- Burst Mode OPERATION
- FORCED CONTINUOUS

I_LOAD (A)

ΔV_OUT/V_OUT (%)

237820 G07

Oscillator Frequency vs Temperature

R_T = 324k

TEMPERATURE (°C)

FREQUENCY VARIATION (%)

3636 G08
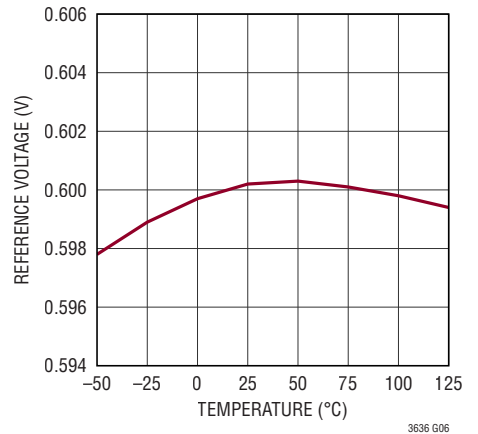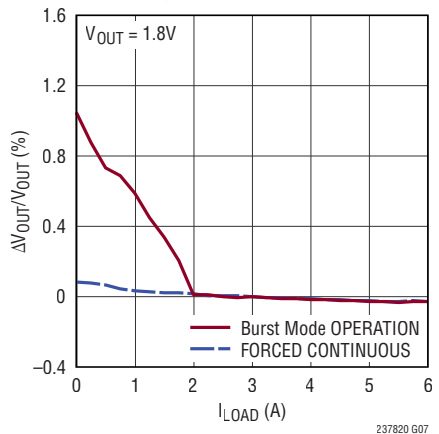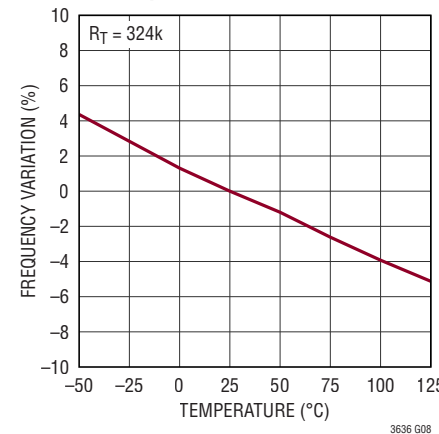
Oscillator Internal Set Frequency vs Temperature

R_T = INTV_CC

TEMPERATURE (°C)

FREQUENCY (MHz)

3636 G09

3636fb

TYPICAL PERFORMANCE CHARACTERISTICS

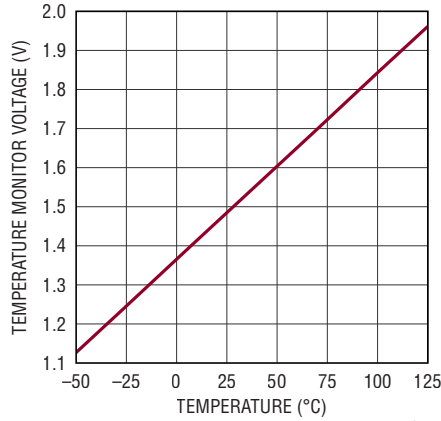$T_J = 25°C$, $V_{IN1} = V_{IN2} = 12V$, $f_{SW} = 1MHz$, $L = 0.55µH$ unless otherwise noted.

Internal MOSFET $R_{DS(ON)}$ vs Temperature
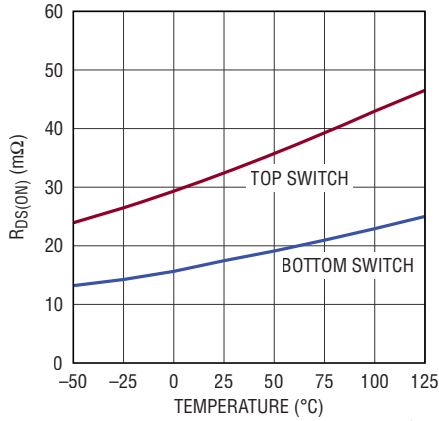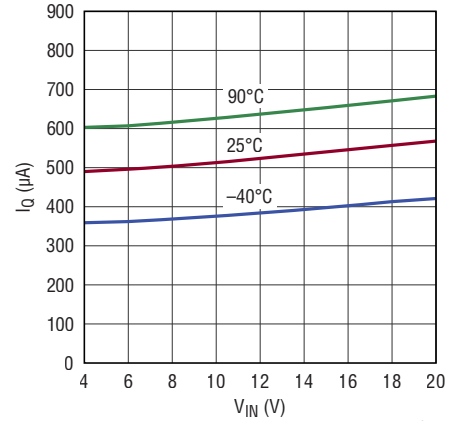

3636 G10

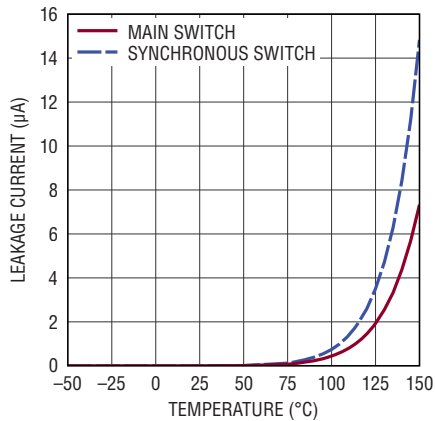### Temperature Monitor vs Temperature

3636 G11

Quiescent Current vs V_{IN} Burst Mode Operation
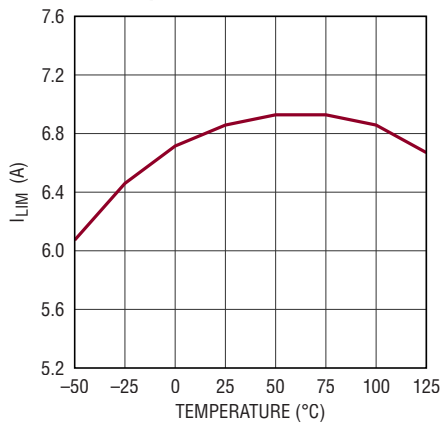

3636 G12

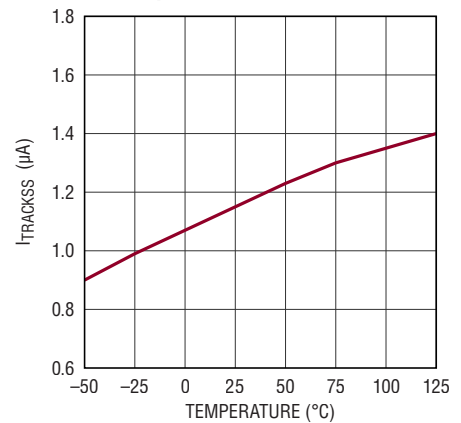### Switch Leakage vs Temperature
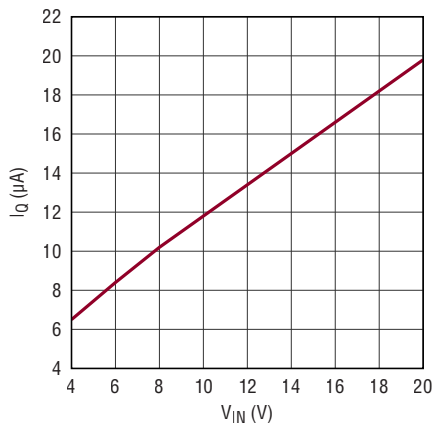

3636 G13

Valley Current Limit vs Temperature
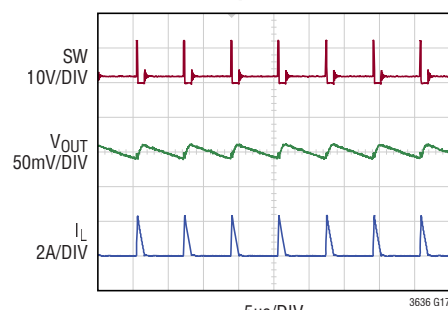

3636 G14

TRACKSS Pull-Up Current vs Temperature

3636 G15

Shutdown Current vs V_{IN}

3636 G16

Burst Mode Operation
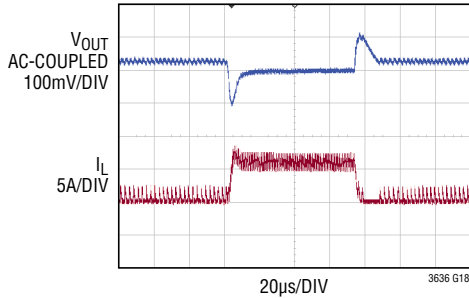

3636 G17

$V_{OUT} = 1.8V$
$I_{LOAD} = 200mA$

3636fb

6

TYPICAL PERFORMANCE CHARACTERISTICS

$T_J = 25°C$, $V_{IN1} = V_{IN2} = 12V$, $f_{SW} = 1MHz$, $L = 0.55\mu H$ unless otherwise noted.

Load Step

V_OUT AC-COUPLED 100mV/DIV
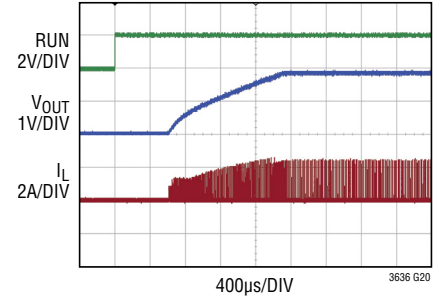
I_L 5A/DIV

20µs/DIV

3636 G18

$V_{OUT} = 1.8V$
$I_{LOAD} = 400mA$ to $6A$
$C_{COMP} = 330pF$
$R_{COMP} = 13k\Omega$
$C_F = 33pF$
$C_{OUT} = 47\mu F \times 2$

Load Step (Internal Compensation)

V_OUT AC-COUPLED 100mV/DIV

I_L 5A/DIV

20µs/DIV

3636 G19
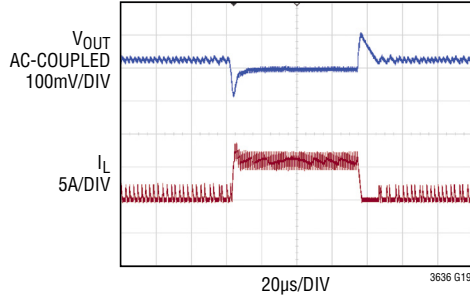
$V_{OUT} = 1.8V$
$I_{LOAD} = 400mA$ to $6A$
$ITH = INTV_{CC}$
$C_F = 33pF$
$C_{OUT} = 47\mu F \times 2$

Start-Up (Burst Mode Operation)

RUN 2V/DIV

V_OUT 1V/DIV

I_L 2A/DIV

400µs/DIV

3636 G20

$V_{OUT} = 1.8V$
$I_{LOAD} = 100mA$

Start-Up (Forced Continuous Mode)

RUN 2V/DIV

V_OUT 1V/DIV

I_L 2A/DIV

400µs/DIV

3636 G21
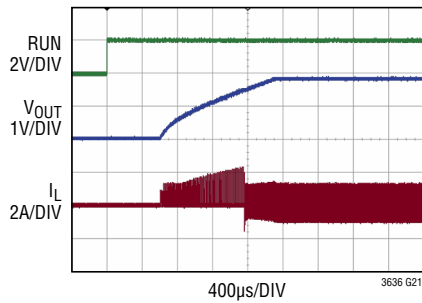
$V_{OUT} = 1.8V$
$I_{LOAD} = 100mA$

Start-Up into Prebiased Output (Burst Mode Operation)

RUN 2V/DIV

V_OUT = 1.8V 1V/DIV

I_L 2A/DIV

400µs/DIV

3636 G22
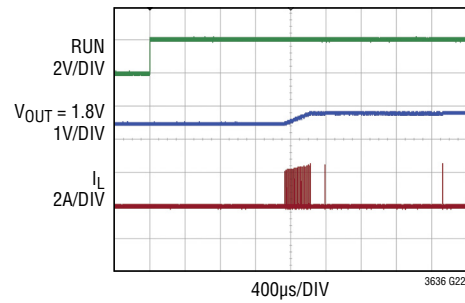
$I_{LOAD} = 0mA$

Start-Up into Prebiased Output (Forced Continuous Mode)

RUN 2V/DIV

V_OUT = 1.8V 1V/DIV

I_L 5A/DIV

400µs/DIV

3636 G23
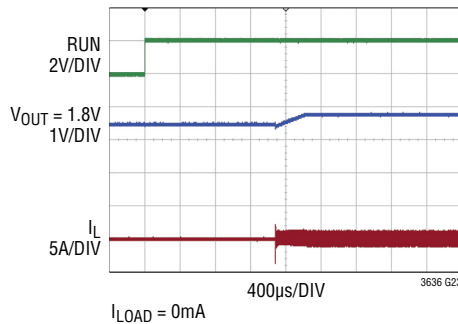
$I_{LOAD} = 0mA$

Short-Circuit and Soft-Start

I_L 10A/DIV

V_IN 5V/DIV

V_OUT 1V/DIV

200µs/DIV

3636 G24
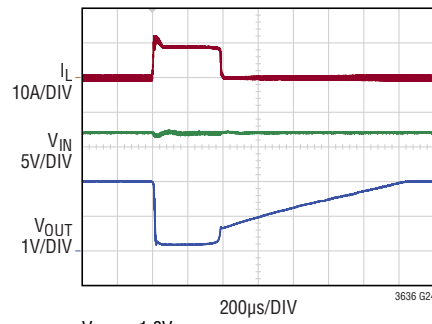
$V_{OUT} = 1.8V$

PIN FUNCTIONS

ITH1 (Pin 1): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

RUN1 (Pin 2): Channel 1 Regulator Enable Pin. Enables channel 1 operation by tying RUN above 1.25V. Tying it below 1V places the part into shutdown. Do not float this pin.

MODE/SYNC (Pin 3): Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTC3636/LTC3636-1 switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

RT (Pin 4): Oscillator Frequency Program Pin. Connect an external resistor (between 80k to 640k) from this pin to GND in order to program the frequency from 500kHz to 4MHz. When RT is tied to $INTV_{CC}$, the switching frequency will default to 2MHz.

INTV$_{CC}$ (Pin 5): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR ceramic capacitor.

TMON (Pin 6): Temperature Monitor Output. A voltage proportional to the measured on-die temperature will appear at this pin. The voltage-to-temperature scaling factor is 200°K/V. See the Applications Information section for detailed information on the TMON function. Tie this pin to $INTV_{CC}$ to disable the temperature monitor circuit.

RUN2 (Pin 7): Channel 2 Regulator Enable Pin. Enables channel 2 operation by tying RUN above 1.22V. Tying it below 1V places the part into shutdown. Do not float this pin.

ITH2 (Pin 8): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

V$_{FB2}$ (Pin 9): Channel 2 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.

PGOOD2 (Pin 10): Channel 2 Open-Drain Power Good Output Pin. PGOOD2 is pulled to ground when the voltage on the V_{FB2} pin is not within ±8% (typical) of the internal 0.6V reference. PGOOD2 becomes high impedance once the V_{FB2} pin returns to within ±5% (typical) of the internal reference.

TRACKSS2 (Pin 11): Output Tracking and Soft-Start Input Pin for Channel 2. Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The LTC3636/LTC3636-1 will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting a capacitor between this pin and PGND.

GND (Pins 12, 18, 19, 25): Power and Signal Ground. These pins must be tied together and soldered to PCB ground.

SW2 (Pins 13, 17): Channel 2 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to V_{IN}.

BOOST2 (Pin 14): Boosted Floating Driver supply for Channel 2. The (+) terminal of the bootstrap capacitor connects to this pin while the (−) terminal connects to the SW pin. The normal operational voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to $V_{IN}+INTV_{CC}$.

PIN FUNCTIONS

V_{IN2} **(Pins 15, 16):** Power Supply Input for Channel 2. This input is capable of operating from a separate supply voltage than V_{IN1}.

SW1 (Pins 20, 24): Channel 1 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to V_{IN}.

V_{IN1} **(Pins 21, 22):** Power Supply Input for Channel 1. Input voltage to the on chip power MOSFETs on channel 1. The internal LDO for $INTV_{CC}$ is powered off of this pin.

BOOST1 (Pin 23): Boosted Floating Driver Supply for Channel 1. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operational voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to $V_{IN} + INTV_{CC}$.

TRACKSS1 (Pin 26): Output Tracking and Soft-Start Input Pin for Channel 1. Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The LTC3636/LTC3636-1 will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting a capacitor between this pin and PGND.

PGOOD1 (Pin 27): Channel 1 Open-Drain Power Good Output Pin. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±8% (typical) of the internal 0.6V reference. PGOOD1 becomes high impedance once the V_{FB1} pin returns to within ±5% (typical) of the internal reference.

V_{FB1} **(Pin 28):** Channel 1 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.

$INTV_{CCT}$ **(Pin 29):** Additional $INTV_{CC}$ pin. Not required to be connected to $INTV_{CC}$ pin for operation.

GNDT (Pins 30, 31, 32): Power Ground. Additional power ground pins for improved thermal dissipation when connected to the GND pins. Not required to be connected to GND pins for operation.

SWT1T (Pin 33): Additional SW1 pin. Not required to be connected to SW1 pins 20 and 24 for operation.

SWT2T (Pins 34): Additional SW2 pin. Not required to be connected to SW2 pins 13 and 17 for operation.

BLOCK DIAGRAM

$$t_{ON} = \frac{V_{VON}}{I_{ION}}$$
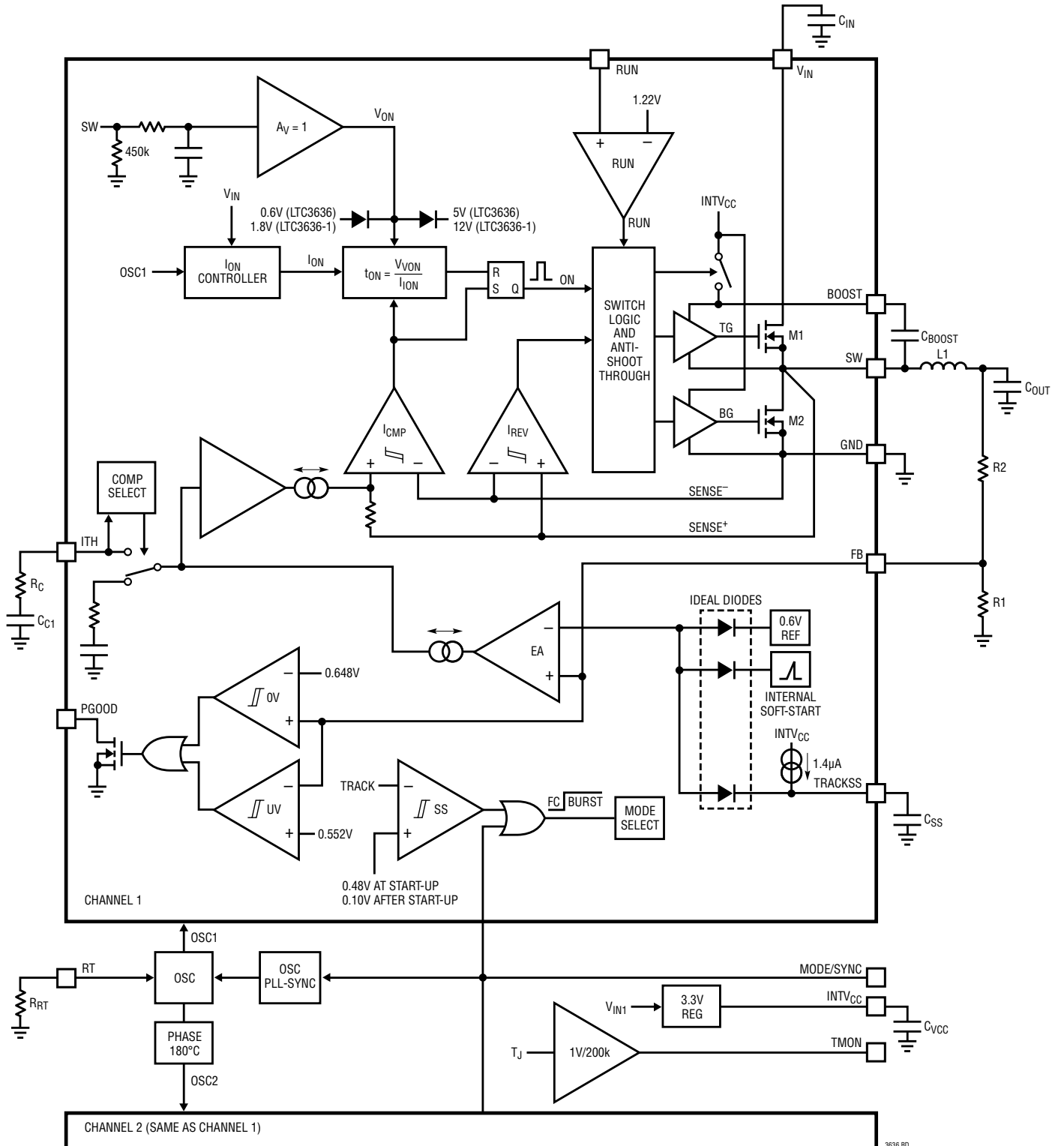
OPERATION

The LTC3636/LTC3636-1 is a dual-channel, current mode monolithic step down regulator capable of providing 6A of output current from each channel. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a constant switching frequency. Both channels share the same clock and run 180° out of phase. Each channel is enabled by raising the voltage on the RUN pin above 1.22V nominally.

Main Control Loop

In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a fixed one-shot timer ("ON" signal in Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, thus restarting the one shot timer and initiating the next cycle. Inductor current is measured by sensing the voltage drop across the SW and GND nodes of the bottom power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this ITH voltage by comparing an internal 0.6V reference to the feedback signal V_{FB} derived from the output voltage. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The ITH voltage then rises until the average inductor current matches that of the load current.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-locked loop servos the switching regulator on-time to track the internal oscillator edge and force a constant switching frequency. A clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external source. The regulator defaults to forced continuous operation once the clock signal is applied.

At light load currents, the inductor current can drop to zero and become negative. In Burst Mode operation, a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, result-ing in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the ITH voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode. Discontinuous mode operation is disabled by tying the MODE/SYNC pin to ground, which forces continuous synchronous operation regardless of output load current.

"Power Good" Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This condition is released once regulation within a ±5% window is achieved. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3636/LTC3636-1 PGOOD falling edge includes a filter time of approximately 40μs.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient input voltage spikes, the LTC3636/LTC3636-1 constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 22.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Overcurrent and Short-Circuit Protection

The LTC3636 protects itself against output overcurrent and short-circuits by sensing the inductor valley current. When the current limit is reached, the output begins to fall, resulting in decreased on-time of the top power MOSFET. If the short is prolonged enough for the on-time to reach its minimum, the off-time will lengthen, lowering the switching frequency and preventing excess current from being drawn from V_{IN}. After the overcurrent or short is removed, the regulator executes its soft-start function to prevent the output voltage from overshooting.

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A general LTC3636/LTC3636-1 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and switching frequency. Component selection typically begins with the selection of the inductor L and resistor R_T. Once the inductor is chosen, the input capacitor, C_{IN}, and the output capacitor, C_{OUT}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, tracking/soft-start, input UVLO, and PGOOD.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Connecting a resistor from the RT pin to GND programs the switching frequency (f) between 500kHz and 4MHz according to the following formula:

$$R_{RT} = \frac{3.2E^{11}}{f}$$

where R_{RT} is in Ω and f is in Hz.

When RT is tied to $INTV_{CC}$, the switching frequency will default to approximately 2MHz, as set by an internal resistor. This internal resistor is more sensitive to process
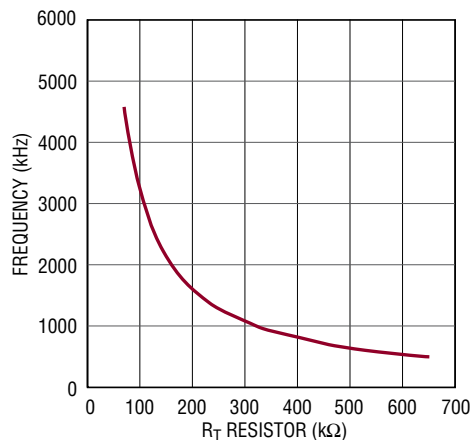
and temperature variations than an external resistor (see Typical Performance Characteristics) and is best used for applications where switching frequency accuracy is not critical.

Dual-Phase Single V_{OUT} Operation

For output loads that demand more than 6A of current, the two channels can be configured in parallel as a single output to provide more output current. During dual-phase operation, it is recommended to set the switching frequency above 800kHz to ensure stability over a wide input voltage range.

With dual-phase operation, the two channels of the LTC3636 are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the switches, greatly reducing the overlap time when they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used and reduces the voltage noise on the supply line.

The two channels in parallel will inherently share current well, because the LTC3636 is a current mode controlled regulator. Good current sharing balances the thermals on the design.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \cdot L} \right) \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where ΔI_L = inductor ripple current, f = operating frequency L = inductor value and V_{IN} is the input power supply voltage applied to the V_{IN} inputs. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater inductor

Figure 1. Switching Frequency vs R_T

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core loss, greater ESR loss in the output capacitor, and larger output voltage ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point is to choose a ripple current of 2.4A which is about 40% of $I_{OUT(MAX)}$. Exceeding 60% of $I_{OUT(MAX)}$ is not recommended. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \cdot \Delta I_{L(MAX)}} \right) \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, leading to increased DCR and copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current, so it is important to ensure that the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 gives a sampling of available surface mount inductors.

Table 1. Inductor Selection Table

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Würth Electronik WE-HC 744312 Series				
0.25	2.5	18	7 × 7.7	3.8
0.47	3.4	16		
0.72	7.5	12		
1.0	9.5	11		
1.5	10.5	9		
Vishay IHLP-2020BZ-01 Series				
0.22	5.2	15	5.2 × 5.5	2
0.33	8.2	12		
0.47	8.8	11.5		
0.68	12.4	10		
1	20	7		
Toko FDVE0603 Series				
0.33	2.7	15.9	7.4 × 6.7	3.0
0.47	3.7	15.6		
0.68	6	10.4		
0.75	6.2	10.9		
1	8.5	9.5		
Coilcraft XAL6030 Series				
0.20	3.04	17.2	6.4 × 6.6	3
0.33	5.18	15.4		
0.56	8	13.8		
0.82	11.8	11.5		
1.0	13.25	9.6		
TDK SMP5030 Series				
0.2	2.31	21	5.2 × 5	3
0.35	4.29	14.9		
0.75	9.35	9.7		
1	11.44	8.5		

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT} \left(V_{IN} - V_{OUT} \right)}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

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Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3636/LTC3636-1 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is approximated by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

When using low-ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor of approximately:

$$C_{OUT} \approx \frac{3 \cdot \Delta I_{OUT}}{f \cdot V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

INTV$_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator draws power from the V_{IN1} input and produces the 3.3V supply that powers the internal bias circuitry and drives the gate of the internal MOSFET switches. The INTV$_{CC}$ pin connects to the output of this regulator and must have a minimum of 4.7µF ceramic decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the INTV$_{CC}$ and GND pins to provide the transient currents required by the LTC3636/LTC3636-1. High input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting any external load to the INTV$_{CC}$ pin is not recommended since it may impact LTC3636/LTC3636-1 operation while increasing power dissipation and die temperature.

Boost Capacitor

The LTC3636/LTC3636-1 uses a "bootstrap" circuit to create a voltage rail above the applied input voltage V_{IN}. Specifically, a boost capacitor, C_{BOOST}, is charged to a voltage approximately equal to INTV$_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be

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equal to approximately V_{IN} + 3.3V. For most applications, a 0.1µF ceramic capacitor closely connected between the BOOST and SW pins will provide adequate performance.

Output Voltage Programming

Each regulator's output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

The desired output voltage is set by appropriate selection of resistors R1 and R2 as shown in Figure 2. Choosing large values for R1 and R2 will result in improved zero-load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the V_{FB} node. Care should be taken to route the V_{FB} trace away from any noise source, such as the SW trace. To improve the frequency response of the main control loop, a feedforward capacitor, C_F, may be used as shown in Figure 2.
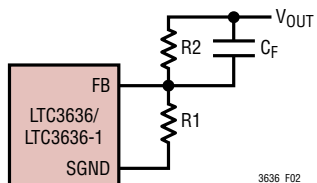

Figure 2. Setting the Output Voltage

If the output voltage is outside the V_{ON} sense range (0.6V – 5V for the LTC3636, 1.8V – 12V for the LTC3636-1), the output voltage will stay in regulation, but the switching frequency may deviate from the programmed frequency.

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3636/LTC3636-1 can turn on the bottom power MOSFET, trip the current comparator and turn the power MOSFET back off. This time is typically 100ns. For the controlled on-time architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{(MAX)} = 1 - f \bullet \left(t_{OFF(MIN)} + 2 \bullet t_{DEAD}\right)$$

where f is the switching frequency, t_{DEAD} is the nonoverlap time, or "dead time" (typically 5ns) and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - f \bullet \left(t_{OFF(MIN)} + 2 \bullet t_{DEAD}\right)}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 30ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{(MIN)} = \left(f \bullet t_{ON(MIN)}\right)$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This constraint may not be of critical importance in most cases, so high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor and Capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

Internal/External Loop Compensation

The LTC3636/LTC3636-1 provides the option to use a fixed internal loop compensation network to reduce both the required external component count and design time. The internal loop compensation network can be selected by connecting the ITH pin to the $INTV_{CC}$ pin. To ensure stability it is recommended that internal compensation only be used with applications with f_{SW} > 1MHz. Alternatively, the user may choose specific external loop compensation components to optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the ITH pin.

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Suggested compensation component values are shown in Figure 3. For a 2MHz application, an R-C network of 220pF and 13kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 10pF bypass capacitor on the ITH pin is recommended for the purposes of filtering out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor C_F can be added to improve the high frequency response, as previously shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.
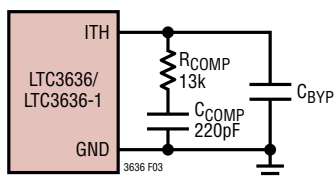

Figure 3. Compensation Component

Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time, and settling behavior at this test point reflect the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external components shown in Figure 3 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of ~1μs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \cdot ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10μF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft starting.

On-Die Temperature Monitor

The LTC3636/LTC3636-1 produces a voltage at the TMON pin proportional to the measured junction temperature. The junction temperature-to-voltage scaling factor is 200°K/V. Thus, to obtain the junction temperature in degrees Kelvin, simply multiply the voltage provided at the TMON pin by the scaling factor. To obtain the junction temperature in degrees Celsius, subtract 273 from the value obtained in degrees Kelvin.

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The temperature monitor function uses a chopping technique to achieve high precision. As a result, a small periodic ripple may be seen at the TMON pin, the average of which is the measured value of interest. The ripple frequency will be the operating frequency divided by 32. If required, a 1μF or greater capacitor to GND may be placed on the output to reduce the magnitude of the ripple.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Floating this pin or connecting it to $INTV_{CC}$ enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is tied to ground, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency.

The LTC3636/LTC3636-1 will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place both regulators into forced continuous mode operation.

Output Voltage Tracking and Soft-Start

The LTC3636/LTC3636-1 allows the user to control the output voltage ramp rate by means of the TRACKSS pin. From 0 to 0.6V, the TRACKSS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of the TRACKSS

pin. When TRACKSS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

The voltage at the TRACKSS pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4μA pull-up current source to implement a soft-start function by connecting an external capacitor (C_{SS}) from the TRACKSS pin to ground. The relationship between output rise time and TRACKSS capacitance is given by:

$$t_{SS} = 430000\Omega \bullet C_{SS}$$

A default internal soft-start ramp forces a minimum soft-start time of 1000μs by overriding the TRACKSS pin input during this time period. Hence, capacitance values less than approximately 2200pF will not significantly affect soft-start behavior.

When driving the TRACKSS pin from another source, each channel's output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 4. In the following discussions, V_{OUT1} refers to the LTC3636/LTC3636-1 output 1 as a master channel and V_{OUT2} refers to output 2 as a slave channel. In practice, either channel can be used as the master.

To implement the coincident tracking in Figure 4a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACKSS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 5a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}.
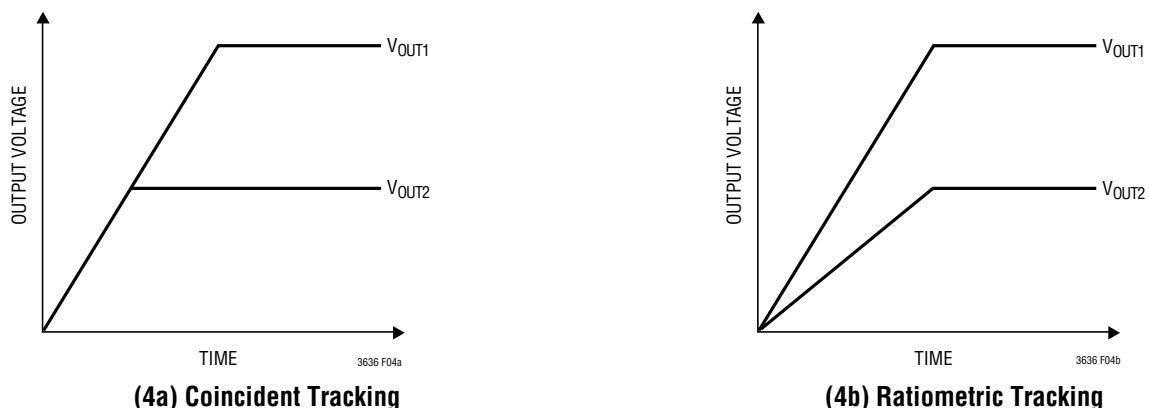

(4a) Coincident Tracking

(4b) Ratiometric Tracking

Figure 4. Two Different Modes of Output Voltage Tracking

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(5a) Coincident Tracking Setup
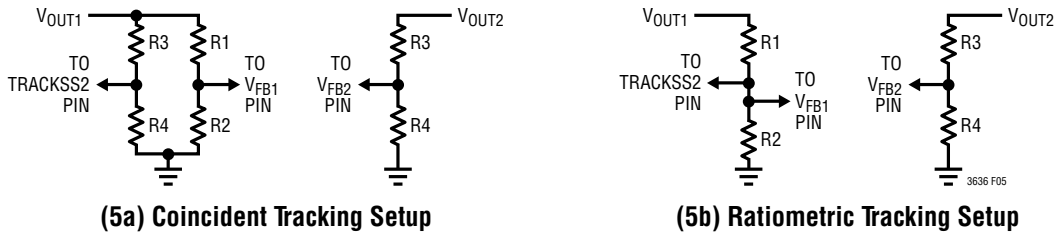
(5b) Ratiometric Tracking Setup

Figure 5. Setup for Coincident and Ratiometric Tracking

To implement the ratiometric tracking, the feedback pin of the master channel should connect to the TRACKSS pin of the slave channel (as in Figure 5b). By selecting different resistors, the LTC3636/LTC3636-1 can achieve different modes of tracking including the two in Figure 4.

Upon start-up, the regulator defaults to Burst Mode operation until the output exceeds 80% of its final value ($V_{FB} >$ 0.48V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value (as it may when tracking down, for instance), the regulator will automatically switch to Burst Mode operation to prevent inductor saturation and improve TRACKSS pin accuracy.

Output Power Good

The PGOOD output of the LTC3636/LTC3636-1 is driven by a 25Ω (typical) open-drain pull-down device. This device will be turned off once the output voltage is within 5% (typical) of the target regulation point, allowing the voltage at PGOOD to rise via an external pull-up resistor. If the output voltage exits an 8% (typical) regulation window around the target regulation point, the open-drain output will pull down with 20Ω output resistance to ground, thus dropping the PGOOD pin voltage. This behavior is described in Figure 6.

A filter time of 40µs (typical) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. As a result, the output voltage must be within the target regulation window of 5% for 40µs before the PGOOD pin pulls high. Conversely, the output voltage must exit the 8% regulation window for 40µs before the PGOOD pin pulls to ground.

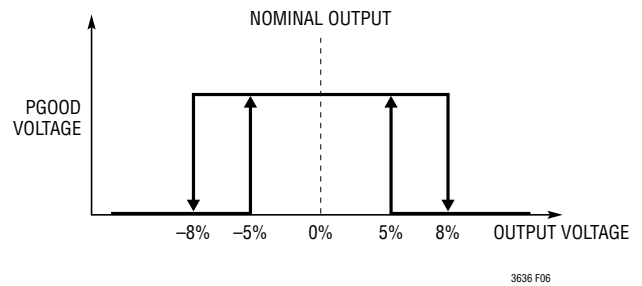**Figure 6. PGOOD Pin Behavior**

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% − (L1 + L2 + L3 +…)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3636/LTC3636-1 circuits: 1) I^2R losses, 2) switching losses and quiescent power loss 3) transition losses and other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 − DC)$$

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The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

2. The internal LDO draws power from the V_{IN} input to regulate the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, the gate charges $(Q_T + Q_B)$ on each LTC3636/LTC3636-1 regulator channel are approximately 7.5nC.

To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by the voltage applied to V_{IN}:

$$P_{LDO} = (I_{GATECHG} + I_Q) \cdot V_{IN}$$

3. Other "hidden" losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3636/LTC3636-1 internal power devices switch quickly enough that these losses are not significant compared to other sources.

Other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3636/LTC3636-1 requires the ground pins to be well soldered to the PC board to provide good thermal contact. This gives the QFN package exceptional thermal properties, which is necessary to prevent excessive self-heating of the part in normal operation.

In a majority of applications, the LTC3636/LTC3636-1 does not dissipate much heat due to its high efficiency and low thermal resistance of its QFN package. However, in applications where the LTC3636/LTC3636-1 is running at high ambient temperature, high input supply voltage, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until temperature returns to 150°C.

To prevent the LTC3636/LTC3636-1 from exceeding the maximum junction temperature of 125°C, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \cdot \theta_{JA}$$

As an example, consider the case when one of the regulators is used in an application where V_{IN} = 12V, I_{OUT} = 6A, frequency = 1MHz, V_{OUT} = 1.8V. From the $R_{DS(ON)}$ graphs in the Typical Performance Characteristics section, the top switch on-resistance is nominally 36mΩ and the bottom switch on-resistance is nominally 19mΩ at 50°C ambient. The equivalent power MOSFET resistance R_{SW} is:

$$R_{DS(ON)TOP} \cdot \frac{1.8V}{12V} + R_{DS(ON)BOT} \cdot \frac{10.2V}{12V} = 21.6m\Omega$$

From the previous section's discussion on gate drive, we estimate the total gate drive current through the LDO to be 1MHz • 7.5nC = 7.5mA, and I_Q of one channel is 0.65mA (see Electrical Characteristics). Therefore, the total power dissipated by a single regulator is:

$$P_D = I_{OUT}^2 \cdot R_{SW} + V_{IN} \cdot (I_{GATECHG} + I_Q)$$

$$P_D = (6A)^2 \cdot (0.0216\Omega) + (12V) \cdot (7.5mA + 0.65mA)$$
$$= 0.874W$$

Running two regulators under the same conditions would result in a power dissipation of 1.748W. The QFN 5mm × 4mm package junction-to-ambient thermal resistance, θ_{JA}, is around 21°C/W. Therefore, the junction temperature of the regulator operating in a 50°C ambient temperature is approximately:

$$T_J = 1.748W \cdot 21°C/W + 50°C = 87°C$$

APPLICATIONS INFORMATION

which is below the maximum junction temperature of 125°C. With higher ambient temperatures, a heat sink or cooling fan should be considered to drop the junction-to-ambient thermal resistance.

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 50°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 15% at 87°C yields a new junction temperature of 92°C. If the application calls for a higher ambient temperature and/or higher load currents, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Figure 7 is a temperature derating curve based on the DC2335 demo board (QFN package). It can be used to estimate the maximum allowable ambient temperature for given DC load currents in order to avoid exceeding the maximum operating junction temperature of 125°C.
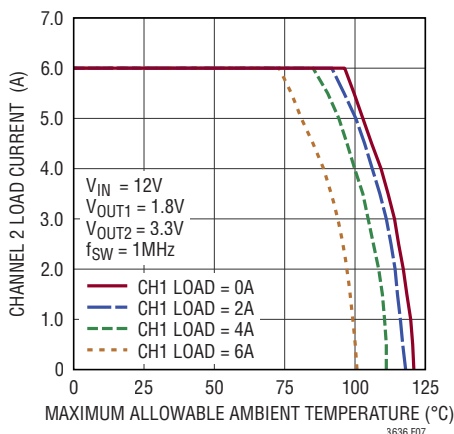

Figure 7. Temperature Derating Curve for DC2335 Demo Circuit

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3636/LTC3636-1. Check the following in your layout:

1) Do the input capacitors connect to the V_{IN} and GND pins as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

2) The output capacitor, C_{OUT}, and inductor L should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to both GND and the (–) plate of C_{IN}.

3) The resistive divider, (e.g. R1 to R4 in Figure 8) must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. Keep R1 and R2 close to the IC.

4) Keep sensitive components away from the SW pin. The R_T resistor, the compensation components, the feedback resistors, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor L.

5) A ground plane is preferred.

6) Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside of the package (GND).

Refer to Figure 9 for board layout examples.

Design Example

As a design example, consider using the LTC3636/LTC3636-1 in an application with the following specifications: $V_{IN(MAX)} = 13.2V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 3.3V$, $I_{OUT(MAX)} = 6A$, $I_{OUT(MIN)} = 10mA$, f = 2MHz, V_{DROOP} ~ (5% • V_{OUT}). The following discussion will use equations from the previous sections.

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

First, the correct R_T resistor value for 2MHz switching frequency must be chosen. Based on the equation discussed earlier, R_T should be 160k; the closest standard value is 162k. RT can be tied to $INTV_{CC}$ if switching frequency accuracy is not critical.

Next, determine the channel 1 inductor value for about 40% ripple current at maximum V_{IN}:

$$L1 = \left(\frac{1.8V}{2MHz \cdot 2.4A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 0.32\mu H$$

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A standard value of 0.33µH should work well here. Solving the same equation for channel 2 results in a 0.47µH inductor.

C_{OUT} will be selected based on the charge storage requirement. For a V_{DROOP} of 90mV for a 6A load step:

$$C_{OUT1} \approx \frac{3 \cdot \Delta I_{OUT}}{f \cdot V_{DROOP}} = \frac{3 \cdot (6A)}{(2MHz)(90mV)} = 100µF$$

Two 47µF ceramic capacitor should be used for channel 1. Solving the same equation for channel 2 (using 5% of V_{OUT} for V_{DROOP}) results in 55µF of capacitance (47µF is the closest standard value).

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 6A \frac{\sqrt{1.8V(13.2V - 1.8V)}}{13.2V} = 2.1A$$

Solving this equation for channel 2 results in an RMS input current of 2.8A. Decoupling each V_{IN} input with a 47µF ceramic capacitor should be adequate for most applications.

Lastly, the feedback resistors must be chosen. Picking R1 and R3 to be 13.7k, R2 and R4 are calculated to be:

$$R2 = (13.7k) \cdot \left(\frac{1.8V}{0.6V} - 1 \right) = 27.4k$$

$$R4 = (13.7k) \cdot \left(\frac{3.3V}{0.6V} - 1 \right) = 61.9k$$
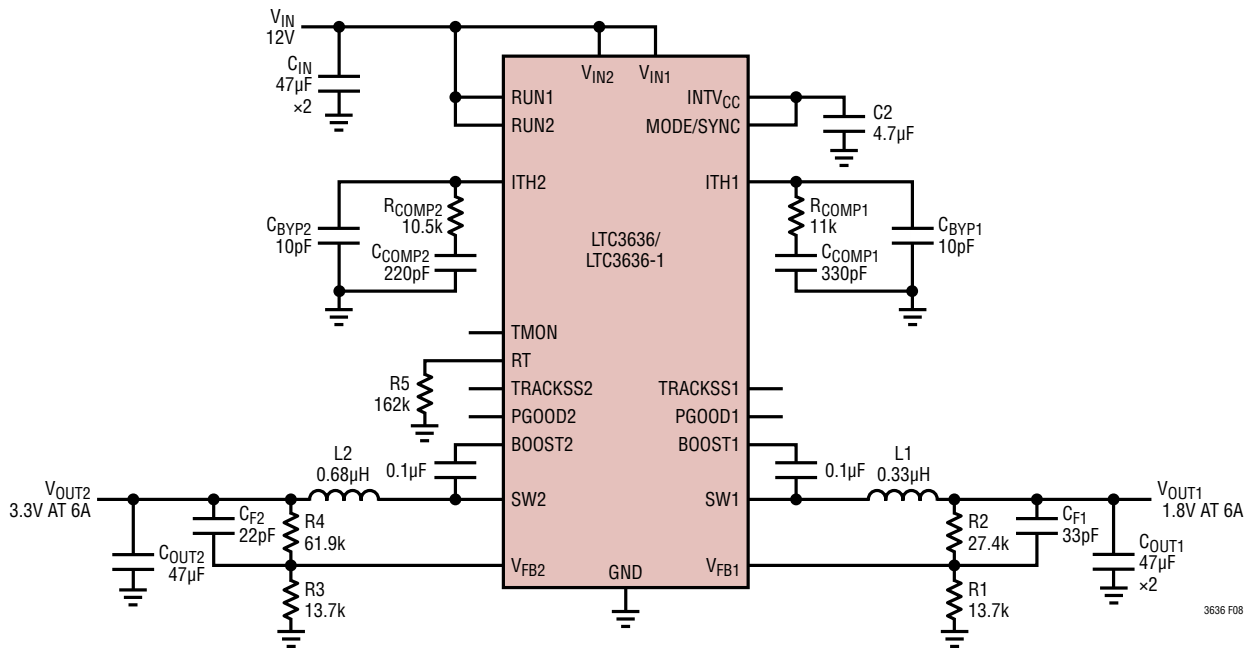
The final circuit is shown in Figure 8.

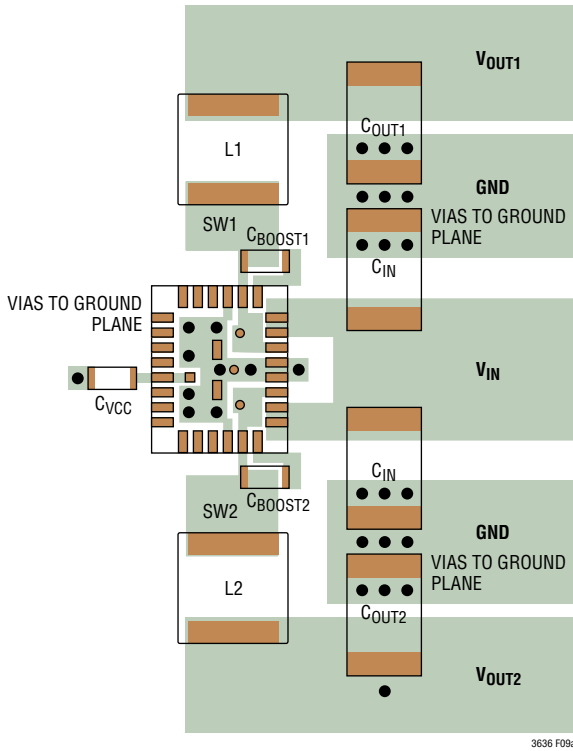Figure 8. Design Example Circuit

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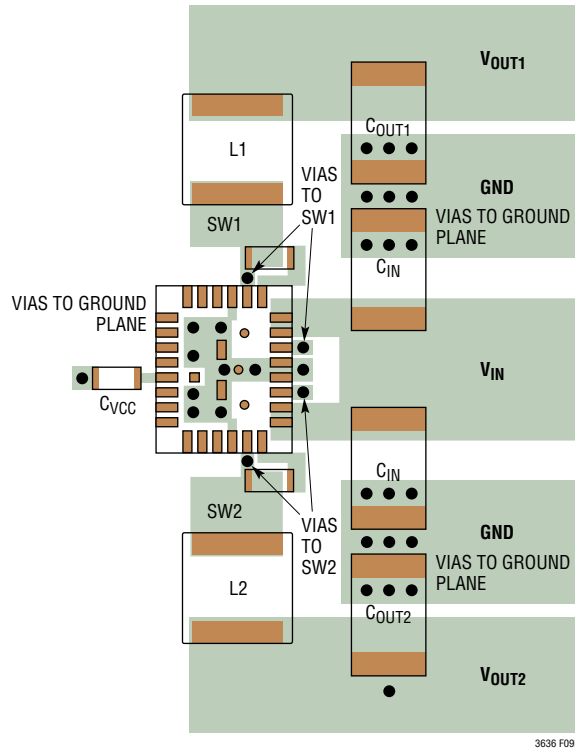Figure 9a. Example of Power Component Layout for QFN Package

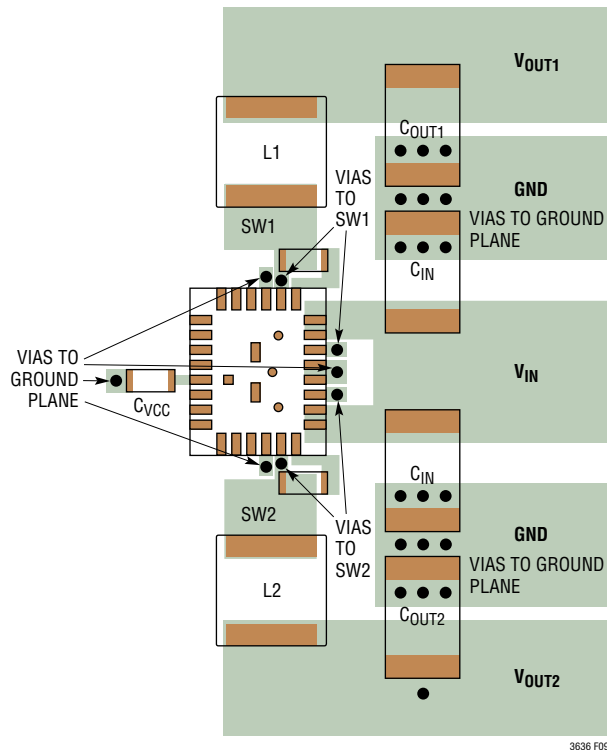Figure 9b. Alternate Layout with GNDT Pins Connected to GND

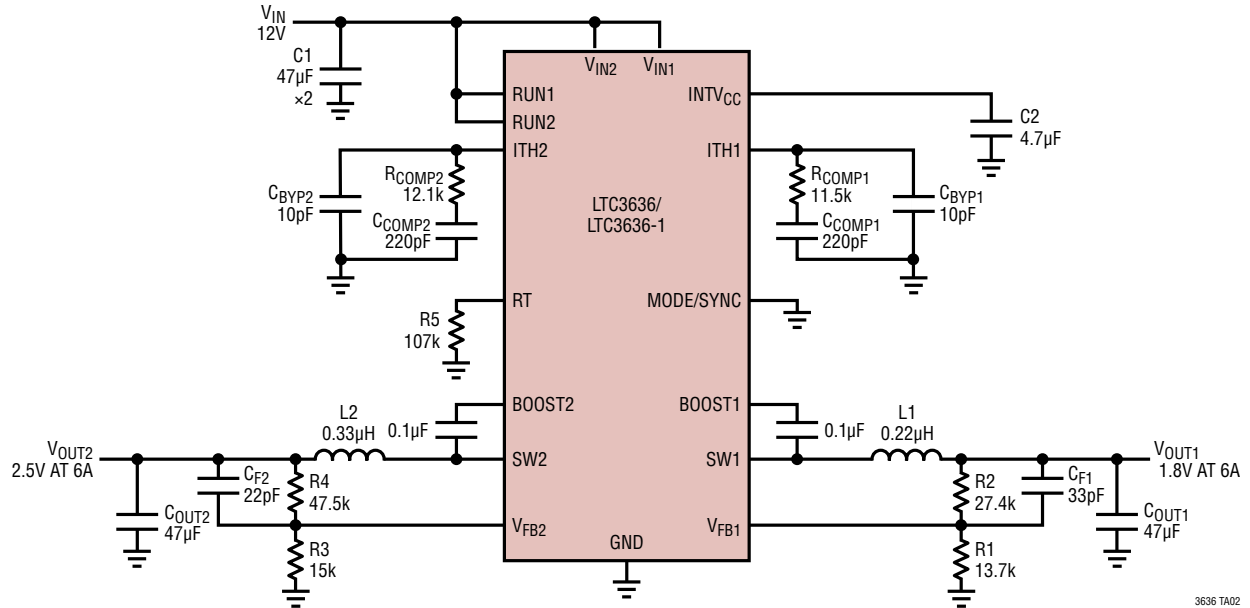Figure 9c. Alternate Layout with Pins 29 to 34 Unconnected

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For more information www.linear.com/LTC3636

TYPICAL APPLICATIONS

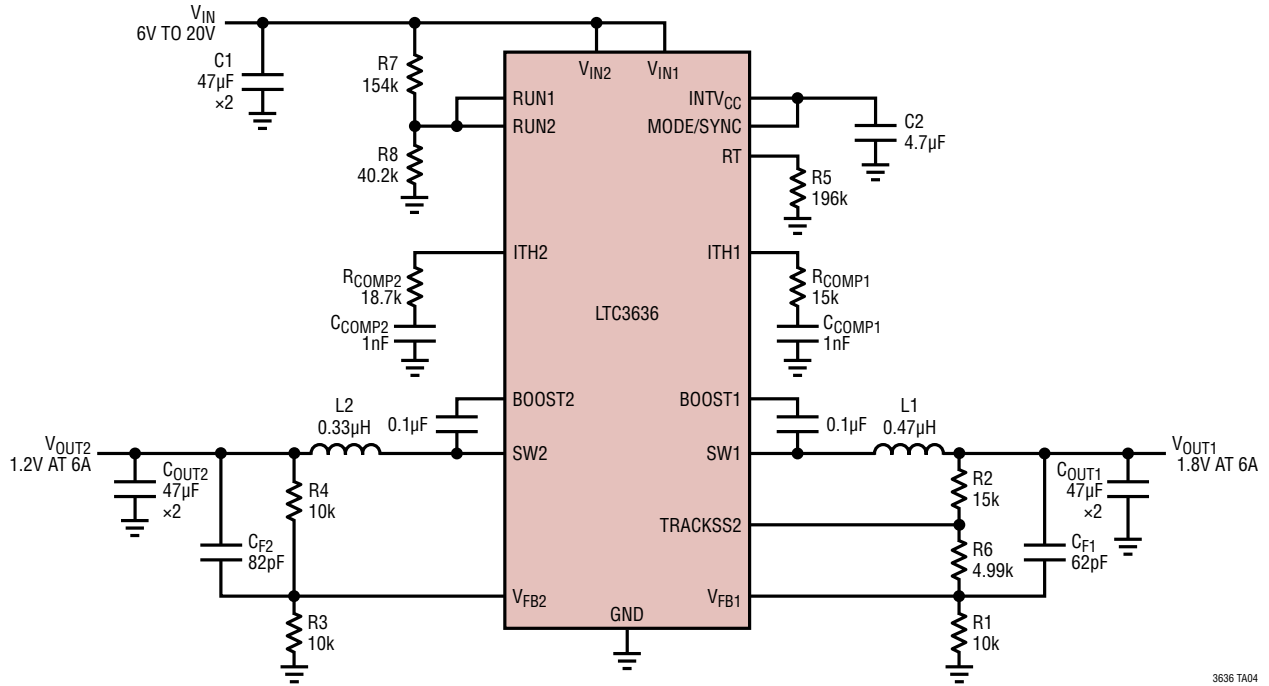**1.8V/2.5V 3MHz Buck Regulator**

3636 TA02

3.3V/1.8V Sequenced Regulator with 8V Input UVLO (V_OUT1 Enabled After V_OUT2)
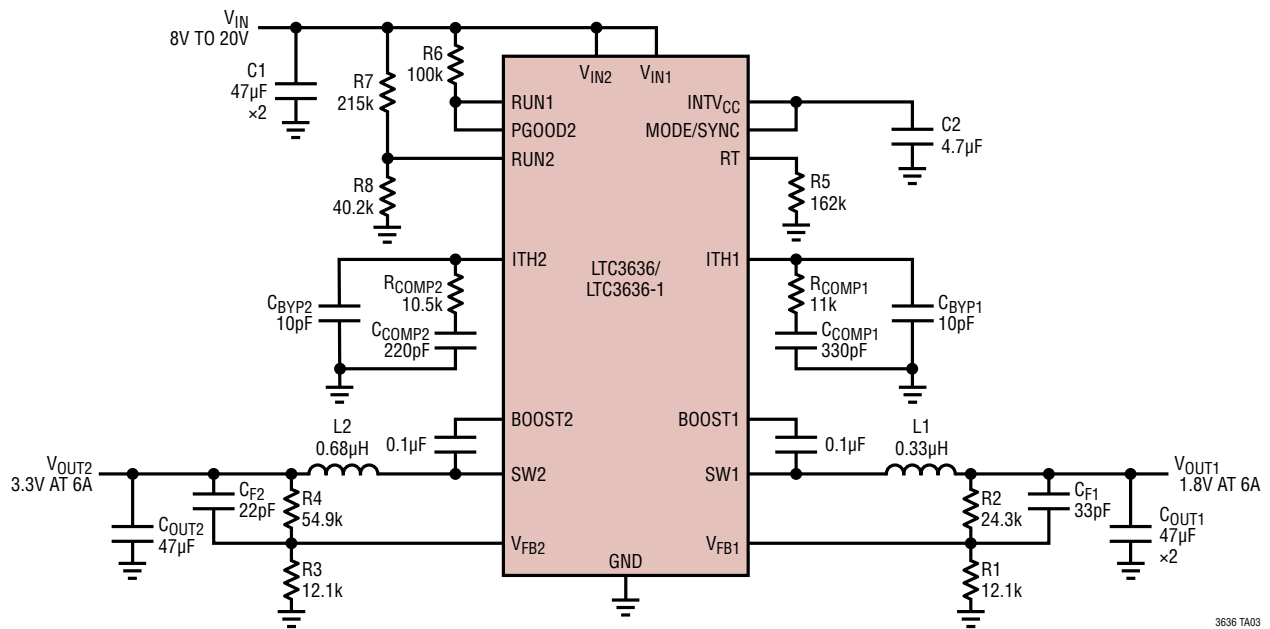
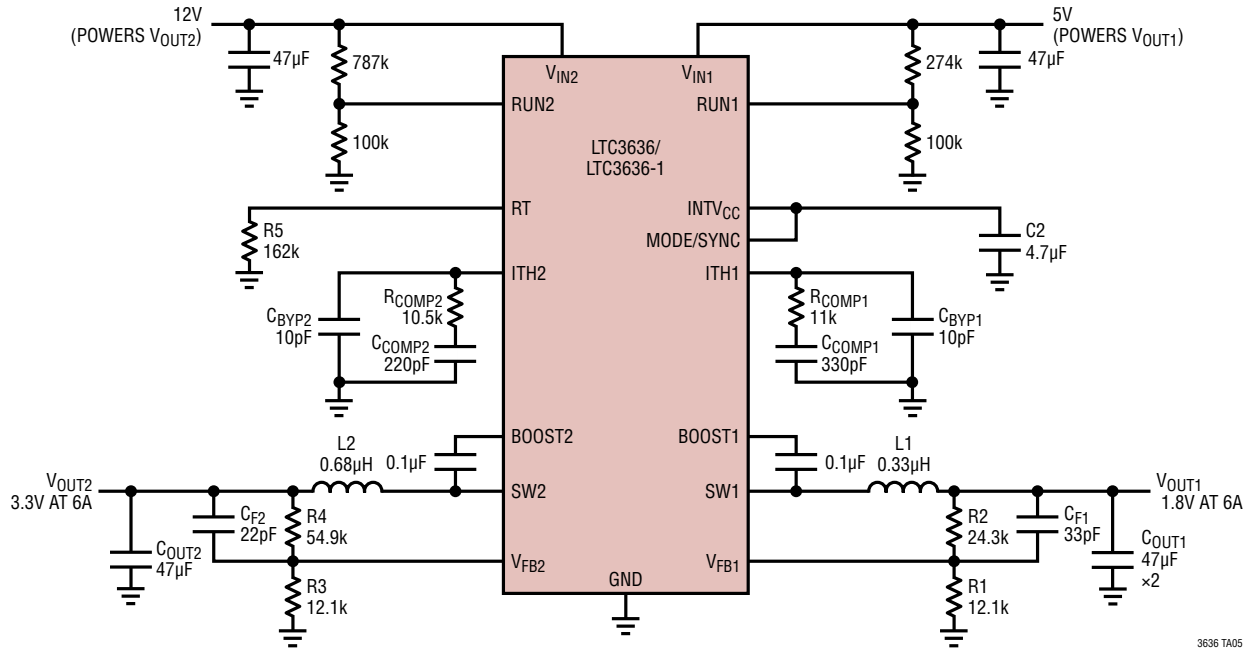3636 TA03

TYPICAL APPLICATIONS

1.2V/1.8V Buck Regulator with Coincident Tracking and 6V Input UVLO

3636 TA04

TYPICAL APPLICATIONS

Dual Output Regulator from Multiple Input Supplies (Powers V_{IN1} Before V_{IN2})

3636 TA05

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3636#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1538 Rev A)

Exposed Pad Variation AA

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

(UDC28) QFN 0816 REV A

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/17	Revised thermal resistance values in Pin Configuration	2
		Revised Thermal Considerations section	19, 20
B	02/18	Clarified Minimum On-Time	3

TYPICAL APPLICATION

12A 1MHz 2-Phase Buck Regulator

3636 TA06
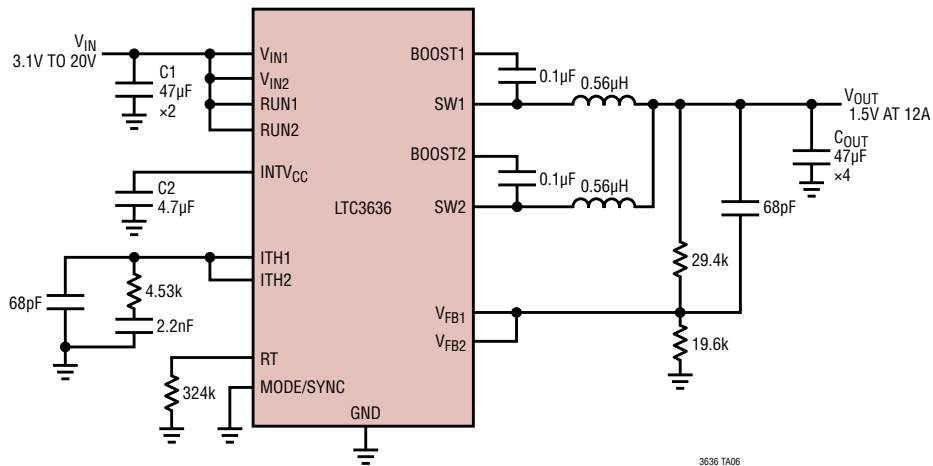
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3633/ LTC3633A	15V/20V, Dual 3A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 13µA, 4mm × 5mm QFN-28, TSSOP-28E
LTC3605/ LTC3605A	15V/20V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 3mm QFN-16, MSOP-16E
LTC3626	20V, 2.5A Synchronous Monolithic Step-Down Regulator with Current and Temperature Monitoring	95% Efficiency, V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 4mm QFN-20
LTC7124	17V, Dual 3.5A Synchronous Step-Down Regulator with Ultralow Quiescent Current	95% Efficiency, V_{IN}: 3.1V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q < 8µA (Both Channels Enabled), I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3622	17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q < 5µA (Both Channels Enabled), I_{SD} < 1µA, 3mm × 4mm DFN-14 and MSOP-16 Packages