DATASHEET

ZVS Full-Bridge PWM Controller with Adjustable Synchronous Rectifier Control

ISL78223

The ISL78223 is a high performance zero voltage switching (ZVS) full-bridge PWM controller. It achieves ZVS operation by driving the upper bridge FETs at a fixed 50% duty cycle while the lower bridge FETs are trailing-edge modulated with adjustable resonant switching delays.

Adding to the ISL78223's feature set are average current monitoring and soft-start. The average current signal may be used for average current limiting, current sharing circuits and average current mode control. Additionally, the ISL78223 supports both voltage and current mode control.

The ISL78223 features complemented PWM outputs for synchronous rectifier (SR) control. The complemented outputs may be dynamically advanced or delayed relative to the PWM outputs using an external control voltage.

This advanced BiCMOS design features precision deadtime and resonant delay control, and an oscillator adjustable to 2MHz operating frequency. Additionally, Multi-Pulse Suppression ensures alternating output pulses at low duty cycles where pulse skipping may occur.

The ISL78223 is rated for the automotive temperature range (-40°C to +105°C).

Features

- Adjustable resonant delay for ZVS operation
- Synchronous rectifier control outputs with adjustable delay/advance
- Voltage or current mode control
- 3% current limit threshold
- Adjustable average current limit
- Adjustable deadtime control
- 175µA start-up current
- Supply UVLO
- Adjustable oscillator frequency up to 2MHz
- Internal over-temperature protection
- Buffered oscillator sawtooth output
- Fast current sense to output delay
- Adjustable cycle-by-cycle peak current limit
- 70ns leading edge blanking
- Multi-pulse suppression
- Pb-free (RoHS compliant)

Applications

- ZVS full-bridge converters
- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems

FIGURE 1. BOARD LAYOUT

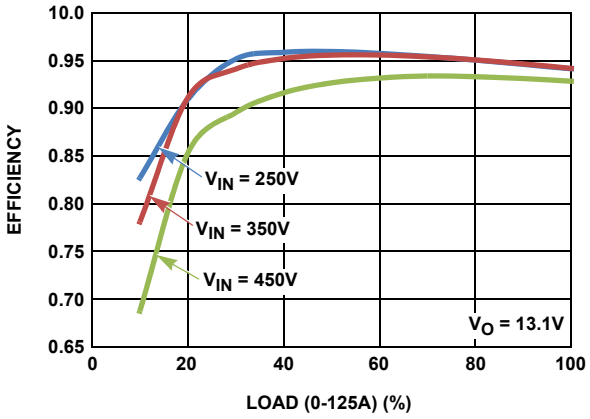
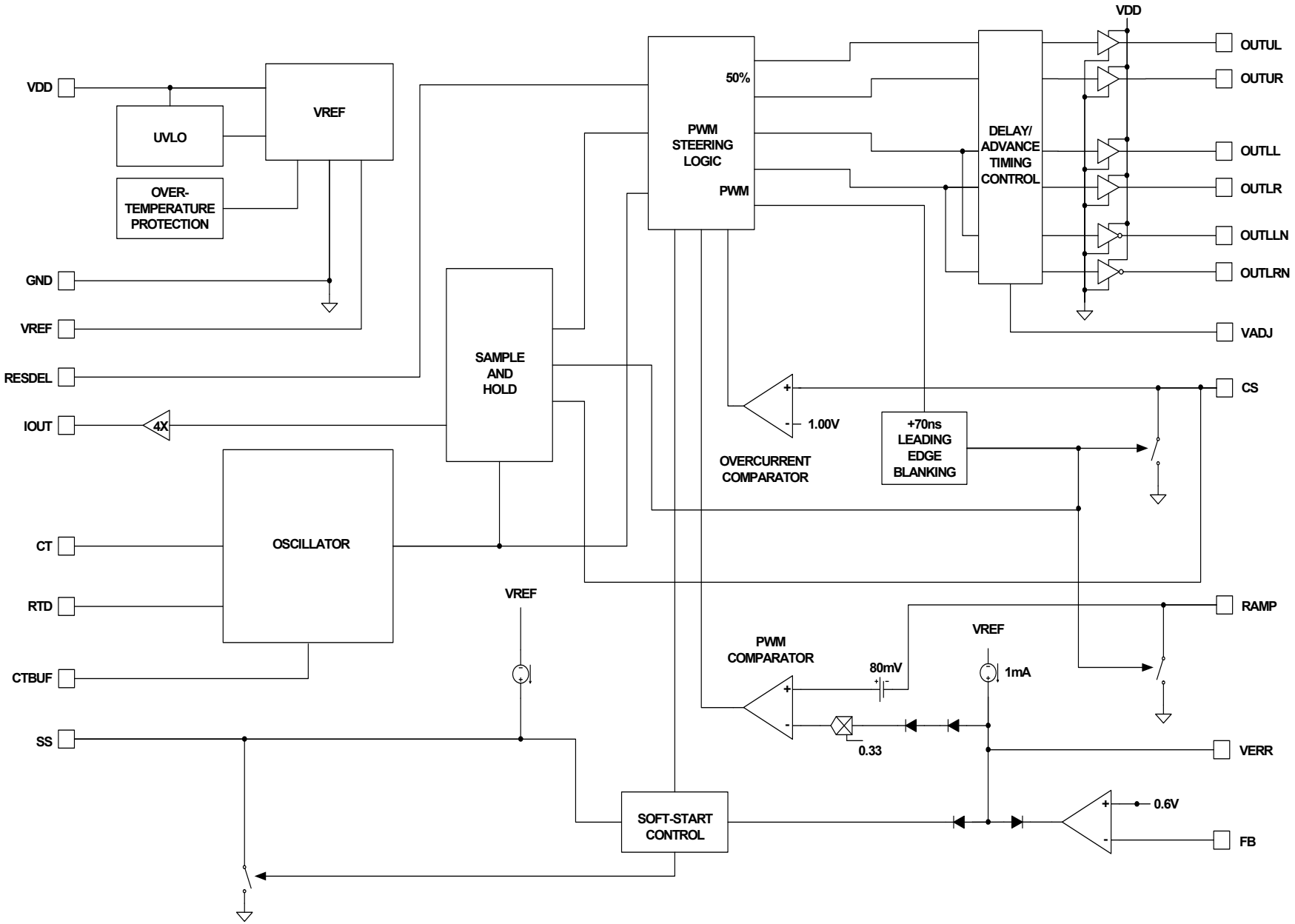
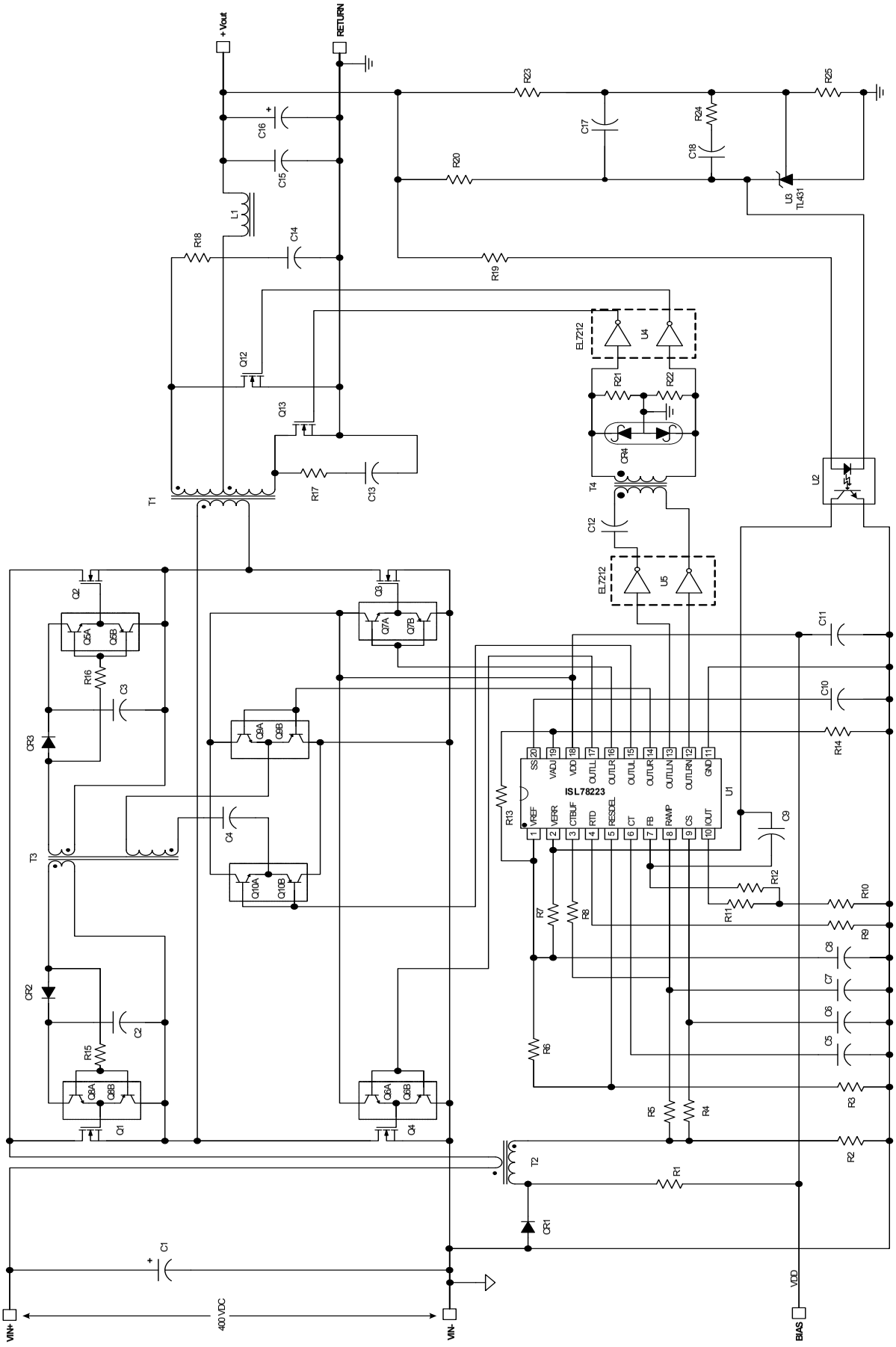


FIGURE 2. EFFICIENCY vs LOAD

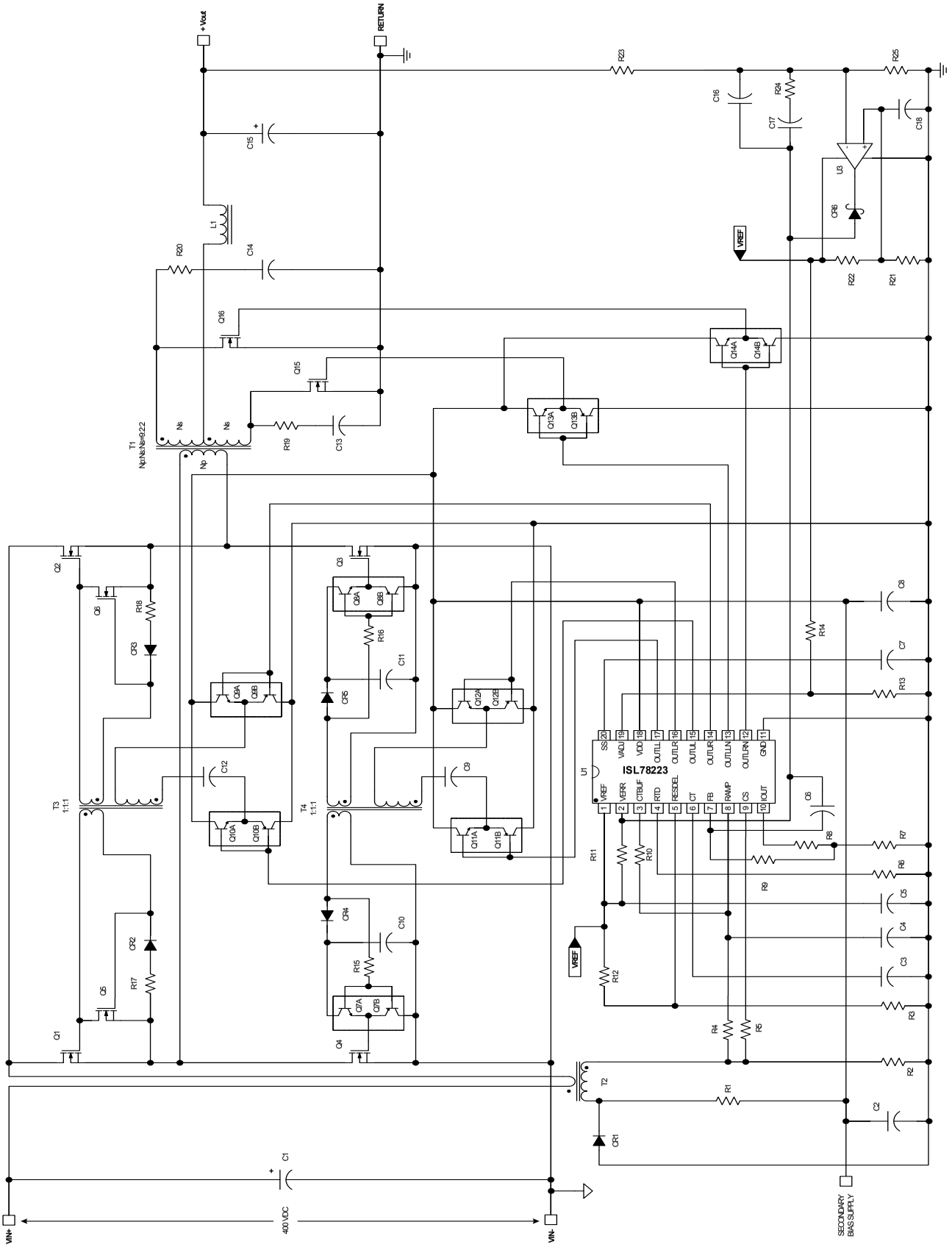
Functional Block Diagram



Typical Application - High Voltage Input Primary Side Control ZVS Full-Bridge Converter

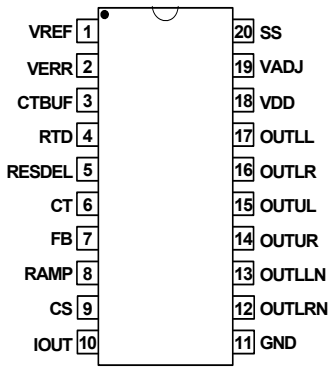


Typical Application - High Voltage Input Secondary Side Control ZVS Full-Bridge Converter



Pin Configuration

ISL78223
(20 LD QSOP)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	VREF	The 5V reference voltage output having 3% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 2.2µF low ESR capacitor.
2	VERR	The control voltage input to the inverting input of the PWM comparator. The output of an external error amplifier (EA) is applied to this input, either directly or through an optocoupler, for closed loop regulation. VERR has a nominal 1mA pull-up current source. When VERR is driven by an optocoupler or other current source device, a pull-up resistor from VREF is required to linearize the gain. Generally, a pull-up resistor on the order of 5kΩ is acceptable.
3	CTBUF	CTBUF is the buffered output of the sawtooth oscillator waveform present on CT and is capable of sourcing 2mA. It is offset from ground by 0.40V and has a nominal valley-to-peak gain of 2. It may be used for slope compensation.
4	RTD	This is the oscillator timing capacitor discharge current control pin. The current flowing in a resistor connected between this pin and GND determines the magnitude of the current that discharges CT. The CT discharge current is nominally 20x the resistor current. The PWM deadtime is determined by the timing capacitor discharge duration. The voltage at RTD is nominally 2.00V.
5	RESDEL	Sets the resonant delay period between the toggle of the upper FETs and the turn on of either of the lower FETs. The voltage applied to RESDEL determines when the upper FETs switch relative to a lower FET turning on. Varying the control voltage from 0 to 2V increases the resonant delay duration from 0 to 100% of the deadtime. The control voltage divided by 2 represents the percent of the deadtime equal to the resonant delay. In practice the maximum resonant delay must be set lower than 2V to ensure that the lower FETs, at maximum duty cycle, are OFF prior to the switching of the upper FETs.
6	CT	The oscillator timing capacitor is connected between this pin and GND. It is charged through an internal 200µA current source and discharged with a user adjustable current source controlled by RTD.
7	FB	FB is the inverting inputs to the error amplifier (EA). The amplifier may be used as the error amplifier for voltage feedback or used as the average current limit amplifier (IEA). If the amplifier is not used, FB should be grounded.
8	RAMP	This is the input for the sawtooth waveform for the PWM comparator. The RAMP pin is shorted to GND at the termination of the PWM signal. A sawtooth voltage waveform is required at this input. For current-mode control this pin is connected to CS and the current loop feedback signal is applied to both inputs. For voltage mode control, the oscillator sawtooth waveform may be buffered and used to generate an appropriate signal, RAMP may be connected to the input voltage through a RC network for voltage feed- forward control, or RAMP may be connected to VREF through a RC network to produce the desired sawtooth waveform.
9	CS	This is the input to the overcurrent comparator. The overcurrent comparator threshold is set at 1V nominal. The CS pin is shorted to GND at the termination of either PWM output. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. This delay may result in CS being discharged prior to the power switching device being turned off.

Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
10	IOUT	Output of the 4x buffer amplifier of the sample and hold circuitry that captures and averages the CS signal.
11	GND	Signal and power ground connections for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
12, 13	OUTLRN, OUTLLN	These outputs are the complements of the PWM (lower) bridge FETs. OUTLLN is the complement of OUTLL and OUTLRN is the complement of OUTLR. These outputs are suitable for control of synchronous rectifiers. The phase relationship between each output and its complement is controlled by the voltage applied to VADJ.
14, 15	OUTUR, OUTUL,	These outputs control the upper bridge FETs and operate at a fixed 50% duty cycle in alternate sequence. OUTUL controls the upper left FET and OUTUR controls the upper right FET. The left and right designation may be switched as long as they are switched in conjunction with the lower FET outputs, OUTLL and OUTLR.
16, 17	OUTLR, OUTLL	These outputs control the lower bridge FETs, are pulse width modulated, and operate in alternate sequence. OUTLL controls the lower left FET and OUTLR controls the lower right FET. The left and right designation may be switched as long as they are switched in conjunction with the upper FET outputs, OUTUL and OUTUR.
18	VDD	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible. VDD is monitored for supply voltage undervoltage lock-out (UVLO). The start and stop thresholds track each other resulting in relatively constant hysteresis.
19	VADJ	A 0V to 5V control voltage applied to this input sets the relative delay or advance between OUTLL/OUTLR and OUTLLN/OUTLRN. The phase relationship between OUTUL/OUTUR and OUTLL/OUTLR is maintained regardless of the phase adjustment between OUTLL/OUTLR and OUTLLN/OUTLRN. The range of phase delay/advance is either zero or 40 to 300ns with the phase differential increasing as the voltage deviation from 2.5V increases. The relationship between the control voltage and phase differential is non-linear. The gain ($\Delta t/\Delta V$) is low for control voltages near 2.5V and rapidly increases as the voltage approaches the extremes of the control range. This behavior provides the user increased accuracy when selecting a shorter delay/advance duration. When the PWM outputs are delayed relative to the SR outputs (VADJ < 2.425V), the delay time should not exceed 90% of the deadtime as determined by RTD and CT.
20	SS	Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor and the internal current source determine the rate of increase of the duty cycle during start-up. SS may also be used to inhibit the outputs by grounding through a small transistor in an open collector/drain configuration.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL78223AAZ	78223 AAZ	-40 to +105	20 Ld QSOP	M20.15

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78223. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +22.0V
OUTxxx . . . . . GND - 0.3V to V_{DD}
Signal Pins. . . . . GND - 0.3V to V_{REF} + 0.3V
V_{REF} . . . . . .GND - 0.3V to 6.0V
Peak GATE Current 0.1A
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per AEC-Q100-011). 1kV
Latch-up Rating (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Lead QSOP (Notes 4, 5)	88	48

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
Supply Voltage Range (Typical). . . . . 9VDC to 16VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application" schematics beginning on page 3. 9V < V_{DD} < 20V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
SUPPLY VOLTAGE					
Supply Voltage		-	-	**20**	V
Start-Up Current, I_{DD}	V_{DD} = 5.0V	-	175	**400**	µA
Operating Current, VDD 12V, I_{DD}	V_{DD} = 12V, LOAD = 0, C_{OUT} = 0	-	12	**17**	mA
UVLO START Threshold		**8.00**	8.75	**9.00**	V
UVLO STOP Threshold		**6.50**	7.00	**7.50**	V
Hysteresis		-	1.75	-	V
REFERENCE VOLTAGE					
Overall Accuracy	I_{VREF} = 0mA to 10mA	**4.78**	5.00	**5.19**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 7)	-	3	-	mV
Load Current (Sourcing)	(Note 7)	**10**	-	-	mA
Load Current (Sinking)		**3.70**	-	-	mA
Current Limit (Sourcing)	V_{REF} = 4.85V	**12**	-	**120**	mA
CURRENT SENSE					
Current Limit Threshold	VERR = V_{REF}	**0.90**	1.00	**1.14**	V
CS to OUT Delay	Excluding LEB	-	35	-	ns
Leading Edge Blanking (LEB) Duration		-	70	-	ns
CS to OUT Delay + LEB	T_A = +25°C	-	-	150	ns
CS Sink Current Device Impedance	V_{CS} = 1.1V	-	-	**20**	Ω
Input Bias Current	V_{CS} = 0.3V	**-1.0**	-	**1.0**	µA
I_{OUT} Sample and Hold Buffer Amplifier Gain	T_A = +25°C	3.85	4.00	4.15	V/V
I_{OUT} Sample and Hold VOH	V_{CS} = max, I_{source} = 300µA	**3.9**	-	-	V
I_{OUT} Sample and Hold VOL	V_{CS} = 0.00V, I_{sink} = 10µA	-	-	**0.3**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application" schematics beginning on page 3. 9V < V_{DD} < 20V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
RAMP					
RAMP Sink Current Device Impedance	V_{RAMP} = 1.1V	-	-	**20**	Ω
RAMP to PWM Comparator Offset	T_A = +25°C (Note 7)	65	80	95	mV
Bias Current (sinking)	V_{RAMP} = 0.3V	**2**	-	**5**	µA
PULSE WIDTH MODULATOR					
Minimum Duty Cycle	VERR < 0.6V (Note 7)	-	-	**0**	%
Maximum Duty Cycle (Per Half-cycle)	VERR = 4.20V, V_{CS} = 0V (Note 8)	-	94	-	%
	RTD = 2.00kΩ, CT = 220pF	-	97	-	%
	RTD = 2.00kΩ, CT = 470pF	-	99	-	%
Zero Duty Cycle VERR Voltage		**0.85**	-	**1.20**	V
VERR to PWM Comparator Input Offset	T_A = +25°C	0.7	0.8	0.9	V
VERR to PWM Comparator Input Gain		**0.31**	0.33	**0.35**	V/V
Common Mode (CM) Input Range	(Note 7)	0	-	**4.45**	V
ERROR AMPLIFIER					
Input Common Mode (CM) Range	(Note 7)	**0**	-	V_{REF}	V
GBWP	(Note 7)	**5**	-	-	MHz
VERR VOL	I_{LOAD_sink} = 2mA		0.2	**0.4**	V
VERR VOH	I_{LOAD} = 0mA	**3.8**	4.5	-	V
VERR Pull-Up Current Source (Sinking)	VERR = 2.5V	**0.8**	1.0	**1.3**	mA
EA Reference	T_A = +25°C (Note 7)	0.594	0.600	0.606	V
EA Reference + EA Input Offset Voltage		**0.590**	0.600	**0.612**	V
OSCILLATOR					
Frequency Accuracy, Overall	(Note 7)	**165**	183	**201**	kHz
		-10	-	**10**	%
Frequency Variation with V_{DD}	T_A = +25°C, (F20V- - F10V)/F10V	-	0.3	1.7	%
Temperature Stability	V_{DD} = 10V, |F-40°C - F0°C|/F0°C	-	4.5	-	%
	|F0°C - F105°C|/F25°C (Note 7)	-	1.5	-	%
Charge Current (Sourcing)	T_A = +25°C	184	200	215	µA
Discharge Current Gain		**17**	21	**24**	µA/µA
CT Valley Voltage	Static Threshold	**0.75**	0.80	**0.88**	V
CT Peak Voltage	Static Threshold	**2.73**	2.80	**2.88**	V
CT Pk-Pk Voltage	Static Value	**1.92**	2.00	**2.05**	V
RTD Voltage		**1.94**	2.00	**2.07**	V
RESDEL Voltage Range		**0**	-	**2.00**	V
CTBUF Gain ($V_{CTBUFP-P}/V_{CTP-P}$)	V_{CT} = 0.8V, 2.6V	**1.95**	2.0	**2.05**	V/V
CTBUF Offset from GND	V_{CT} = 0.8V	**0.34**	0.40	**0.45**	V
CTBUF VOH	ΔV(I_{LOAD} = 0mA, I_{LOAD} = 2mA), V_{CT} = 2.6V	-	-	**0.10**	V
CTBUF VOL	ΔV(I_{LOAD} = 2mA, I_{LOAD} = 0mA), V_{CT} = 0.8V	-	-	**0.10**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application" schematics beginning on page 3. 9V < V_{DD} < 20V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
SOFT-START					
Charging Current (Sourcing)	SS = 3V	**55**	70	**81**	µA
SS Clamp Voltage		**4.4**	4.500	**4.65**	V
SS Discharge Current	SS = 2V	**10**	30	-	mA
Reset Threshold Voltage	T_A = +25°C	0.23	0.27	0.33	V
OUTPUT					
High Level Output Voltage (VOH)	I_{OUT} = 10mA, V_{DD} - VOH	-	0.5	**1.0**	V
Low Level Output Voltage (VOL)	I_{OUT} = -10mA, VOL - GND	-	0.3	**1.0**	V
Rise Time	C_{OUT} = 220pF, V_{DD} = 15V (Note 7)	-	110	**200**	ns
Fall Time	C_{OUT} = 220pF, V_{DD} = 15V (Note 7)	-	90	**150**	ns
UVLO Output Voltage Clamp	V_{DD} = 7V, I_{LOAD} = 1mA (Note 9)	-	-	**1.25**	V
Output Delay/Advance Range OUTLLN/OUTLRN Relative to OUTLL/OUTLR	V_{ADJ} = 2.50V (Note 7)	-	2	-	ns
	V_{ADJ} < 2.425V (Note 7)	**-40**	-	**-300**	ns
	V_{ADJ} > 2.575V (Note 7)	**40**	-	**300**	ns
Delay/Advance Control Voltage Range OUTLLN/OUTLRN Relative to OUTLL/OUTLR	OUTLxN Delayed (Note 7)	**2.575**	-	**5.000**	V
	OUTLxN Advanced (Note 7)	**0**	-	**2.425**	V
V_{ADJ} Delay Time	T_A = +25°C (OUTLx Delayed) (Note 10)				
	V_{ADJ} = 0	-	300	-	ns
	V_{ADJ} = 0.5V	-	105	-	ns
	V_{ADJ} = 1.0V	-	70	-	ns
	V_{ADJ} = 1.5V	-	55	-	ns
	V_{ADJ} = 2.0V	-	50	-	ns
	T_A = +25°C (OUTLxN Delayed)				
	V_{ADJ} = V_{REF}	-	300	-	ns
	V_{ADJ} = V_{REF} - 0.5V	-	100	-	ns
	V_{ADJ} = V_{REF} - 1.0V	-	68	-	ns
	V_{ADJ} = V_{REF} - 1.5V	-	55	-	ns
	V_{ADJ} = V_{REF} - 2.0V	-	48	-	ns
THERMAL PROTECTION					
Thermal Shutdown	(Note 7)	-	140	-	°C
Thermal Shutdown Clear	(Note 7)	-	125	-	°C
Hysteresis, Internal Protection	(Note 7)	-	15	-	°C

NOTES:

7. Limits established by characterization and are not production tested.
8. This is the maximum duty cycle achievable using the specified values of RTD and CT. Larger or smaller maximum duty cycles may be obtained using other values for these components. See Equations 1 through 3.
9. Adjust V_{DD} below the UVLO stop threshold prior to setting at 7V.
10. When OUTLx is delayed relative to OUTLxN (V_{ADJ} < 2.425V), the delay duration as set by V_{ADJ} should not exceed 90% of the CT discharge time (deadtime) as determined by CT and RTD.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

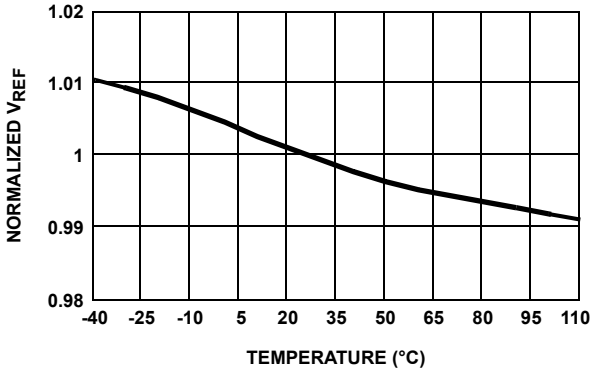


FIGURE 3. REFERENCE VOLTAGE vs TEMPERATURE

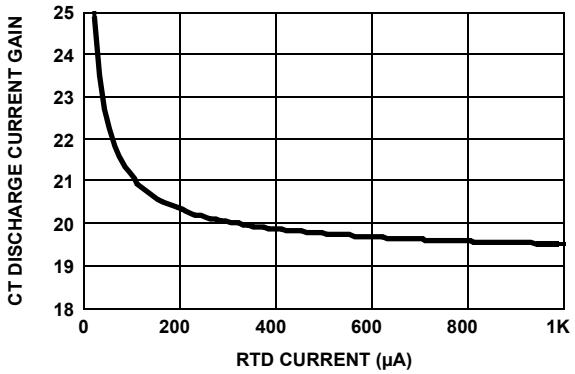


FIGURE 4. CT DISCHARGE CURRENT GAIN vs RTD CURRENT

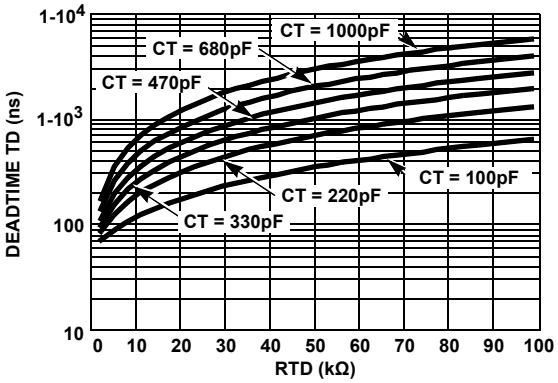


FIGURE 5. DEADTIME (DT) vs CAPACITANCE

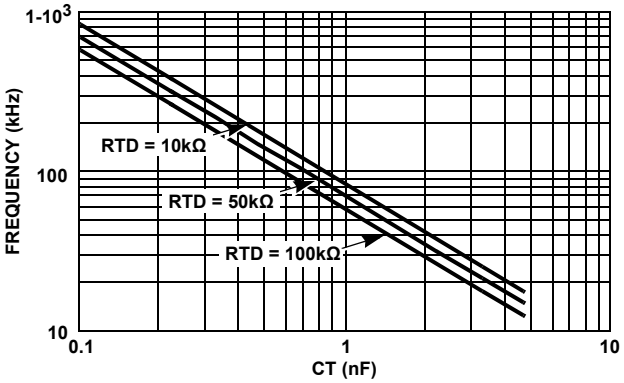


FIGURE 6. CAPACITANCE vs FREQUENCY

Functional Description

Features

The ISL78223 PWM is an excellent choice for low cost ZVS full-bridge applications requiring adjustable synchronous rectifier drive. With its many protection and control features, a highly flexible design with minimal external components is possible. Among its many features are a very accurate overcurrent limit threshold, thermal protection, a buffered sawtooth oscillator output suitable for slope compensation, synchronous rectifier outputs with variable delay/advance timing, and adjustable frequency.

Oscillator

The ISL78223 has an oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor and capacitor.

The switching period is the sum of the timing capacitor charge and discharge durations. The charge duration is determined by CT and a fixed 200µA internal current source. The discharge duration is determined by RTD and CT.

$$t_C \approx 11.5 \cdot 10^3 \cdot CT \quad S \qquad \text{(EQ. 1)}$$

$$t_D \approx (0.06 \cdot RTD \cdot CT) + 50 \cdot 10^{-9} \quad S \qquad \text{(EQ. 2)}$$

$$t_{SW} = T_C + T_D = \frac{1}{F_{SW}} \quad S \qquad \text{(EQ. 3)}$$

where t_C and t_D are the charge and discharge times, respectively, CT is the timing capacitor in Farads, RTD is the discharge programming resistance in ohms, t_{SW} is the oscillator period, and F_{SW} is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay adds directly to the switching duration, but also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very small discharge currents are used, there will be increased error due to the input impedance at the CT pin. The maximum recommended current through RTD is 1mA, which produces a CT discharge current of 20mA.

The maximum duty cycle, D, and percent deadtime, DT, can be calculated from:

$$D = \frac{T_C}{t_{SW}} \qquad \text{(EQ. 4)}$$

$$DT = 1 - D \qquad \text{(EQ. 5)}$$

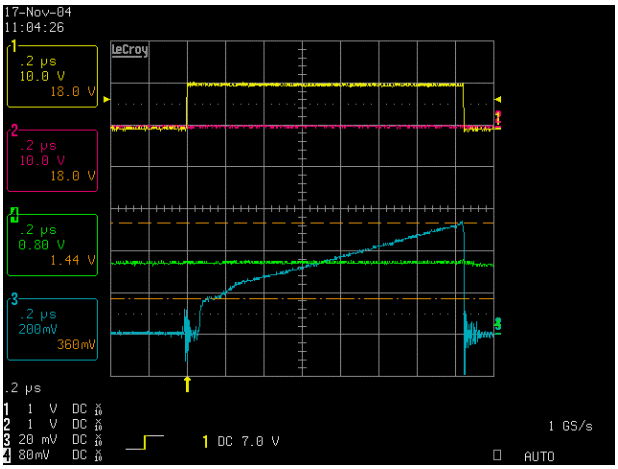
Overcurrent Operation

Two overcurrent protection mechanisms are available to the power supply designer. The first method is cycle-by-cycle peak overcurrent protection which provides fast response. The cycle-by-cycle peak current limit results in pulse-by-pulse duty cycle reduction when the current feedback signal exceeds 1.0V. When the peak current exceeds the threshold, the active output pulse is immediately terminated. This results in a decrease in output voltage as the load current increases beyond the current limit threshold. The ISL78223 operates continuously in an overcurrent condition without shutdown.

The second method is a slower, averaging method which produces constant or “brick-wall” current limit behavior. If voltage mode control is used, the average overcurrent protection also maintains flux balance in the transformer by maintaining duty cycle symmetry between half-cycles. If voltage mode control is used in a bridge topology, it should be noted that peak current limit results in inherently unstable operation. The DC blocking capacitors used in voltage mode bridge topologies become unbalanced, as does the flux in the transformer core. Average current limit will prevent the instability and allow continuous operation in current limit provided the control loop is designed with adequate bandwidth.

The propagation delay from CS exceeding the current limit threshold to the termination of the output pulse is increased by the leading edge blanking (LEB) interval. The effective delay is the sum of the two delays and is nominally 105ns.

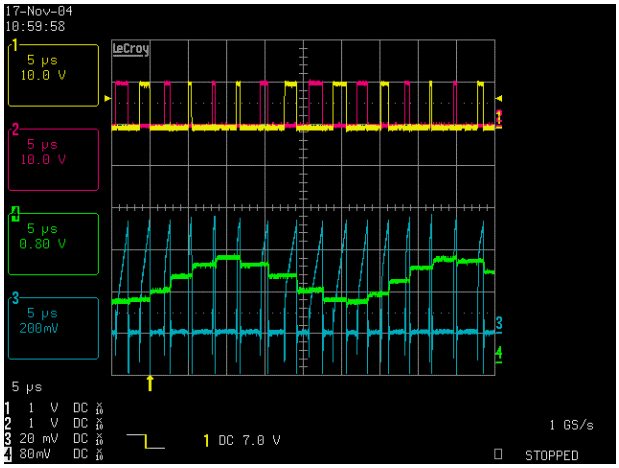
The current sense signal applied to the CS pin connects to the peak current comparator and a sample and hold averaging circuit. After a 70ns leading edge blanking (LEB) delay, the current sense signal is actively sampled during the on time, the average current for the cycle is determined, and the result is amplified by 4x and output on the IOUT pin. If an RC filter is placed on the CS input, its time constant should not exceed ~50ns or significant error may be introduced on I_{OUT}.



CHANNEL 1 (YELLOW): OUTLL CHANNEL 2 (RED): OUTLR
CHANNEL 3 (BLUE): CS CHANNEL 4 (GREEN): IOUT

FIGURE 7. CS INPUT vs I_{OUT}

Figure 7 shows the relationship between the CS signal and I_{OUT} under steady state conditions. The I_{OUT} is 4x the average of CS. Figure 8 shows the dynamic behavior of the current averaging circuitry when CS is modulated by an external sine wave. Notice I_{OUT} is updated by the sample and hold circuitry at the termination of the active output pulse.



CHANNEL 1 (YELLOW): OUTLL CHANNEL 2 (RED): OUTLR
CHANNEL 3 (BLUE): CS CHANNEL 4 (GREEN): I_{OUT}

FIGURE 8. DYNAMIC BEHAVIOR OF CS vs I_{OUT}

The average current signal on I_{OUT} remains accurate provided the output inductor current remains continuous (CCM operation). Once the inductor current becomes discontinuous (DCM operation), I_{OUT} represents 1/2 the peak inductor current rather than the average current. This occurs because the sample and hold circuitry is active only during the on time of the switching cycle. It is unable to detect when the inductor current reaches zero during the off time.

If average overcurrent limit is desired, I_{OUT} may be used with the error amplifier of the ISL78223. Typically I_{OUT} is divided down and filtered as required to achieve the desired amplitude. The resulting signal is input to the current error amplifier (IEA). The IEA is similar to the voltage EA found in most PWM controllers, except it cannot source current. Instead, VERR has a separate internal 1mA pull-up current source.

Configure the IEA as an integrating (Type I) amplifier using the internal 0.6V reference. The voltage applied at FB is integrated against the 0.6V reference. The resulting signal, VERR, is applied to the PWM comparator where it is compared to the sawtooth voltage on RAMP. If FB is less than 0.6V, the IEA will be open loop (can not source current), VERR will be at a level determined by the voltage loop, and the duty cycle is unaffected. As the output load increases, I_{OUT} will increase, and the voltage applied to FB will increase until it reaches 0.6V. At this point the IEA will reduce VERR as required to maintain the output current at the level that corresponds to the 0.6V reference. When the output current again drops below the average current limit threshold, the IEA returns to an open loop condition, and the duty cycle is again controlled by the voltage loop.

The average current control loop behaves much the same as the voltage control loop found in typical power supplies except it regulates current rather than voltage.

The EA available on the ISL78223 may also be used as the voltage EA for the voltage feedback control loop rather than the current EA as described above. An external op-amp may be used as either the current or voltage EA providing the circuit is not allowed to source current into VERR. The external EA must only sink current, which may be accomplished by adding a diode in series with its output.

The 4x gain of the sample and hold buffer allows a range of 150mV to 1000mV peak on the CS signal, depending on the resistor divider placed on I_{OUT}. The overall bandwidth of the average current loop is determined by the integrating current EA compensation and the divider on I_{OUT}.

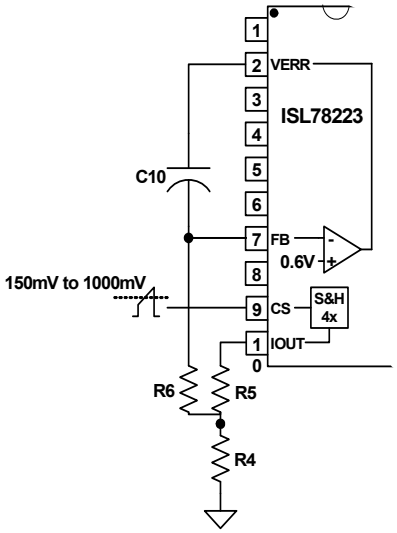


FIGURE 9. AVERAGE OVERCURRENT IMPLEMENTATION

The current EA crossover frequency, assuming R6 >> (R4||R5), is:

$$f_{CO} = \frac{1}{2\pi \cdot R6 \cdot C10} \quad Hz \qquad \text{(EQ. 6)}$$

where f_{CO} is the crossover frequency. A capacitor in parallel with R4 may be used to provide a double-pole roll-off.

The average current loop bandwidth is normally set to be much less than the switching frequency, typically less than 5kHz and often as slow as a few hundred hertz or less. This is especially useful if the application experiences large surges. The average current loop can be set to the steady state overcurrent threshold and have a time response that is longer than the required transient. The peak current limit can be set higher than the expected transient so that it does not interfere with the transient, but still protects for short-term larger faults. In essence a 2-stage overcurrent response is possible.

The peak overcurrent behavior is similar to most other PWM controllers. If the peak current exceeds 1.0V, the active output pulse is terminated immediately.

If voltage mode control is used in a bridge topology, it should be noted that peak current limit results in inherently unstable operation. DC blocking capacitors used in voltage mode bridge topologies become unbalanced, as does the flux in the transformer core. The average overcurrent circuitry prevents this behavior by maintaining symmetric duty cycles for each half-cycle. If the average current limit circuitry is not used, a latching overcurrent shutdown method using external components is recommended.

The CS to output propagation delay is increased by the leading edge blanking (LEB) interval. The effective delay is the sum of the two delays and is 130ns maximum.

Voltage Feed-Forward Operation

Voltage feed-forward is a technique used to regulate the output voltage for changes in input voltage without the intervention of the control loop. Voltage feed-forward is implemented in voltage mode control loops, but is redundant and unnecessary in peak current mode control loops.

Voltage feed-forward operates by modulating the sawtooth ramp in direct proportion to the input voltage. Figure 10 demonstrates the concept.

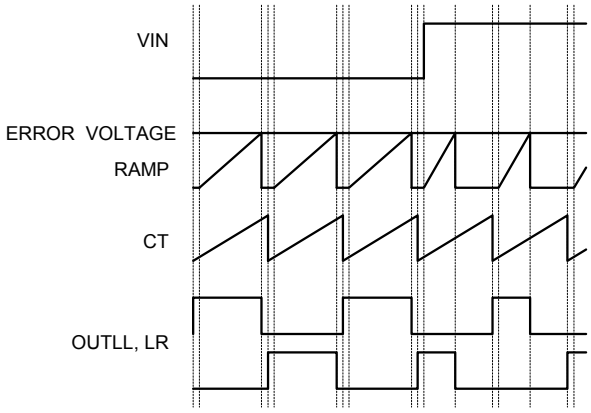


FIGURE 10. VOLTAGE FEED-FORWARD BEHAVIOR

Input voltage feed-forward may be implemented using the RAMP input. An RC network connected between the input voltage and ground, as shown in Figure 11, generates a voltage ramp whose charging rate varies with the amplitude of the source voltage. At the termination of the active output pulse, the RAMP is discharged to ground so, that a repetitive sawtooth waveform is created. The RAMP waveform is compared to the VERR voltage to determine duty cycle. The selection of the RC components depends upon the desired input voltage operating range and the frequency of the oscillator. In typical applications, the RC components are selected so, that the ramp amplitude reaches 1V at minimum input voltage within the duration of one half-cycle.

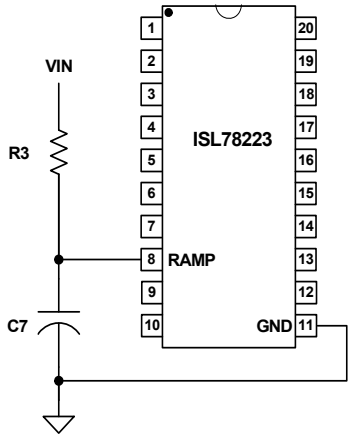


FIGURE 11. VOLTAGE FEED-FORWARD CONTROL

The charging time of the ramp capacitor is:

$$t = -R3 \cdot C7 \cdot \ln\left(1 - \frac{V_{RAMP(PEAK)}}{V_{IN(MIN)}}\right) \quad S \qquad \text{(EQ. 7)}$$

For optimum performance, the maximum value of the capacitor should be limited to 10nF. The maximum DC current through the resistor should be limited to 2mA maximum. For example, if the oscillator frequency is 400kHz, the minimum input voltage is 300V, and a 4.7nF ramp capacitor is selected, the value of the resistor can be determined by rearranging Equation 8.

$$R3 = \frac{-t}{C7 \cdot \ln\left(1 - \frac{V_{RAMP(PEAK)}}{V_{IN(MIN))}}\right)} = \frac{-2.5 \cdot 10^{-6}}{4.7 \cdot 10^{-9} \cdot \ln\left(1 - \frac{1}{300}\right)}$$

$$= 159 \quad k\Omega \qquad \text{(EQ. 8)}$$

where t is equal to the oscillator period minus the deadtime. If the deadtime is short relative to the oscillator period, it can be ignored for this calculation.

If feed-forward operation is not desired, the RC network may be connected to V_{REF} rather than the input voltage. Alternatively, a resistor divider from CTBUF may be used as the sawtooth signal. Regardless, a sawtooth waveform must be generated on RAMP as it is required for proper PWM operation.

Gate Drive

The ISL78223 outputs are capable of sourcing and sinking 10mA (at rated VOH, VOL) and are intended to be used in conjunction with integrated FET drivers or discrete bipolar totem pole drivers. The typical on resistance of the outputs is 50Ω.

Slope Compensation

Peak current mode control requires slope compensation to improve noise immunity, particularly at lighter loads, and to prevent current loop instability, particularly for duty cycles greater than 50%. Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation, is:

$$Fm = \frac{1}{Sntsw} \qquad \text{(EQ. 9)}$$

where Sn is the slope of the sawtooth signal and tsw is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes:

$$Fm = \frac{1}{(Sn + Se)tsw} = \frac{1}{m_c Sntsw} \qquad \text{(EQ. 10)}$$

where Se is slope of the external ramp and

$$m_c = 1 + \frac{Se}{Sn} \qquad \text{(EQ. 11)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at half the oscillator frequency. The double-pole will be critically damped if the Q-factor is set to 1, and over-damped for Q > 1, and under-damped for Q < 1. An under-damped condition can result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D)-0.5)} \quad \text{(EQ. 12)}$$

where D is the percent of on time during a half cycle. Setting Q = 1 and solving for S_e yields:

$$S_e = S_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 13)}$$

Since S_n and S_e are the on time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

$$V_e = V_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 14)}$$

where V_n is the change in the current feedback signal during the on time and V_e is the voltage that must be added by the external ramp.

V_n can be solved for in terms of input voltage, current transducer components, and output inductance yielding:

$$V_e = \frac{t_{SW}\cdot V_O \cdot R_{CS}}{N_{CT}\cdot L_O}\cdot\frac{N_S}{N_P}\left(\frac{1}{\pi}+D-0.5\right) \quad V \quad \text{(EQ. 15)}$$

where R_{CS} is the current sense burden resistor, N_{CT} is the current transformer turns ratio, L_O is the output inductance, V_O is the output voltage, and N_S and N_P are the secondary and primary turns, respectively.

The inductor current, when reflected through the isolation transformer and the current sense transformer to obtain the current feedback signal at the sense resistor yields:

$$V_{CS} = \frac{N_S\cdot R_{CS}}{N_P\cdot N_{CT}}\left(I_O+\frac{D\cdot t_{SW}}{2L_O}\left(V_{IN}\cdot\frac{N_S}{N_P}-V_O\right)\right) \quad V \quad \text{(EQ. 16)}$$

where V_{CS} is the voltage across the current sense resistor and I_O is the output current at current limit.

Since the peak current limit threshold is 1V, the total current feedback signal plus the external ramp voltage must sum to this value.

$$V_e + V_{CS} = 1 \quad \text{(EQ. 17)}$$

Substituting Equations 15 and 16 into Equation 17 and solving for R_{CS} yields:

$$R_{CS} = \frac{N_P\cdot N_{CT}}{N_S}\cdot\frac{1}{I_O+\frac{V_O}{L_O}t_{SW}\left(\frac{1}{\pi}+\frac{D}{2}\right)} \quad \Omega \quad \text{(EQ. 18)}$$

For simplicity, idealized components have been used for this discussion, but the effect of magnetizing inductance must be considered when determining the amount of external ramp to add. Magnetizing inductance provides a degree of slope compensation to the current feedback signal and reduces the amount of external ramp required. The magnetizing inductance adds primary current in excess of what is reflected from the inductor current in the secondary.

$$\Delta I_P = \frac{V_{IN}\cdot Dt_{SW}}{L_m} \quad A \quad \text{(EQ. 19)}$$

where V_{IN} is the input voltage that corresponds to the duty cycle D and L_m is the primary magnetizing inductance. The effect of the magnetizing current at the current sense resistor, R_{CS}, is:

$$\Delta V_{CS} = \frac{\Delta I_P\cdot R_{CS}}{N_{CT}} \quad V \quad \text{(EQ. 20)}$$

If ΔV_{CS} is greater than or equal to V_e, then no additional slope compensation is needed and R_{CS} becomes:

$$R_{CS} = \frac{N_{CT}}{\frac{N_S}{N_P}\cdot\left(I_O+\frac{Dt_{SW}}{2L_O}\cdot\left(V_{IN}\cdot\frac{N_S}{N_P}-V_O\right)\right)+\frac{V_{IN}\cdot Dt_{SW}}{L_m}} \quad \text{(EQ. 21)}$$

If ΔV_{CS} is less than Ve, then Equation 16 is still valid for the value of R_{CS}, but the amount of slope compensation added by the external ramp must be reduced by ΔV_{CS}.

Adding slope compensation may be accomplished in the ISL78223 using the CTBUF signal. The CTBUF is an amplified representation of the sawtooth signal that appears on the CT pin. It is offset from ground by 0.4V and is 2x the peak-to-peak amplitude of CT (0.4V to 4.4V). A typical application sums this signal with the current sense feedback and applies the result to the CS pin as shown in Figure 12.

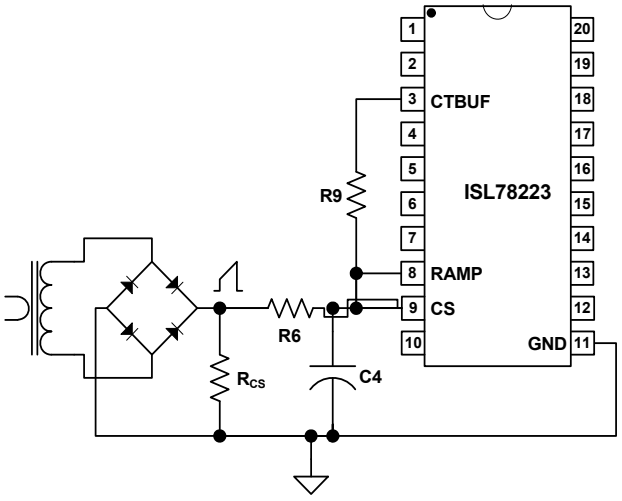


FIGURE 12. ADDING SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter placed on the CS pin, the value of R9 required to add the appropriate external ramp can be found by superposition.

$$V_e - \Delta V_{CS} = \frac{(D(V_{CTBUF}-0.4)+0.4)\cdot R6}{R6+R9} \quad V \quad \text{(EQ. 22)}$$

Rearranging to solve for R9 yields:

$$R9 = \frac{(D(V_{CTBUF} - 0.4) - V_e + \Delta V_{CS} + 0.4) \cdot R6}{V_e - \Delta V_{CS}} \quad \Omega \qquad \text{(EQ. 23)}$$

The value of R_{CS} determined in Equations 18 or 21 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 16. The divider created by R6 and R9 makes this necessary.

$$R'_{CS} = \frac{R6 + R9}{R9} \cdot R_{CS} \qquad \text{(EQ. 24)}$$

Example:

V_{IN} = 280V

V_O = 12V

L_O = 2.0µH

Np/Ns = 20

Lm = 2mH

I_O = 55A

Oscillator Frequency, Fsw = 400kHz

Duty Cycle, D = 85.7%

N_{CT} = 50

R6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equations 18.

R_{CS} = 15.1Ω.

Determine the amount of voltage, V_e, that must be added to the current feedback signal using Equation 15.

Ve = 153mV

Next, determine the effect of the magnetizing current from Equation 20.

ΔV_{CS} = 91mV

Using Equation 23, solve for the summing resistor, R9, from CTBUF to CS.

R9 = 30.1kΩ

Determine the new value of R_{CS}, R'_{CS}, using Equation 24.

R'_{CS} = 15.4Ω

The above discussion determines the minimum external ramp that is required. Additional slope compensation may be considered for design margin.

If the application requires deadtime less than about 500ns, the CTBUF signal may not perform adequately for slope compensation. The CTBUF lags the CT sawtooth waveform by 300ns to 400ns. This behavior results in a non-zero value of the CTBUF when the next half-cycle begins when the deadtime is short.

Under these situations, slope compensation may be added by externally buffering the CT signal as shown in Figure 13.

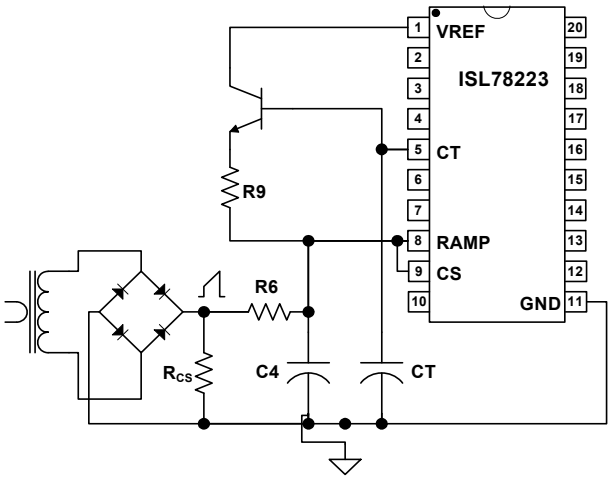


FIGURE 13. ADDING SLOPE COMPENSATION USING CT

Using CT to provide slope compensation instead of CTBUF requires the same calculations, except that Equations 22 and 23 require modification. Equation 22 becomes:

$$V_e - \Delta V_{CS} = \frac{2D \cdot R6}{R6 + R9} \quad V \qquad \text{(EQ. 25)}$$

and Equation 23 becomes:

$$R9 = \frac{(2D - V_e + \Delta V_{CS}) \cdot R6}{V_e - \Delta V_{CS}} \quad \Omega \qquad \text{(EQ. 26)}$$

The buffer transistor used to create the external ramp from CT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into CT and will reduce the oscillator frequency.

ZVS Full-Bridge Operation

The ISL78223 is a full-bridge zero voltage switching (ZVS) PWM controller that behaves much like a traditional hard-switched topology controller. Rather than drive the diagonal bridge switches simultaneously, the upper switches (OUTUL, OUTUR) are driven at a fixed 50% duty cycle and the lower switches (OUTLL, OUTLR) are pulse width modulated on the trailing edge.

To understand how the ZVS method operates, one must include the parasitic elements of the circuit and examine a full switching cycle.

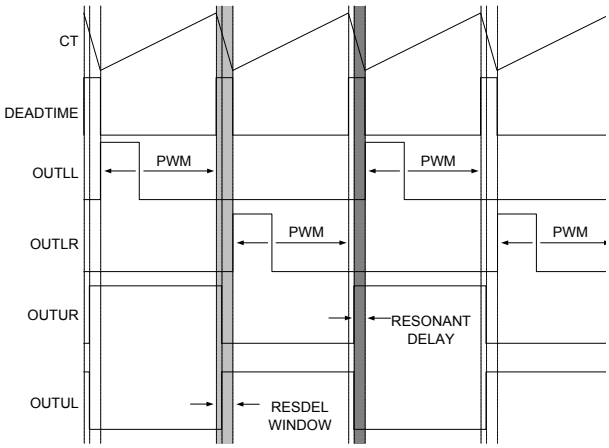


FIGURE 14. BRIDGE DRIVE SIGNAL TIMING

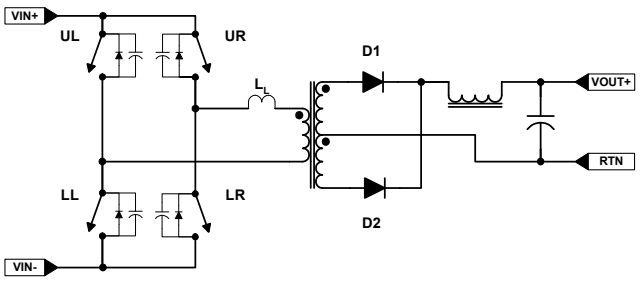


FIGURE 15. IDEALIZED FULL-BRIDGE

In Figure 15, the power semiconductor switches have been replaced by ideal switch elements with parallel diodes and capacitance, the output rectifiers are ideal, and the transformer leakage inductance has been included as a discrete element. The parasitic capacitance has been lumped together as switch capacitance, but represents all parasitic capacitance in the circuit including winding capacitance. Each switch is designated by its position, upper left (UL), upper right (UR), lower left (LL) and lower right (LR). The beginning of the cycle, shown in Figure 16, is arbitrarily set as having switches UL and LR on and UR and LL off. The direction of the primary and secondary currents are indicated by I_P and I_S, respectively.

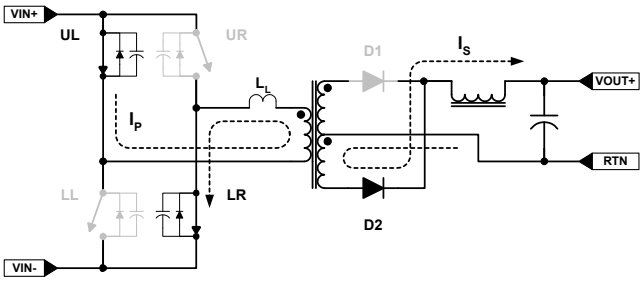


FIGURE 16. UL - LR POWER TRANSFER CYCLE

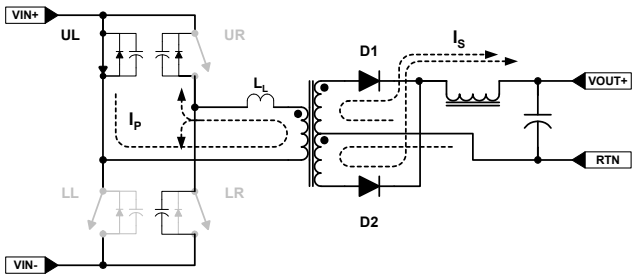


FIGURE 17. UL - UR FREE-WHEELING PERIOD

The UL - LR power transfer period terminates when switch LR turns off as determined by the PWM. The current flowing in the primary cannot be interrupted instantaneously, so it must find an alternate path. The current flows into the parasitic switch capacitance of LR and UR, which charges the node to VIN and then forward biases the body diode of upper switch UR.

The primary leakage inductance, L_L, maintains the current which now circulates around the path of switch UL, the transformer primary, and switch UR. When switch LR opens, the output inductor current free-wheels through both output diodes, D1 and D2. During the switch transition, the output inductor current assists the leakage inductance in charging the upper and lower bridge FET capacitance.

The current flow from the previous power transfer cycle tends to be maintained during the free-wheeling period because the transformer primary winding is essentially shorted. Diode D1 may conduct very little or none of the free-wheeling current, depending on circuit parasitics. This behavior is quite different than what occurs in a conventional hard-switched full-bridge topology where the free-wheeling current splits nearly evenly between the output diodes, and flows not at all in the primary. This condition persists through the remainder of the half-cycle. During the period when CT discharges, also referred to as the deadtime, the upper switches toggle. Switch UL turns off and switch UR turns on. The actual timing of the upper switch toggle is dependent on RESDEL which sets the resonant delay. The voltage applied to RESDEL determines how far in advance the toggle occurs prior to a lower switch turning on. The ZVS transition occurs after the upper switches toggle and before the diagonal lower switch turns on. The required resonant delay is 1/4 of the period of the LC resonant frequency of the circuit formed by the leakage inductance and the parasitic capacitance. The resonant transition may be estimated from Equation 27.

$$\tau = \frac{\pi}{2}\frac{1}{\sqrt{\frac{1}{L_L C_P} - \frac{R^2}{4L_L^2}}} \quad \text{(EQ. 27)}$$

where τ is the resonant transition time, L_L is the leakage inductance, C_P is the parasitic capacitance, and R is the equivalent resistance in series with L_L and C_P.

The resonant delay is always less than or equal to the deadtime and may be calculated using Equation 28.

$$\tau_{resdel} = \frac{V_{resdel}}{2} \cdot DT \quad S \qquad \text{(EQ. 28)}$$

where τ_{resdel} is the desired resonant delay, V_{resdel} is a voltage between 0V and 2V applied to the RESDEL pin, and DT is the deadtime (see Equations 1 through 5).

When the upper switches toggle, the primary current that was flowing through UL must find an alternate path. It charges/discharges the parasitic capacitance of switches UL and LL until the body diode of LL is forward biased. If RESDEL is set properly, switch L_L will be turned on at this time. The output inductor does not assist this transition. It is purely a resonant transition driven by the leakage inductance.

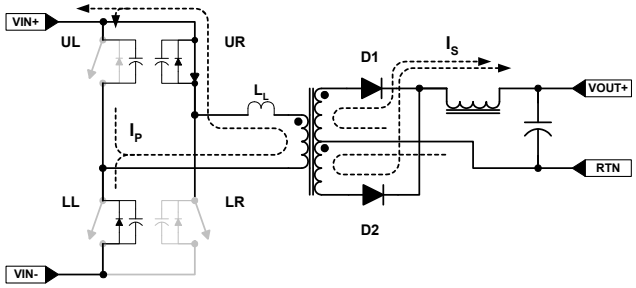


FIGURE 18. UPPER SWITCH TOGGLE AND RESONANT TRANSITION

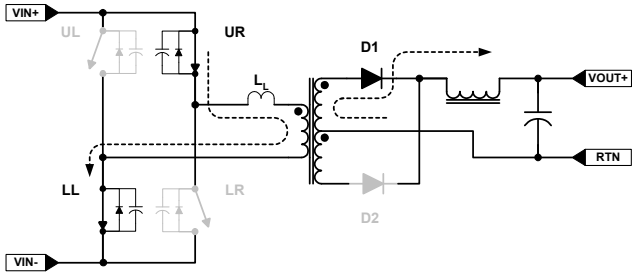


FIGURE 19. UR - LL POWER TRANSFER CYCLE

The second power transfer period commences when switch LL closes. With switches UR and L_L on, the primary and secondary currents flow as indicated in Figure 19.

The UR - LL power transfer period terminates when switch LL turns off as determined by the PWM. The current flowing in the primary must find an alternate path. The current flows into the parasitic switch capacitance which charges the node to V_{IN} and then forward biases the body diode of upper switch UL. As before, the output inductor current assists in this transition. The primary leakage inductance, L_L, maintains the current, which now circulates around the path of switch UR, the transformer primary, and switch UL. When switch L_L opens, the output inductor current free-wheels predominantly through diode D1. Diode D2 may actually conduct very little or none of the free wheeling current, depending on circuit parasitics. This condition persists through the remainder of the half-cycle.

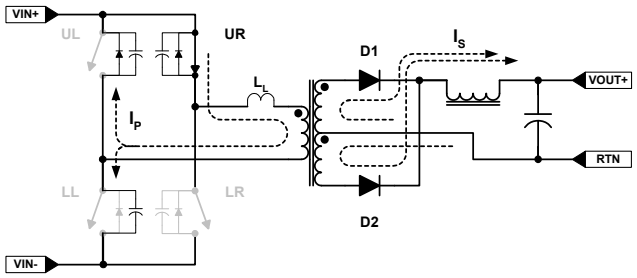


FIGURE 20. UR - UL FREE-WHEELING PERIOD

When the upper switches toggle, the primary current that was flowing through UR must find an alternate path. It charges/discharges the parasitic capacitance of switches UR and LR until the body diode of LR is forward biased. If RESDEL is set properly, switch LR will be turned on at this time.

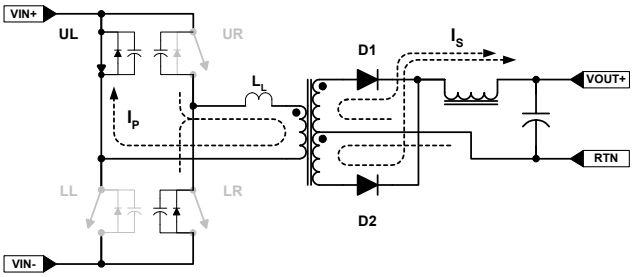


FIGURE 21. UPPER SWITCH TOGGLE AND RESONANT TRANSITION

The first power transfer period commences when switch LR closes and the cycle repeats. The ZVS transition requires that the leakage inductance has sufficient energy stored to fully charge the parasitic capacitances. Since the energy stored is proportional to the square of the current ($1/2\ L_L I_P^2$), the ZVS resonant transition is load dependent. If the leakage inductance is not able to store sufficient energy for ZVS, a discrete inductor may be added in series with the transformer primary.

Synchronous Rectifier Outputs and Control

The ISL78223 provides double-ended PWM outputs, OUTLL and OUTLR, and synchronous rectifier (SR) outputs, OUTLLN and OUTLRN. The SR outputs are the complements of the PWM outputs. It should be noted that the complemented outputs are used in conjunction with the opposite PWM output, i.e., the OUTLL and OUTLRN are paired together, the OUTLR and OUTLLN are paired together.

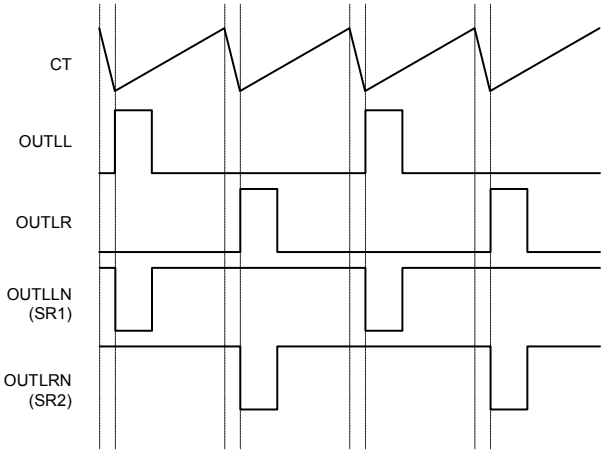


FIGURE 22. BASIC WAVEFORM TIMING

Referring to Figure 22, the SRs alternate between being both on during the free-wheeling portion of the cycle (OUTLL/LR off), and one or the other being off when OUTLL or OUTLR is on. If OUTLL is on, its corresponding SR must also be on, indicating that OUTLRN is the correct SR control signal. Likewise, if OUTLR is on, its corresponding SR must also be on, indicating that OUTLLN is the correct SR control signal.

A useful feature of the ISL78223 is the ability to vary the phase relationship between the PWM outputs (OUTLL, OUT LR) and the their complements (OUTLLN, OUTLRN) by ±300ns. This feature allows the designer to compensate for differences in the propagation times between the PWM FETs and the SR FETs. A voltage applied to V_{ADJ} controls the phase relationship.

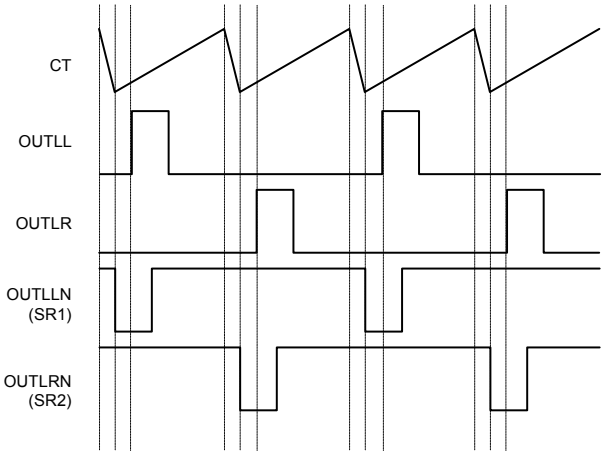


FIGURE 23. WAVEFORM TIMING WITH PWM OUTPUTS DELAYED, 0V < V_{ADJ} < 2.425V

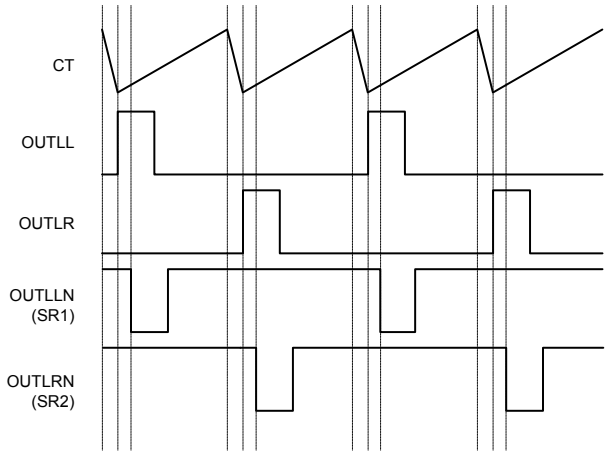


FIGURE 24. WAVEFORM TIMING WITH SR OUTPUTS DELAYED, 2.575V < V_{ADJ} < 5.00V

Setting V_{ADJ} to $V_{REF}/2$ results in no delay on any output. The no delay voltage has a ±75mV tolerance window. Control voltages below the $V_{REF}/2$ zero delay threshold cause the PWM outputs, OUTLL/OUTLR, to be delayed. Control voltages greater than the $V_{REF}/2$ zero delay threshold cause the SR outputs, OUTLLN/OUTLRN, to be delayed. It should be noted that when the PWM outputs, OUTLL/OUTLR, are delayed, the CS to output propagation delay is increased by the amount of the added delay.

The delay feature is provided to compensate for mismatched propagation delays between the PWM and SR outputs as may be experienced when one set of signals crosses the primary-secondary isolation boundary. If required, individual output pulses may be stretched or compressed as required using external resistors, capacitors, and diodes. When the PWM outputs are delayed, the 50% upper outputs are equally delayed, so the resonant delay setting is unaffected.

On/Off Control

The ISL78223 does not have a separate enable/disable control pin. The PWM outputs, OUTLL/OUTLR, may be disabled by pulling VERR to ground. Doing so reduces the duty cycle to zero, but the upper 50% duty cycle outputs, OUTUL/OUTUR, will continue operation. Likewise, the SR outputs OUTLLN/OUTLRN will be active high. Pulling Soft-Start to ground will disable all outputs and set them to a low condition.

Fault Conditions

A fault condition occurs if V_{REF} or V_{DD} fall below their undervoltage lockout (UVLO) thresholds or if the thermal protection is triggered. When a fault is detected the outputs are disabled low. When the fault condition clears the outputs are re-enabled. An overcurrent condition is not considered a fault and does not result in a shutdown.

Thermal Protection

Internal die over temperature protection is provided. An integrated temperature sensor protects the device should the junction temperature exceed +140°C. There is approximately +15°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} and V_{REF} should be bypassed directly to GND with good high frequency capacitance.

References

[1] Ridley, R., "A New Continuous-Time Model for Current Mode Control", IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 20, 2014	FN7936.3	Removed "AEC Q100 qualified" from the Features section on page 1. Removed "The ISL78223 is AEC Q100 rated." from page 1. "Absolute Maximum Ratings" on page 7: Updated CDM testing from: Charged Device Model (Tested per JESD22-C101E) to Charged Device Model (Tested per AEC Q100-011).
December 7, 2013	FN7936.2	page 19 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted"
January 2, 2013	FN7936.1	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

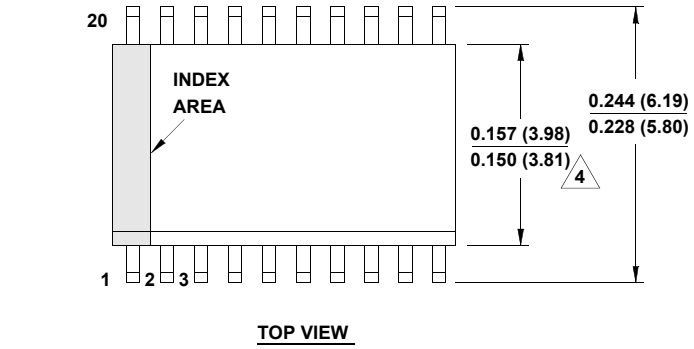
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

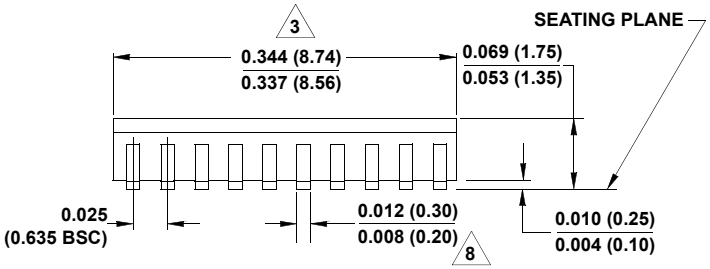
Package Outline Drawing

M20.15

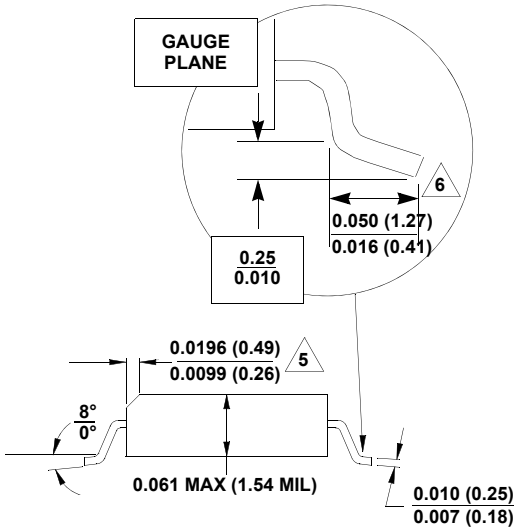
20 LEAD QUARTER SIZE OUTLINE PLASTIC PACKAGE (QSOP)
Rev 2, 1/11



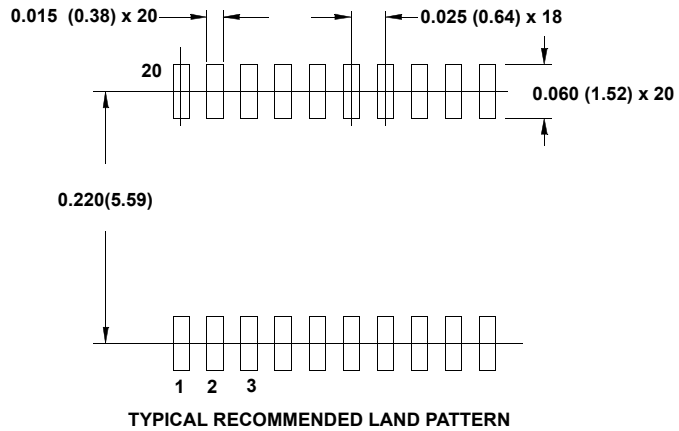
TOP VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Length of terminal for soldering to a substrate.
7. Terminal numbers are shown for reference only.
8. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of dimension at maximum material condition.
9. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.