IGLOO FPGAs

Smallest Size | Single Chip | Flash*Freeze | 1.2 V | 2 µW

The Industry's Lowest Power FPGAs

Microsemi

IGLOO FPGAs

The IGLOO families, which include IGLOO/e, IGLOO nano, and IGLOO PLUS devices, are reprogrammable, full-featured flash FPGAs designed to meet the demanding power and area requirements of today's portable and power-conscious electronics. Based on non-volatile flash technology and single-chip ProASIC®3 FPGA architecture, the 1.2 V to 1.5 V operating voltage family offers the industry's lowest power consumption at competitive prices with many devices under $0.99.

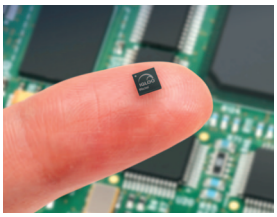
Flash*Freeze technology used in IGLOO devices enables easy entry to and exit from ultra-low-power mode, which consumes as little as 2 µW, while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. The Microsemi IGLOO families supports secure in-system reprogrammability, which allows quick and easy upgrades or design updates in the final stages of manufacturing or in the field.

The IGLOO families support up to 3 million system gates with up to 504 kbits of true dual-port SRAM, up to 6 embedded PLLs, and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the ARM Cortex-M1 processor without license fee or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 offers an optimal balance between performance and size to minimize power consumption.

Key Benefits

- **Flash*Freeze Ultra-low Power (from 2 µW) while Maintaining FPGA Content**
- **1.2 V to 1.5 V Core and I/O Voltage Minimizes Static and Active Power Consumption**
- **Supports ARM® Cortex™-M1**
- **True Single Chip and Small Form Factor for Space-constrained Applications**
- **Full-featured FPGA with On-chip Nonvolatile Memory, SRAM, and PLLs**
- **Comprehensive I/O Offering with High I/O per Area and Logic Ratios**
- **Secure In-System Programmability**

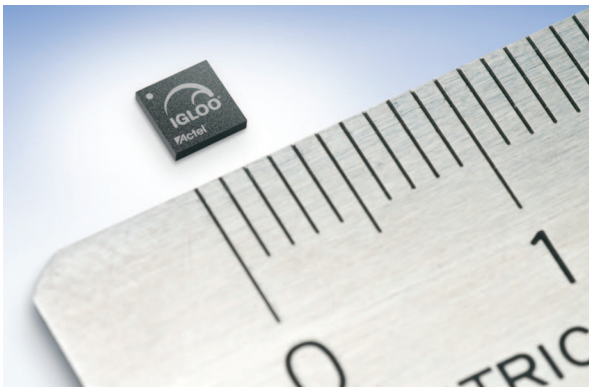
IGLOO nano — Industry's Lowest Power and Smallest Size FPGAs



Microsemi's IGLOO nano products offer the largest selection of small-footprint packages with six distinctive packages at 8x8 mm or less, including the industry's smallest 3x3 mm micro chip scale package. Small size combined with the lowest-power FPGA available, starting at just 2 µW, opens new opportunities for designers of battery-powered and handheld applications.

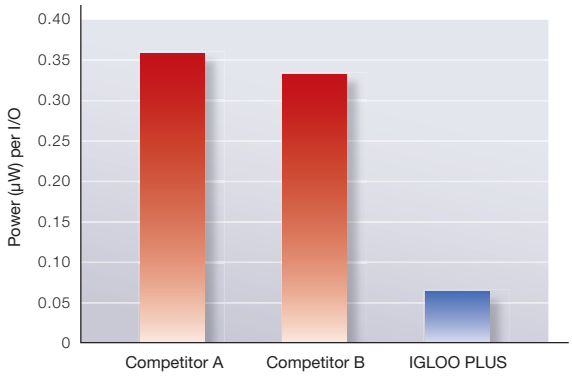
Available in logic densities from 10 k to 250 k gates, the 1.2 V to 1.5 V IGLOO nano devices have been designed for consumer, industrial, medical, and other high-volume, cost-sensitive applications where power and size are key decision criteria and market differentiators. IGLOO nano devices are ideal for independent level shifting to enable support for varying voltage levels, for I/O expansion or multiplexing, for adapting to changing standards, and when embedded security is required to ensure fidelity of valuable Intellectual Property. Priced competitively in the market, IGLOO nano devices are perfect ASIC or ASSP replacements yet retain the historical FPGA advantages of flexibility and quick time-to- market in low-power and small-footprint profiles.

IGLOO PLUS and IGLOO nano devices support Flash*Freeze bus hold, which allows users to hold the I/O states while in Flash*Freeze mode—a capability that is necessary in applications such as smartphones, wireless audio, and video equipment. Additionally, both IGLOO PLUS and IGLOO nano devices support Schmitt trigger inputs and are hot-swappable. The Schmitt trigger input delivers greater noise immunity in the circuit, enabling designers to safely identify an input signal that rises slowly, such as a keyboard or touchpad. The hot-swap capability offers designers the flexibility to maintain direct system connection while powering up.



IGLOO PLUS—Ultra-Low-Power FPGAs with Enhanced I/O Capabilities

Today's highly competitive market demands devices that consume minimum power and offer differentiating features at a competitive price. Responding to the challenge, IGLOO PLUS family delivers unrivaled low-power options and I/O features in a feature-rich programmable device. Starting at 5 µW, IGLOO PLUS devices are the best low-power solution for I/O-intensive applications employing memory bus manipulation, general-purpose I/O expansion, sequencing, interface translation, storage, and human interface touch screens and keypads.



Ranging from 30 k to 125 k gates, the 1.2 V to 1.5 V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive power-conscious applications that require exceptional features. These area- and cost-effective devices offer four I/O banks for independent level shifting to enable support for varying voltage levels, a feature that bridges the gap between application processors and application-specific standard products (ASSPs) in which differing I/O standards and voltages may be utilized.

Lowest Power Devices

Three Low-Power Capabilities

The IGLOO families are designed to maximize usable power in many different ways. In Flash*Freeze mode, power drops to as low as 2 µW, and no additional components are required to turn off I/Os or clocks while preserving the design information, SRAM content, and registers. I/Os can maintain their state during Flash*Freeze mode. Entering and exiting Flash*Freeze mode takes less than 1 µs.

Additionally, the Low-Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO device is completely functional in the system, maintaining I/Os, SRAM, registers, and logic functions. This allows the IGLOO device to control the system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

In Sleep mode, larger IGLOO FPGAs experience maximum power savings when the FPGA core voltage is powered down. The unique Level 0 instant-on capability of flash devices allows for rapid system wake-up from Sleep mode.

IGLOO FPGAs are 1.2 V low-power programmable logic devices (PLDs) and consume 90 percent less static power and over 50 percent less dynamic power than 1.8 V “low-power” PLD alternatives. IGLOO 1.2 V operation often eliminates an additional DC/DC power converter for the 1.8 V power rail, saving power, area, and cost. Unlike other PLD technologies, flash-based IGLOO devices do not suffer from high inrush current or battery-sapping configuration current each time the system is powered up. Having a true ASIC-like power profile enables IGLOO FPGAs to dramatically extend battery life relative to SRAM and Hybrid PLD alternatives.

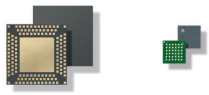
Flash-based IGLOO FPGAs are full-featured and include clock conditioning analog PLLs for clock generation, on-chip SRAM, and nonvolatile user memory storage, all of which help eliminate parts and reduce total system power consumption and cost.

Battery Life Experiment

Using IGLOO families can extend your product’s battery life dramatically. IGLOO devices can provide ten times the battery life of their nearest low-power competitor.

Low-Power Devices Are Just the Beginning

IGLOO FPGAs are true single-chip devices, do not require configuration or other support components, and offer a variety of small-footprint packages with high I/O pin count to match design needs.

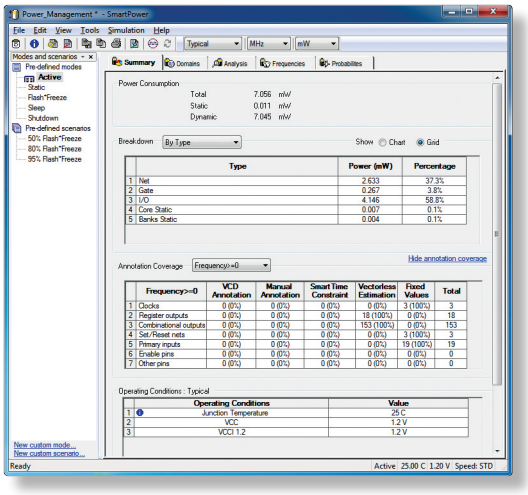


8x8 mm 3x3 mm

The IGLOO families are offered in a small-form-factor (3x3, 4x4, 5x5, 6x6, and 8x8 mm), high-density, chip-scale package and quad flat no-lead package.

Packages shown approximately to scale.

Like a digital ASIC, nonvolatile flash-based IGLOO devices have the advantage of being a secure, low-power, single-chip solution that is Level 0 instant-on. Unlike ASIC devices, IGLOO devices are reprogrammable and offer time-to-market benefits, allowing users to quickly and easily upgrade and update the design in the final stages of manufacturing or in the field without non-recurring engineering (NRE) charges and at an ASIC-level unit cost.



Comprehensive Power Analysis Tools

Microsemi provides accurate, comprehensive power analysis tools for IGLOO devices. These range from the Power Calculator (pre-netlist) tool for device comparison to post-layout, in-depth analysis and reporting tools. These tools provide an easy-to-use Power-Driven Layout (PDL) that can minimize design power by as much as 30 percent.

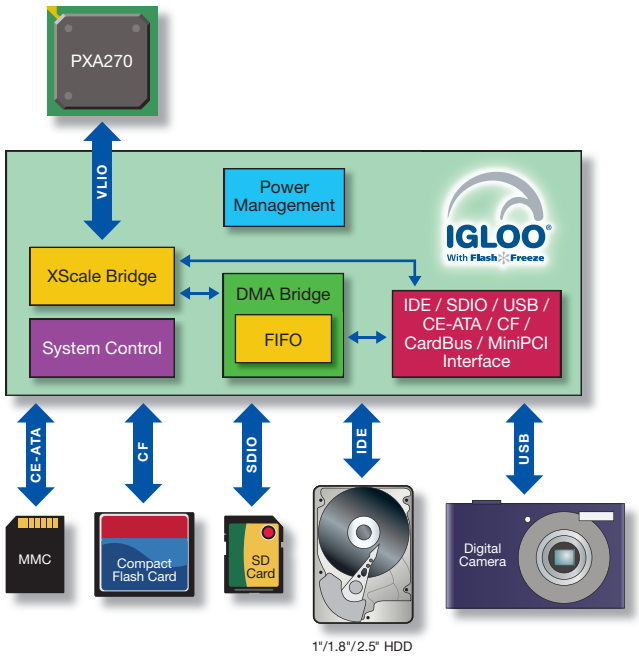
Prior to compiling a design, the enhanced spreadsheet-based Power Calculator helps in analyzing design implementation options for rapid "what if…" power analysis and design partitioning. Enhanced power reporting for low-power Flash*Freeze mode, and all other operating modes, enables the designer to calculate and predict total system power consumption, summing up power consumed in each mode.

The Libero® Integrated Design Environment (IDE) SmartPower tool provides market-leading netlist-based analysis capabilities. Power reports are broken down by net, gate, I/O, memory, clock, core static, instance, and power rail. A design-level power summary includes average switching activity, ambient temperature, and junction temperature readings.

Microsemi Power tools provide an accurate prediction that gives straightforward analysis of design options to help meet your system power budget.

Low-Power Solutions for Portable Devices

Microsemi provides a variety of low-power solutions, such as storage and display interfaces, to help customers get to market fast. Embedded processors need to work with one or more of the popular storage interfaces such as IDE, CE-ATA, SDIO, or CF. There is a pressing need to efficiently manage the interface for the storage devices by offloading the task from the processor to an FPGA. With its ultra-low power capabilities, ease of use, and reprogrammability, an IGLOO FPGA is the ideal choice. IGLOO devices can manage interfaces between the VLIO or AMBA bus and the different types of storage devices.



IGLOO Design Resources—Extensive Application Support

Microsemi provides extensive application support for IGLOO FPGAs, including board-level schematics, IP cores, and development platforms for low-power applications. Reference designs and documentation are available for cost-sensitive portable electronics, such as handheld and mobile storage, GPS, PDA, and smartphones, as well as portable medical and industrial applications.

IGLOO FPGA Product Family

IGLOO/e Devices

IGLOO Devices	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
ARM-Enabled IGLOO Devices				M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
Typical Equivalent Macrocells	256	512	1,024	2,048	—	—	—	—	—
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	75,264
Flash*Freeze Mode (typical, µW)	5	10	16	24	32	36	53	49	137
RAM (1,024 bits)	—	18	36	36	54	108	144	108	504
RAM Blocks (4,608 bits)	—	4	8	8	12	24	32	24	112
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1	1
AES-Protected ISP[1]	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs with CCC	—	1	1	1	1	1	1	6	6
VersaNet Globals[2]	6	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4	8	8
Maximum User I/Os	81	96	133	143	194	235	300	270	620
Package Pins UC CS QN VQ FG	 UC81 CS81 QN48 QN68 QN132 VQ100	 CS121[2] QN132 VQ100 FG144[2]	 CS196 QN132 VQ100 FG144	 CS81 CS196[3] QN132[3,4] VQ100 FG144	 CS196 FG144 FG256 FG484	 CS281 FG144 FG256 FG484	 CS281 FG144 FG256 FG484	 FG256 FG484	 FG484 FG896

Notes:
1. *AES is not available for Cortex-M1 IGLOO devices.*
2. *Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.*
3. *The M1AGL250 device does not support this package.*
4. *Device/package support TBD.*

I/Os Per Package

IGLOO Devices	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000		AGLE600		AGLE3000	
ARM-Enabled IGLOO Devices				M1AGL250				M1AGL600		M1AGL1000				M1AGLE3000	
I/O Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
QN48	34	—	—	—	—	—	—	—	—	—	—	—	—	—	—
QN68	49	—	—	—	—	—	—	—	—	—	—	—	—	—	—
UC81	66	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CS81	66	—	—	60	7	—	—	—	—	—	—	—	—	—	—
CS121	—	96	96	—	—	—	—	—	—	—	—	—	—	—	—
VQ100	77	71	71	68	13	—	—	—	—	—	—	—	—	—	—
QN132	81	80	84	87[1,4]	19[1,4]	—	—	—	—	—	—	—	—	—	—
CS196	—	—	133	143[1]	35[1]	143	35	—	—	—	—	—	—	—	—
FG144	—	96[7]	97	97	24	97	25	97	25	97	25	—	—	—	—
FG256[5]	—	—	—	—	—	178	38	177	43	177	44	165	79	—	—
CS281	—	—	—	—	—	—	—	215	53	215	53	—	—	—	—
FG484[5]	—	—	—	—	—	194	38	235	60	300	74	270	135	341	168
FG896	—	—	—	—	—	—	—	—	—	—	—	—	—	620	310

Notes:
1. *The M1AGL250 device does not support QN132 or CS196 packages.*
2. *Each used differential pair reduces the number of single-ended I/Os available by two.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *Device/package support TBD.*
5. *FG256 and FG484 are footprint-compatible packages.*

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